Capacitance of the MOS structure

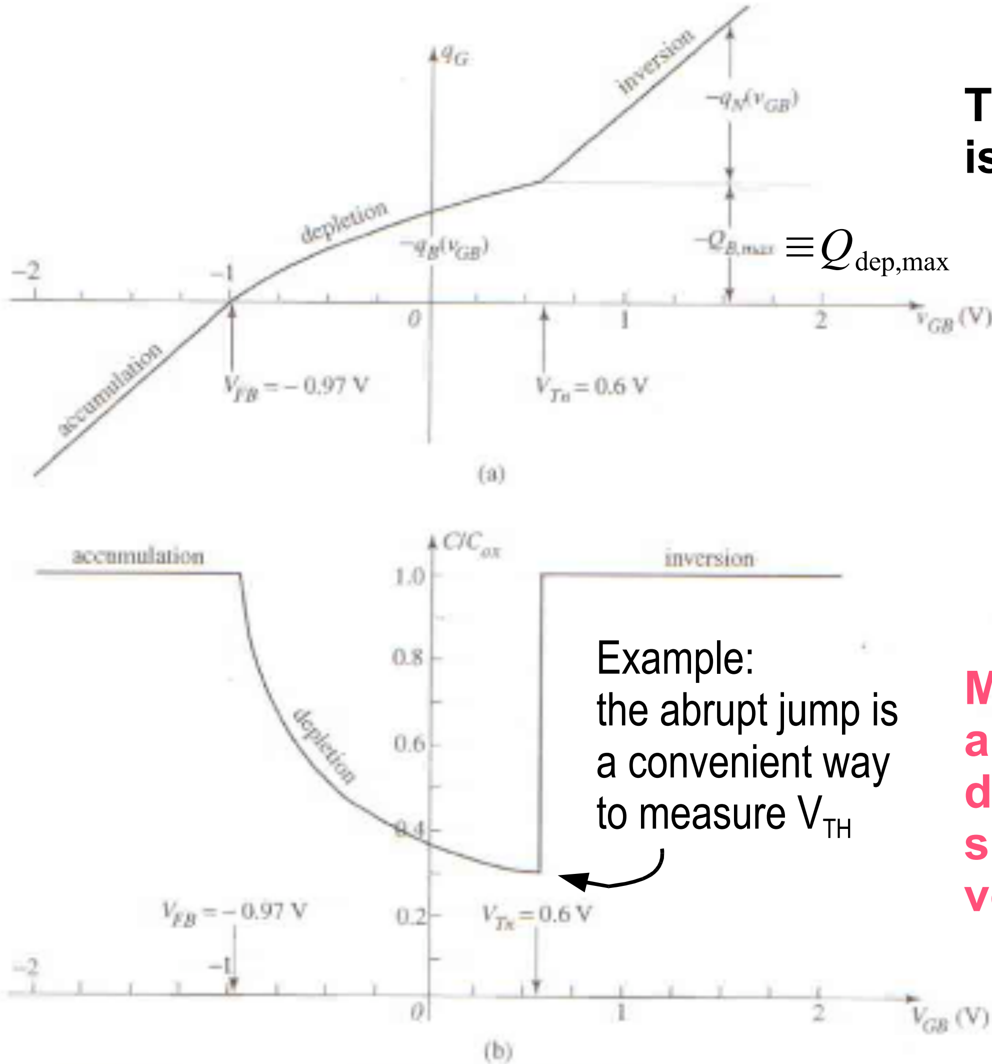


Figure 3.35 (a) Gate charge as a function of gate-bulk voltage for an MOS capacitor on a p-type substrate with a 150 Å-thick gate oxide and a substrate doping $N_a = 10^{17}$ cm^{-3} and (b) capacitance as a function of gate-bulk voltage, found by graphically differentiating (a).

The capacitance we refer in MOS theory is always the small signal capacitance:

$$C(V_{GB}) = \frac{dQ_g}{dV_{gb}}\Big|_{V_{GB}} \equiv \frac{dq_G}{dv_{GB}}\Big|_{V_{GB}}$$

MOS C-V Characteristic measurements are a commonly used method of determining gate oxide thickness, substrate doping concentration, flat-band voltage and threshold voltage

MOS C-V behavior

- Accumulation

$$C = C_{ox}$$

- Depletion

$$C = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \quad \textit{series of } C_{ox} \text{ and } C_{dep}$$

- Inversion

$$C = C_{ox}$$

Mathematical Derivation

- Accumulation: $v_{GB} \le V_{FB}$

$$\mathbb{C} = \frac{d\left[\mathbb{C}_{ox}\left(v_{GB} - V_{FB}\right)\right]}{dv_{GB}} \Big|_{V_{GB}} = \mathbb{C}_{ox}$$

- Inversion: $v_{GB} > V_{TH}$

$$\mathbb{C} = \frac{d\left[\mathbb{C}_{ox}\left(v_{GB} - V_{TH}\right) - \mathbb{Q}_{\text{dep,max}}\right]}{dv_{GB}} \Big|_{V_{GB}} = \mathbb{C}_{ox}$$

Mathematical Derivation

- Depletion: $V_{FB} < v_{GB} \le V_{TH}$

$$-\mathbb{Q}_{dep} = q N_A X_d$$

$$X_d = \frac{\epsilon_s}{\mathbb{C}_{ox}}\left(\sqrt{1+\frac{2\mathbb{C}_{ox}^2(v_{GB}-V_{FB})}{q N_A \epsilon_s}}-1\right)$$

$$\mathbb{C} = \frac{d[-\mathbb{Q}_{dep}]}{dv_{GB}}\bigg|_{V_{GB}} =$$

$$= \frac{d}{dv_{GB}}\left[\frac{q N_A \epsilon_s}{\mathbb{C}_{ox}}\left(\sqrt{1+\frac{2\mathbb{C}_{ox}^2(v_{GB}-V_{FB})}{q N_A \epsilon_s}}-1\right)\right]_{V_{GB}} =$$

$$= \frac{d}{dv_{GB}}\left[\frac{q N_A \epsilon_s}{\mathbb{C}_{ox}}\sqrt{1+\frac{2\mathbb{C}_{ox}^2(v_{GB}-V_{FB})}{q N_A \epsilon_s}}-\frac{q N_A \epsilon_s}{\mathbb{C}_{ox}}\right]_{V_{GB}} =$$

$$= \frac{q N_A \epsilon_s}{\mathbb{C}_{ox}} \frac{d}{dv_{GB}}\left[\left(\sqrt{1+\frac{2\mathbb{C}_{ox}^2(v_{GB}-V_{FB})}{q N_A \epsilon_s}}\right)\right]_{V_{GB}} = \longrightarrow$$

Mathematical Derivation

$$=\frac{qN_A\epsilon_s}{\mathbb{C}_{ox}}\frac{d}{dv_{GB}}\left[\left(1+\frac{2\mathbb{C}_{ox}^2(v_{GB}-V_{FB})}{qN_A\epsilon_s}\right)^{1/2}\right]_{V_{GB}}=$$

$$=\frac{qN_A\epsilon_s}{\mathbb{C}_{ox}}\left[\frac{1}{2}\left(1+\frac{2\mathbb{C}_{ox}^2(v_{GB}-V_{FB})}{qN_A\epsilon_s}\right)^{-1/2}\left(\frac{2\mathbb{C}_{ox}^2}{qN_A\epsilon_s}\right)\right]_{V_{GB}}=$$

$$=\frac{\mathbb{C}_{ox}}{\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}}}$$	**Capacitance in Depletion** $V_{FB}<v_{GB}\le V_{TH}$

- In order to better understand the “nature” of the capacitance we just found let's try to express it in term of the depletion layer width

Mathematical Derivation

$$X_d = \frac{\epsilon_s}{\mathbb{C}_{ox}}\left(\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}}-1\right) =$$

$$= \frac{\epsilon_s}{\mathbb{C}_{ox}}\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}} - \frac{\epsilon_s}{\mathbb{C}_{ox}}$$

$$\downarrow$$

$$X_d + \frac{\epsilon_s}{\mathbb{C}_{ox}} = \frac{\epsilon_s}{\mathbb{C}_{ox}}\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}}$$

$$\downarrow$$

$$\frac{1}{\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}}} = \frac{\epsilon_s/\mathbb{C}_{ox}}{X_d+\epsilon_s/\mathbb{C}_{ox}}$$

Mathematical Derivation

$$\frac{1}{\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}}}=\frac{\epsilon_s/\mathbb{C}_{ox}}{X_d+\epsilon_s/\mathbb{C}_{ox}}$$

$$\mathbb{C}=\frac{\mathbb{C}_{ox}}{\sqrt{1+\frac{2\mathbb{C}_{ox}^2(V_{GB}-V_{FB})}{qN_A\epsilon_s}}}=\frac{\epsilon_s}{X_d+\epsilon_s/\mathbb{C}_{ox}}=\frac{1}{\frac{X_d}{\epsilon_s}+\frac{1}{\mathbb{C}_{ox}}}$$

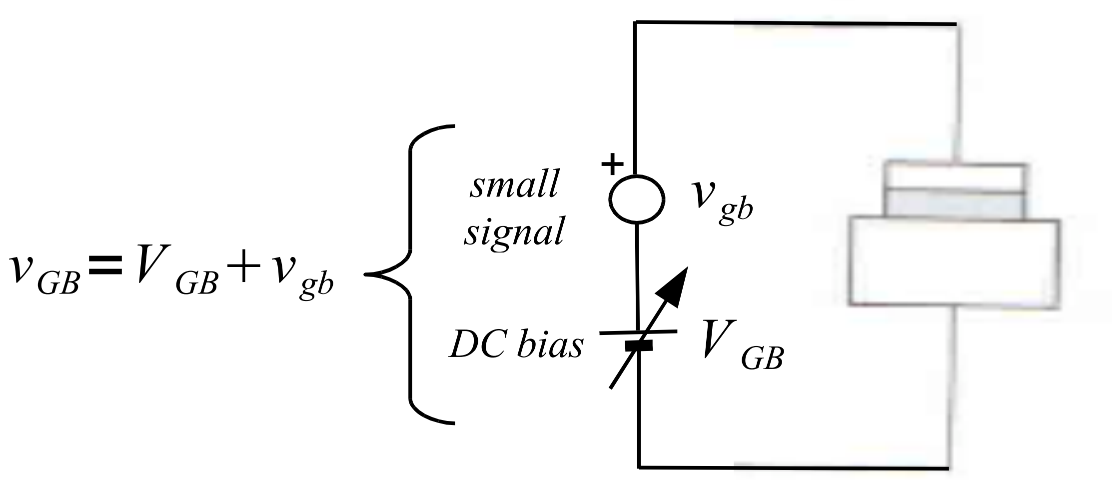
NOTE: ϵ_s/X_d is simply the capacitance per area of the depletion region

$$\mathbb{C}=\frac{1}{\frac{1}{\frac{\epsilon_s}{X_d}}+\frac{1}{\mathbb{C}_{ox}}}=\frac{1}{\frac{1}{\mathbb{C}_{dep}}+\frac{1}{\mathbb{C}_{ox}}}=\frac{\mathbb{C}_{ox}\cdot\mathbb{C}_{dep}}{\mathbb{C}_{ox}+\mathbb{C}_{dep}}$$

Series of $\mathbb{C}_{ox}$ and $\mathbb{C}_{dep}$

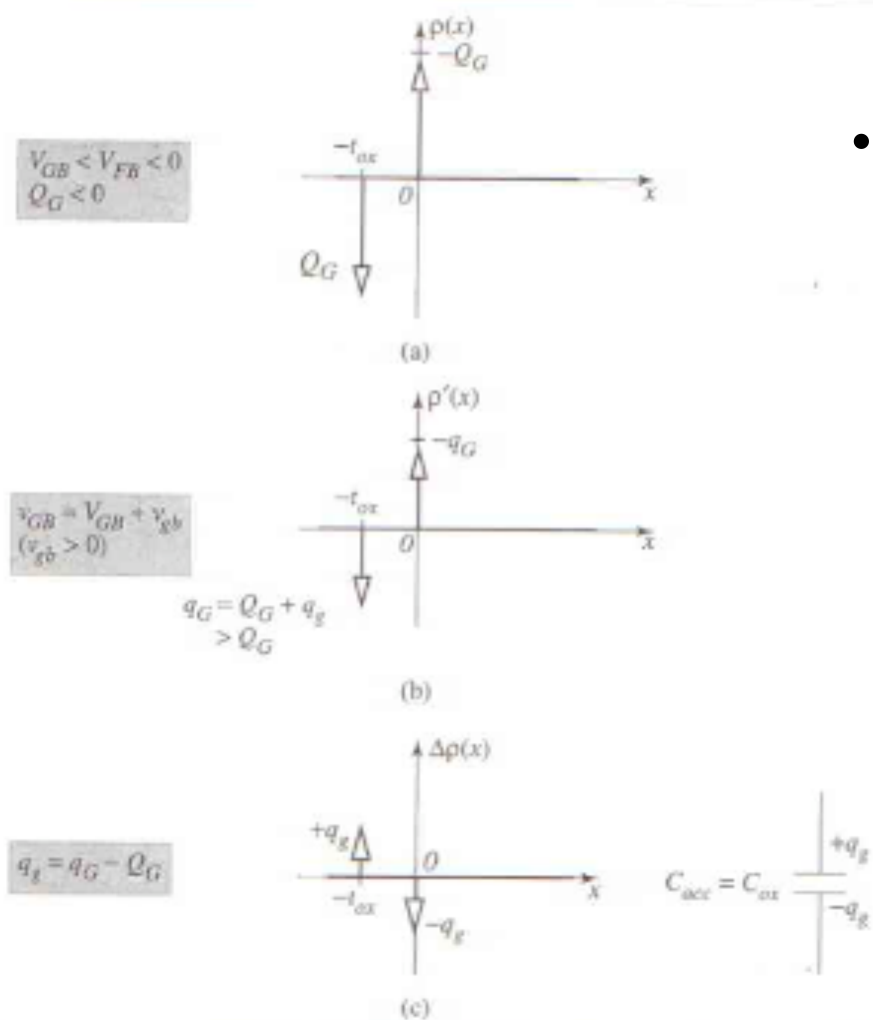
Physical Interpretation

- We investigate where the increment in gate charge q_g due to a positive increment in the gate voltage v_{gb} (relative to the DC gate voltage V_{GB} and charge Q_G) is mirrored for each of the three operating regions



MOS capacitor

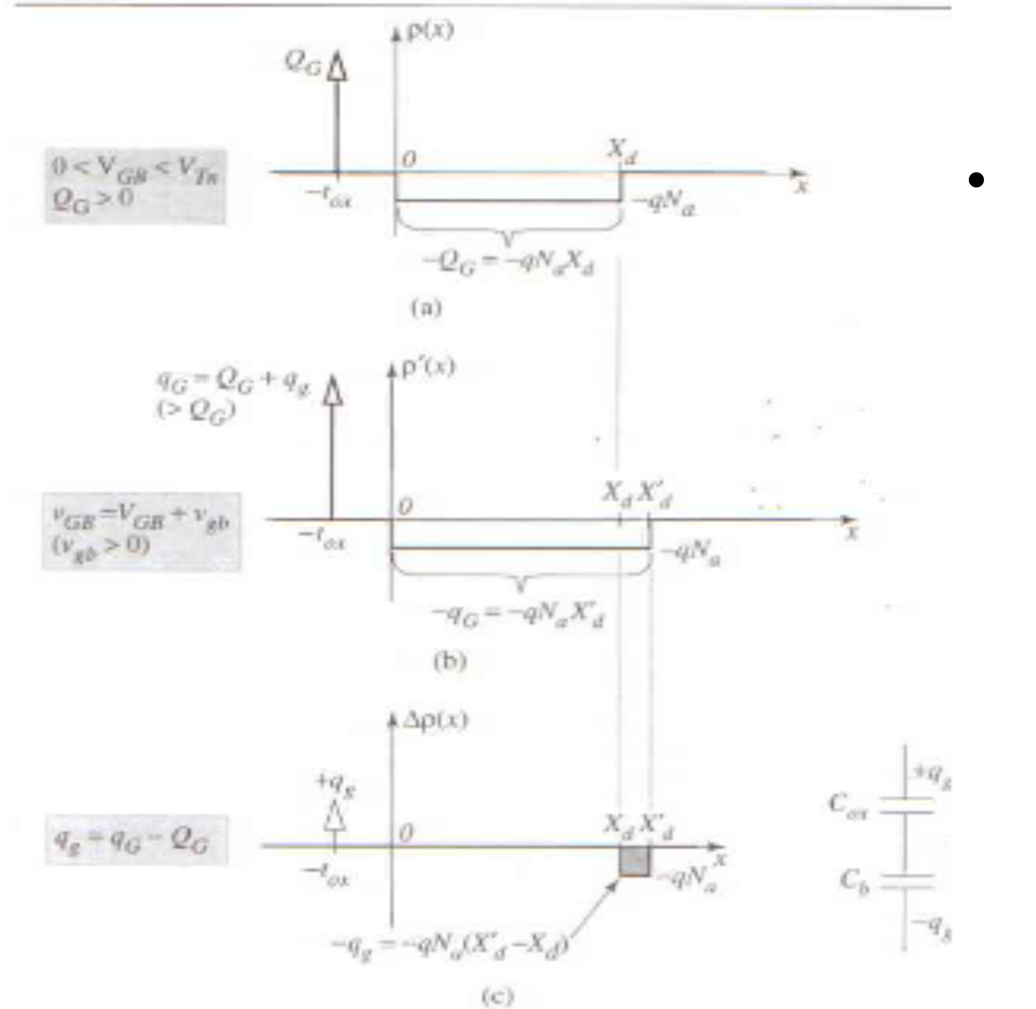
Accumulation



➤ **Figure 3.37** Charge density $\rho(x)$ for a MOS structure on a p-type substrate in accumulation: (a) bias voltage $V_{GB} < V_{FB}$, (b) perturbed charge density $\rho'(x)$ for $v_{GB} = V_{GB} + v_{gb}$, where the incremental voltage $v_{gb} > 0$, and (c) incremental charge density $\Delta\rho(x) = \rho'(x) - \rho(x)$ showing that the incremental charges $\pm q_g$ are separated by the gate oxide. The small-signal model in accumulation is the oxide capacitance.

- The charge increment on the gate is mirrored in the accumulated holes under the oxide/substrate interface

Depletion



➤ **Figure 3.38** Charge density ρ(x) for a MOS structure on a p-type substrate in depletion: (a) bias voltage $V_{FB} < V_{GB} < V_{Tn}$, (b) perturbed charge density $\rho'(x)$ for $v_{GB} = V_{GB} + v_{gb}$, where the incremental voltage $v_{gb} > 0$, and (c) incremental charge density $\Delta\rho(x) = \rho'(x) - \rho(x)$ showing that the incremental charges $\pm q_g$ are separated by the gate oxide and the depletion region. The small-signal model in depletion is two capacitors in series.

- The gate charge increment is mirrored at the bottom of the depletion region. The incremental charges $+q_g$ and $–q_g$ are separated by an oxide layer of thickness t_{ox} with capacitance $C_{ox} = \varepsilon_s/t_{ox}$ and a depletion region of thickness $X_d(V_{GB})$ with capacitance $\varepsilon_s/X_d(V_{GB})$.

Inversion

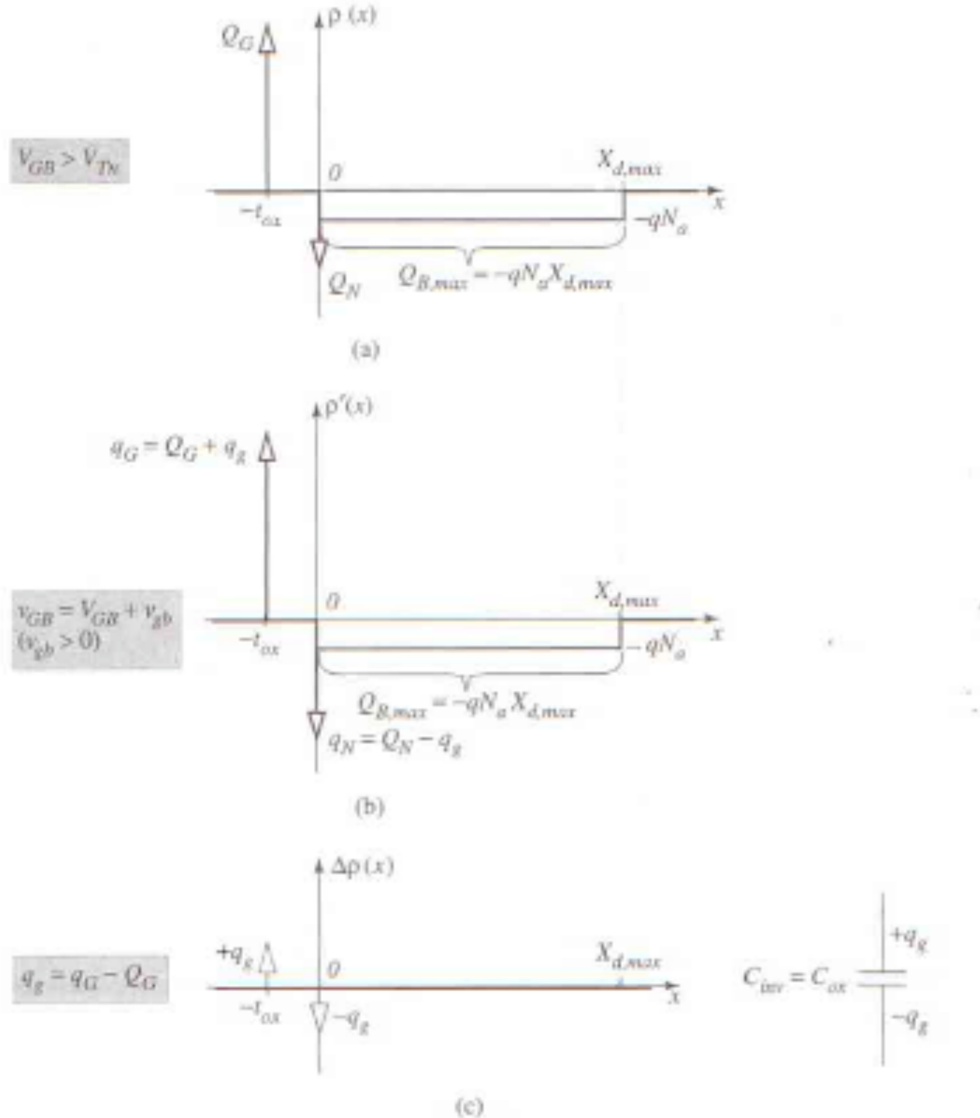
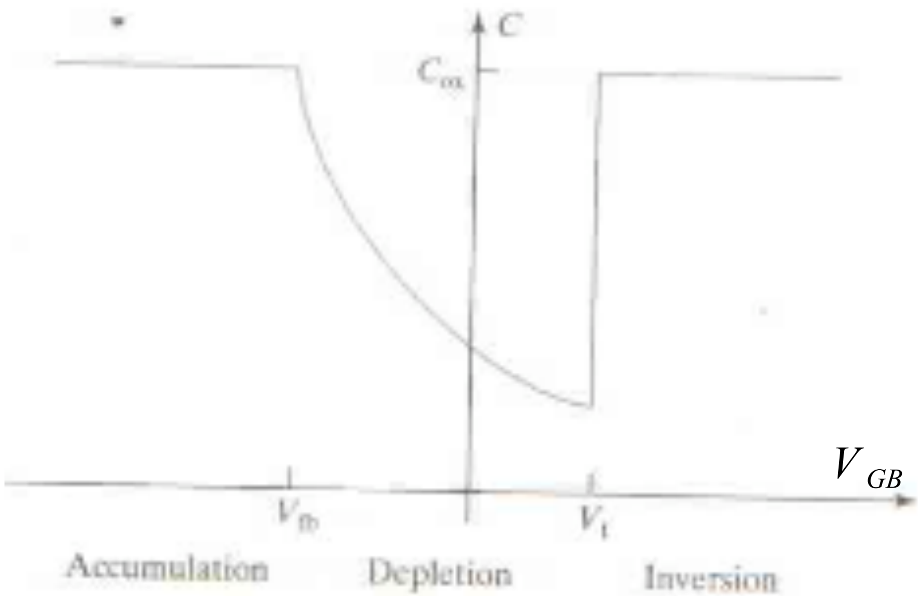


Figure 3.39 Charge density ρ(x) for a MOS capacitor on a p-type substrate in inversion: (a) bias voltage $V_{GB} > V_{Tn}$, (b) perturbed charge density ρ′(x) for $v_{GB} = V_{GB} + v_{gb}$, where the incremental voltage $v_{gb} > 0$, and (c) incremental charge density $\Delta\rho(x) = \rho'(x) - \rho(x)$ showing that the incremental gate charge is mirrored by an increment in the electron inversion charge. Therefore, the small-signal model in the inversion region is again the oxide capacitance.

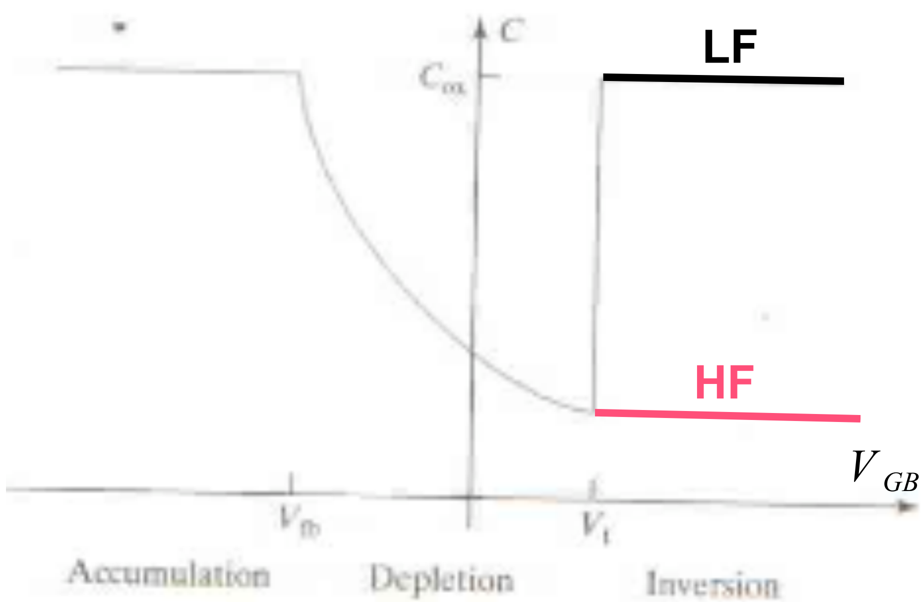
For an inverted MOS capacitor, an increment in gate voltage is mirrored in an increase electron charge in the inversion layer

MOS C-V behavior with frequency

- LF



- HF



- If the signal is too fast the device cannot keep up forming the inversion layer