Problem Set

Problem #1

Using custom designer and Synopsys 90 nm technology (V_{DD}=1.2V, T=25°C) draw the transistor schematic of a CMOS compound AND-OR-INVERT gate implementing the following function:

F = not [(A+B) * C]

Verify exhaustively the correct functionality of the gate through an HSPICE transient simulation.

NOTE: Assume the gate is loaded by a capacitance equal to 8*Csl and the slope of the input signals is equal to 6.4*Tisl.

Browse Synopsys 90nm SAED_Digital_Standard_Cell_Library Databook to find out the value of the capacitive standard load Csl and the input signal slope Tisl.

Problem #2

Using custom designer and Synopsys 90 nm technology draw the transistor schematic of a CMOS compound OR-OR-AND-INVERT gate implementing the following function:

F = not [(A+B) * (C+D)]