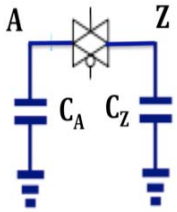
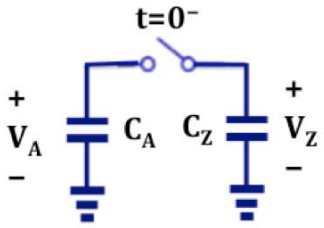
Problem Set

Problem 1

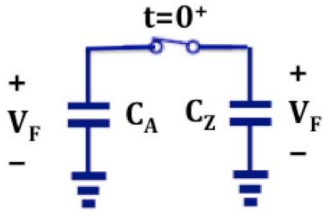
Whenever logic gates are built using transmission gates or pass transistors an important issue that need to be taken in consideration is the so called charge sharing problem.



Assume the transmission gate (or pass transistor) in initially “open” and the capacitances CA and CZ are respectively charged at VA and VZ.



Find out the voltage across CA and CZ when the transmission gate (or pass transistor) is finally “closed”.



Problem

Draw the logic-level schematic of a CMOS positive edge triggered D flip-flop with asynchronous clear (use only inverters, 2-input nands, and transmission gates)

Truth Table:

d	cp	cd	q
0	↑	1	0
1	↑	1	1
x	x	0	0

approach: just use a nand gate instead of an inverver in the feedback path of the basic latch cell