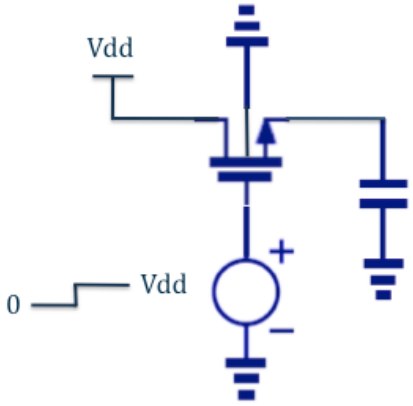
# *Problem Set*

Problem #1




Given the simple nMOS pass transistor circuit shown compute the max voltage that is possible to pass to the load capacitor (CL=16fF). Design the nMOS pass transistor to be unit size in TSMC 180nm technology.
Verify your hand derivations are consistent with the hspice simulation.

Write a short report including:

1. Hand calculation (state clearly any assumption you make)
2. hspice deck
3. Input and output voltage waveforms (using either CosmosScope or CustomExplorer)
4. How much is the relative error between hand calculation and SPICE result. Explain the discrepancy.

Problem #2

Design a transmission gate using TSMC 180nm technology, and characterize its resistance using HSPICE

Add to the report

1. HSPICE deck
2. Plots of:
    - The resistance Rds of the transmission gate vs. Vin (sweep Vin from 0 to VDD)
    - The resistance Rdsn of the nMOS transistor vs. Vin (sweep Vin from 0 to VDD)
    - The resistance Rdsp of the pMOS transistor vs. Vin (sweep Vin from 0 to VDD)