# Problem Set

## Problem #1

Consider the schematic of the compound CMOS or-and-invert gate you designed in one of the previous problem sets.

$$F = \overline{(A + B) \bullet C}$$

1. Sketch a stick diagram of the layout
2. Estimate the area from the stick diagram

## Problem #2

Consider the schematic of the compound CMOS or-or-and-invert gate you designed in one of the previous problem sets:

$$F = \overline{(A + B) \bullet (C + D)}$$

1. Sketch a stick diagram of the layout
2. Estimate the area from the stick diagram

## Problem #3

Figure 1.75 gives the stick diagram for a level-sensitive latch.

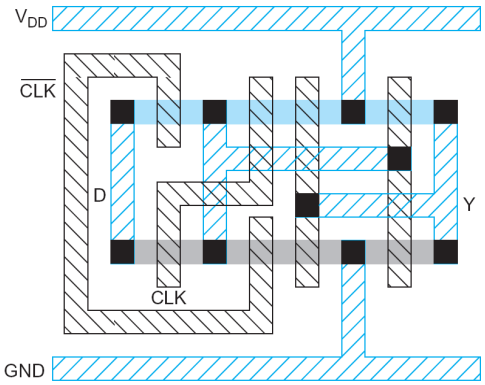


Fig.1.75 Level-sensitive latch stick diagram

1. Estimate the area of the latch.
2. Using LTSpice draw a transistor level schematic for the latch
3. How does the schematic differ from the schematic of the latch given in Fig. 1.31(b)

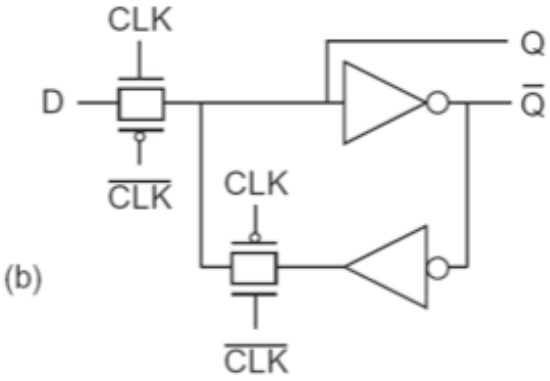


Figure 1.31 (b) CMOS positive-level-sensitive D-latch