TSMC 0.18μm Process 1.8-Volt SAGE-X™ Standard Cell Library Databook

October 2001

Release 3.1

DB-SX-TSM003-3.1/18

Artisan Components, Inc., 141 Caspian Court, Sunnyvale, CA 94089, USA

Table of Contents

Base Cells

Synthesis Optimized Arithmetics

Advanced Arithmetics

Register File Cells

Release History

This section contains the release history for the TSMC 0.18µm Process 1.8-Volt SAGE-X™ Standard Cell Library Databook. For more detailed technical information, please contact Artisan Customer support at support@artisan.com.

Part Number	Release Number	Date of Release	Updates
DB-SX-TSM003-1.0/18	1.0	March 2000	• Initial Release
DB-SX-TSM003-2.2/18	2.2	September 2000	• Document updated
DB-SX-TSM003-3.0/18	3.0	July 2001	• A*CSH* cells redesigned
DB-SX-TSM003-3.1/18	3.1	October 2001	• Update adder cells

Customer Support

For all customer service or technical support questions, please visit the Artisan Components Web site at www.artisan.com and click on Customer Support.

You may also contact Artisan by telephone or email, using the following information:

- United States and North America 877-ARTILIB (877-278-4542)
- International 408-548-3298
- Email support@artisan.com

Introduction

Artisan's SAGE-X™ standard cell library builds upon our SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- ***Global Parameters*** provides an overview of parameters specific to your SAGE-X library.
- ***Special Cells*** details the types of special cells you will find included in the library.
- ***Reading the Standard Cell Datasheet*** describes what you will find in each datasheet.

Datasheets for each cell in this lirbary are provided after the introduction. The datasheets are included in alphabetical order within the following catgories:

- Base Cells
- Custom Cells (if your project includes these)
- Advancec Arithmetics
- Register File Cells
- Symthesis Optimized Arithmetics

Global Parameters

This section specifies global parameters for the TSMC 0.18µm Process 1.8-Volt SAGE-X™ Standard Cell Library Databook. It covers physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this SAGE-X Standard Cell Library.

Table 1. Physical Specifications

Drawn Gate Length (µm)	0.18
Layers of Metal	4, 5, or 6
Layout Grid (µm)	0.005
Vertical Pin Grid (µm)	0.56
Horizontal Pin Grid (µm)	0.66
Cell Power and Ground Rail Width (µm)	0.8

In this library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

This library also supports designs with 4, 5, or 6 layers of metal. The designer may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "Design Rule 0.18µm LOGIC Salicide 1.8V/3.3V Process" design rule manual. The designer must define these correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

Parameter	Minimum	Maximum
DC Supply Voltage (Vdd)	1.62 V	1.98 V
Junction Temperature	0°C	125°C

Table 3 shows the derating factors for this SAGE-X Standard Cell Library.

Table 3. Derating Factors

$K_{Process}$ (slow)	1.293
$K_{Process}$ (typical)	1.000 (by definition)
$K_{Process}$ (fast)	0.781
K_{Volt} (1.8V to 1.62V)	-0.731/V
K_{Volt} (1.8V to 1.98V)	-0.511/V

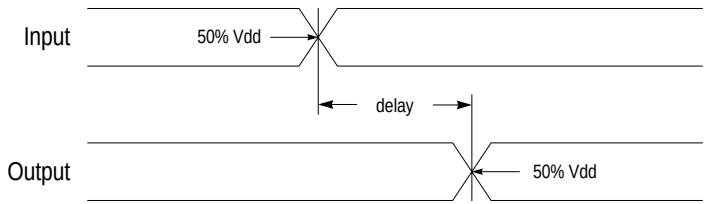
Table 3. Derating Factors

$K_{Process}$ (slow)	1.293
K_{Temp} (25°C to 0°C)	0.00137/°C
K_{Temp} (25°C to125°C)	0.00123/°C

Propagation Delay

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates propagation delay.

Figure 1. Propagation Delay



Factors that affect propagation delays include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints (see below). The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.03ns and a linearized load factor, K_{load}, which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.66µm horizontal pitch) and metal3 (0.56µm vertical pitch) routing grid across the entire cell layout.

The SAGE-X Standard Cell Library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. The derating factor table on page 10 provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is

$$t_{TPD} = (K_{Process}) \bullet [1+(K_{Volt} \bullet \Delta Vdd)] \bullet [1+(K_{Temp} \bullet \Delta T)] \bullet t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} \bullet C_{load})$$

where:

t_{TPD}	=	total propagation delay (ns);
$t_{typical}$	=	delay at typical corner—1.8V, 25°C, typical process (ns);
$t_{intrinsic}$	=	delay through the cell when there is no output load (ns);
K_{load}	=	load delay multiplier (ns/pF);
C_{load}	=	total output load capacitance (pF);
$K_{Process}$	=	process derating factor, where process is slow, typical, or fast;
K_{Volt}	=	voltage derating factor (/V);
ΔVdd	=	Vdd —1.8V;
K_{Temp}	=	temperature derating factor (/°C);
ΔT	=	junction temperature — 25°C.

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

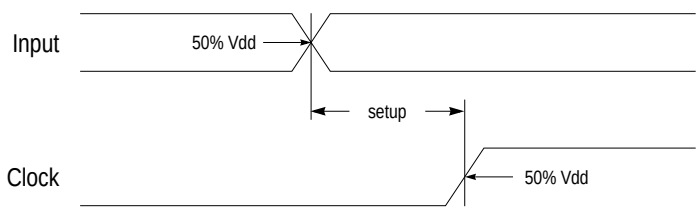
The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.03ns data slew and 0.03ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.66µm horizontal pitch) and metal3 (0.56µm vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 2 illustrates setup time for a positive-edge-triggered sequential cell.

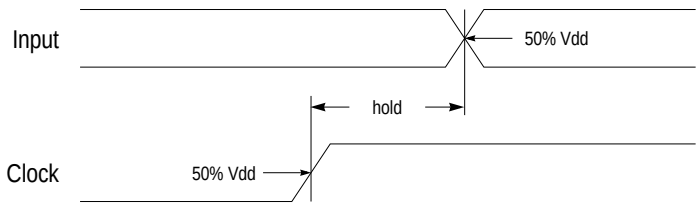
Figure 2. Setup Time



Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the clock signal crossing 50% of Vdd and the data signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 3 illustrates hold time for a positive-edge-triggered sequential cell.

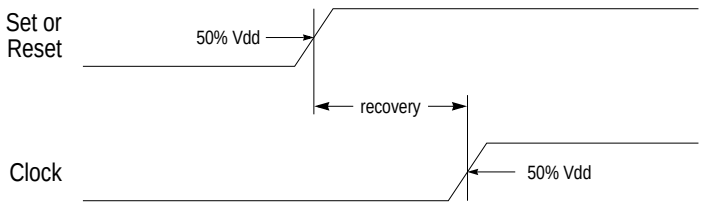
Figure 3. Hold Time



Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. Figure 4 illustrates recovery time.

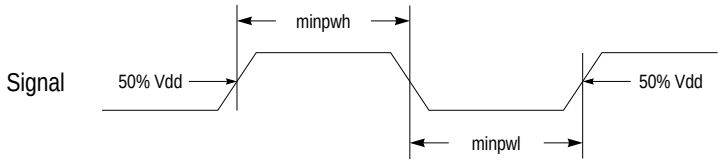
Figure 4. Recovery Time



Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 5 illustrates minimum pulse width.

Figure 5. Minimum Pulse Width



Minimum pulse width is defined to be 0.50 ns for all set/reset pins (SN, RN) and 0.18 ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Power Dissipation

The SAGE-X Standard Cell Library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the SAGE-X Library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The SAGE-X Library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell (µW/MHz) when the corresponding pin changes state at 25 ^{o}C, V, and typical process. The energy data in the tables were measured for an input slew of 0.03 ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

where:

P_{avg} = average power (µW);

x = number of input pins;

E_{in} = energy associated with the *n*th input pin (µW/MHz);

f_{in} = frequency at which the *n*th input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the *n*th output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd = operating voltage = 1.8V;

f_{on} = frequency at which the *n*th output pin changes state during the normal operation of the design (MHz);

E_{os} = energy associated with the output pin for sequential cells only (µW/MHz).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator, for example Verilog, by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

For example, for a DFFXL cell with clock switching at 133MHz, input and output pins switching at 20MHz, an external capacitive loading on the output pin of 0.02pF, and using the power table in the DFF datasheet shown on page 26, the power dissipated by the DFFXL is given by the equation:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

Substituting,

x =2;

E_{i1} = 0.00306 µW/MHz;

E_{i2} = 0.0335 µW/MHz;

f_{i1} = 20 MHz;

f_{i2} = 133 MHz;

y =2;

C_{o1} =0.02 pF;

C_{o2} =0.02 pF;

Vdd= 1.8V;

f_{o1} =20 MHz;

f_{o2} =20 MHz;

E_{os} =0.0260 µW/MHz

we have:

$$P_{avg} = \sum_{n=1}^{2} (E_{in} \bullet f_{in}) + \sum_{n=1}^{2} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1}$$

$$P_{avg} = (E_{i1} \bullet f_{i1}) + (E_{i2} \bullet f_{i2}) + \left(C_{o1} \bullet 1.8^2 \bullet \frac{1}{2} f_{o1} \right) + \left(C_{o2} \bullet 1.8^2 \bullet \frac{1}{2} f_{o2} \right) + (E_{os} \bullet f_{o1})$$

$$P_{avg} = (0.0306 \bullet 20) + (0.0335 \bullet 133) + \left(0.02 \bullet 3.24 \bullet \frac{1}{2}(20)\right) + \left(0.02 \bullet 3.24 \bullet \frac{1}{2}(20)\right) + (0.0260 \bullet 20)$$

$$P_{avg} = 6.89 \ \mu W$$

Power-Rail Strapping

The designer must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The following guidelines provide a rough estimate with many simplifying assumptions. For a given module design, the designer can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

I_{avg} = total average current for the module, calculated from previous section (mA);

w_{m1} = VSS/VDD metal1 wire width (µm), see Physical Specifications;

r = number of rows in module;

d_{m1} = maximum metal1 current density allowed for the process (mA/µm);

d_{m2} = maximum metal2 current density allowed for the process (mA/µm);

I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);

I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);

w_{m2} = metal2 wire width required for vertical strapping (µm);

c = minimum number of metal2 straps;

we have:

$I_{m1} = w_{m1} \bullet r \bullet 2 \bullet d_{m1}$,

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$I_{strap} = \frac{(I_{avg} - I_{m1})}{2}$,

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$w_{m2} = \frac{I_{strap}}{d_{m2}}$,

It is recommended that the metal2 wire width, w_{m2}, be divided into c equal portions which are spaced equidistant across the module, where

$c = \frac{I_{avg}}{I_{m1}}$, rounded up to the next integer.

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the SAGE-X Standard Cell Library, each cell is designed with a uniform cell height of 5.0µm (i.e., 9 tracks tall with 0.56µm per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, the designer may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s). Table 4 indicates which

DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

Row Separation in Number of Grids	Expected DRC Violations	Action to Correct DRC Violations
0 (Rows Abut)	None	None
1	None	None
2	NWELL space < 0.6 µm	Draw NWELL layer between rows to merge NWELL regions above and below row separation.
3	None	None
4	None	None
5 or more	None	None

Special Cells

This section discusses special cells in the SAGE-X Standard Cell Library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The 0.18 TSMC antenna effect prevention guideline, "Design Rule 0.18mm LOGIC Salicide 1.8V/3.3V Process," specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

Fill Cells

The library contains several FILL cells: FILL1, FILL2, FILL4, FILL8, FILL16, FILL32, FILL64. The number appended to "FILL" in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow the designer to adjust a given delay path with a simple cell substitution after place and route.

Reading the Standard Cell Datasheet

Please refer to the datasheet for DFF on pages 25 and 26 for the arrangement of each of the following datasheet sections.

1. Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Function Table

The function table gives all possible combinations of input and output signals for the cell. Table 5 defines the symbols used in datasheet function tables.

Table 5. Function Table Key

Symbol	Description
0	Logic Low
1	Logic High
⎺_	High to Low Transition
_/⎺	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (µm) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an "X" followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed (µW/MHz) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell are calculated at 25°C, 1.8V, typical process, input slew of 0.03ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell are calculated at 25°C, 1.8 V, typical process, and input slew of 0.03 ns.

10. Timing Constraints

The timing constraints table shows the timing conditions (ns) required at 25°C, 1.8 V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.03 ns data slew and 0.03 ns clock slew. Hold constraint values are measured for 0.03 ns data slew and 0.03 ns clock slew. Minimum pulse width is defined to be 0.50 ns for all set/reset pins and 0.18 ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

DFF

1

2

Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

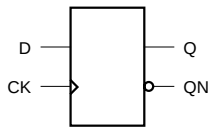
3

Functions

D	CK	Q[n+1]	QN[n+1]
0	↑	0	1
1	↑	1	0
x	↓	Q[n]	QN[n]

4

Logic Symbol



5

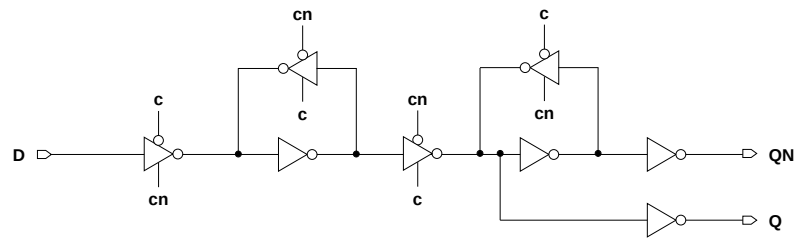
Cell Size

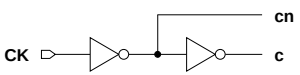
Drive Strength	Height (µm)	Width (µm)
DFFXL	5.0	11.2
DFFX1	5.0	11.2
DFFX2	5.0	13.9
DFFX4	5.0	16.5

7

6

Functional Schematic





DFF

8 **AC Power**

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0306	0.0276	0.0368	0.0606
CK	0.0335	0.0318	0.0396	0.0579
Q	0.0260	0.0346	0.0614	0.1091

7

11 **Pin Capacitance**

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0033	0.0020	0.0024	0.0038
CK	0.0020	0.0026	0.0038	0.0059

9 **Delays at 25°C, 1.8V, Typical Process**

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.219	0.197	0.180	0.155	5.696	4.288	2.261	1.139
CK → Q↓	0.179	0.166	0.153	0.132	3.406	2.469	1.234	0.611
CK → QN↑	0.238	0.221	0.196	0.179	6.239	4.518	2.259	1.138
CK → QN↓	0.304	0.280	0.251	0.219	3.342	2.444	1.219	0.605

10 **Timing Constraints at 25°C, 1.8V, Typical Process**

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.04	0.06	0.06	0.06
	setup↓ → CK	0.10	0.15	0.15	0.14
	hold↑ → CK	-0.02	-0.04	-0.04	-0.03
	hold↓ → CK	0.01	-0.04	-0.04	-0.04
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25

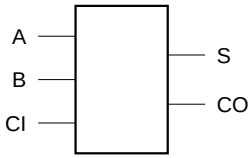
Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



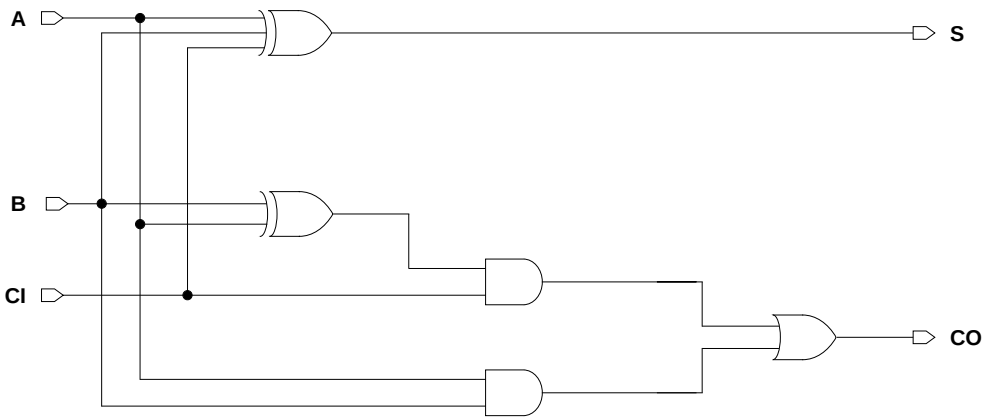
Functions

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
ADDFXL	5.0	13.9
ADDFX1	5.0	13.9
ADDFX2	5.0	13.9
ADDFX4	5.0	15.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.1044	0.1083	0.1290	0.1978
B	0.1668	0.1378	0.1771	0.2502
CI	0.0557	0.0580	0.0826	0.1559

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0020	0.0070	0.0070	0.0070
B	0.0020	0.0067	0.0067	0.0067
CI	0.0062	0.0061	0.0061	0.0061

Delays (25°C, 1.8V, Typical Process)

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.454	0.202	0.220	0.269	6.395	4.529	2.253	1.117
A → S↓	0.497	0.271	0.300	0.362	4.155	2.584	1.335	0.688
B → S↑	0.720	0.236	0.250	0.289	6.364	4.535	2.256	1.119
B → S↓	0.589	0.308	0.337	0.400	4.188	2.583	1.336	0.687
CI → S↑	0.209	0.159	0.186	0.249	6.329	4.531	2.254	1.118
CI → S↓	0.153	0.141	0.168	0.226	4.070	2.585	1.343	0.698
A → CO↑	0.484	0.247	0.275	0.338	6.239	4.515	2.245	1.110
A → CO↓	0.522	0.244	0.272	0.324	3.591	2.502	1.297	0.668
B → CO↑	0.555	0.284	0.312	0.374	6.239	4.513	2.244	1.110
B → CO↓	0.758	0.263	0.286	0.330	3.666	2.458	1.265	0.641
CI → CO↑	0.153	0.128	0.155	0.217	6.272	4.527	2.251	1.115
CI → CO↓	0.211	0.168	0.196	0.252	3.637	2.521	1.305	0.672

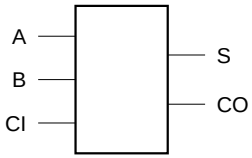
Cell Description

The ADDFH cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



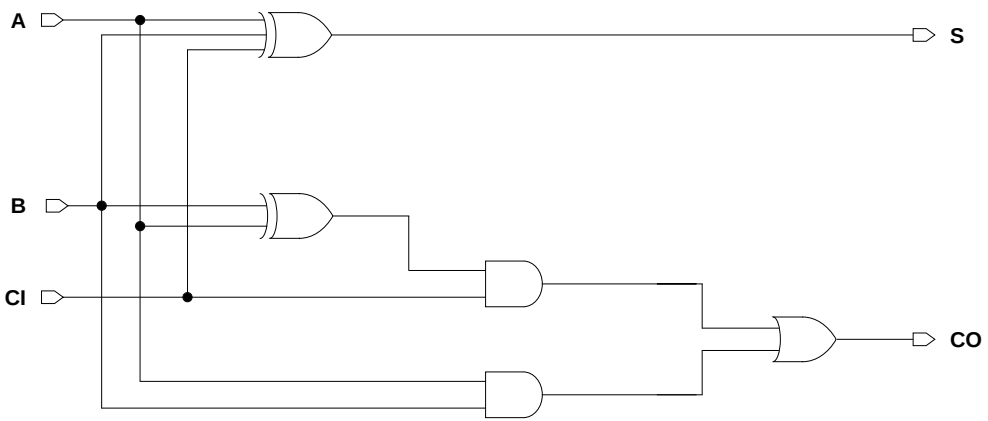
Functions

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
ADDFHXL	5.04	14.52
ADDFHX1	5.04	15.18
ADDFHX2	5.04	22.44
ADDFHX4	5.04	23.10

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.1006	0.1259	0.2494	0.2886
B	0.0889	0.1151	0.2144	0.2538
CI	0.0574	0.0673	0.1162	0.1551

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0039	0.0061	0.0116	0.0116
B	0.0079	0.0138	0.0260	0.0260
CI	0.0021	0.0041	0.0080	0.0081

Delays (25°C, 1.8V, Typical Process)

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.322	0.217	0.221	0.236	6.245	4.519	2.249	1.063
A → S↓	0.313	0.245	0.240	0.266	3.476	2.476	1.222	0.671
B → S↑	0.229	0.159	0.147	0.166	6.262	4.522	2.249	1.064
B → S↓	0.293	0.193	0.179	0.208	3.488	2.475	1.222	0.671
CI → S↑	0.282	0.179	0.154	0.177	6.252	4.522	2.250	1.064
CI → S↓	0.249	0.177	0.150	0.182	3.517	2.482	1.225	0.673
A → CO↑	0.324	0.217	0.224	0.238	6.251	4.520	2.249	1.064
A → CO↓	0.324	0.242	0.242	0.266	3.576	2.478	1.224	0.672
B → CO↑	0.196	0.140	0.135	0.150	6.272	4.517	2.249	1.063
B → CO↓	0.311	0.182	0.173	0.196	3.601	2.455	1.219	0.667
CI → CO↑	0.130	0.101	0.087	0.098	6.267	4.523	2.250	1.064
CI → CO↓	0.208	0.145	0.128	0.151	3.695	2.498	1.234	0.676

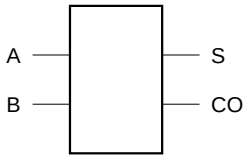
Cell Description

The ADDH cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$$

$$CO = A \bullet B$$

Logic Symbol



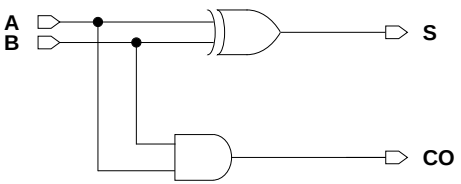
Functions

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
ADDHXL	5.0	7.3
ADDHX1	5.0	7.9
ADDHX2	5.0	11.9
ADDHX4	5.0	18.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0576	0.1026	0.1844	0.3550
B	0.0423	0.0540	0.1018	0.1779

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0047	0.0104	0.0213	0.0415
B	0.0059	0.0082	0.0126	0.0241

Delays (25°C, 1.8V, Typical Process)

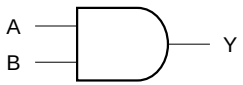
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → S↑	0.124	0.077	0.065	0.062	7.069	2.756	1.348	0.671
A → S↓	0.129	0.081	0.073	0.068	3.917	1.629	0.803	0.397
B → S↑	0.060	0.052	0.049	0.043	6.981	2.732	1.337	0.665
B → S↓	0.076	0.070	0.066	0.061	3.716	1.558	0.770	0.382
A → CO↑	0.070	0.081	0.074	0.068	6.242	4.520	2.219	1.110
A → CO↓	0.091	0.117	0.102	0.097	3.308	2.619	1.222	0.612
B → CO↑	0.068	0.081	0.072	0.065	6.242	4.520	2.219	1.110
B → CO↓	0.083	0.111	0.096	0.090	3.303	2.616	1.221	0.611

Cell Description

The AND2 cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$Y = (A \bullet B)$

Logic Symbol



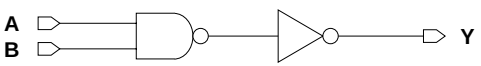
Functions

A	B	Y
0	x	0
x	0	0
1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AND2XL	5.0	2.6
AND2X1	5.0	2.6
AND2X2	5.0	2.6
AND2X4	5.04	3.30

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0176	0.0200	0.0286	0.0503
B	0.0199	0.0228	0.0315	0.0598

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0021	0.0019	0.0032	0.0058
B	0.0021	0.0020	0.0033	0.0063

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.079	0.084	0.068	0.065	6.250	4.523	2.261	1.034
A → Y↓	0.092	0.112	0.090	0.100	3.318	2.448	1.220	0.737
B → Y↑	0.083	0.088	0.072	0.069	6.247	4.521	2.261	1.034
B → Y↓	0.101	0.123	0.099	0.112	3.324	2.451	1.221	0.737

Cell Description

The AND3 cell provides the logical AND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C)$$

Logic Symbol

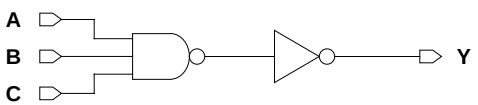
Functions

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AND3XL	5.0	3.3
AND3X1	5.0	3.3
AND3X2	5.0	3.3
AND3X4	5.0	4.0

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0187	0.0209	0.0319	0.0606
B	0.0210	0.0229	0.0359	0.0688
C	0.0241	0.0250	0.0405	0.0763

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0026	0.0023	0.0035	0.0068
B	0.0024	0.0022	0.0036	0.0074
C	0.0024	0.0022	0.0037	0.0081

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.095	0.105	0.087	0.075	6.260	4.530	2.242	1.141
A → Y↓	0.111	0.129	0.109	0.094	3.135	2.633	1.228	0.608
B → Y↑	0.104	0.113	0.096	0.084	6.258	4.530	2.241	1.141
B → Y↓	0.122	0.140	0.120	0.106	3.145	2.636	1.230	0.609
C → Y↑	0.107	0.117	0.099	0.088	6.259	4.530	2.242	1.141
C → Y↓	0.134	0.151	0.131	0.117	3.156	2.642	1.232	0.610

Cell Description

The AND4 cell provides the logical AND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B \bullet C \bullet D)$$

Logic Symbol

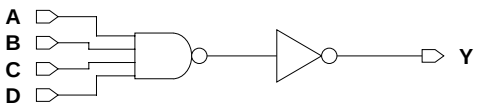
Functions

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AND4XL	5.0	4.0
AND4X1	5.0	4.0
AND4X2	5.0	4.0
AND4X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0184	0.0198	0.0340	0.0606
B	0.0208	0.0233	0.0388	0.0688
C	0.0242	0.0253	0.0433	0.0803
D	0.0266	0.0276	0.0480	0.0889

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0025	0.0023	0.0037	0.0068
B	0.0024	0.0021	0.0036	0.0069
C	0.0025	0.0022	0.0038	0.0075
D	0.0025	0.0023	0.0038	0.0082

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.102	0.120	0.097	0.087	6.272	4.540	2.284	1.122
A → Y↓	0.109	0.126	0.107	0.106	3.353	2.463	1.217	0.610
B → Y↑	0.114	0.131	0.108	0.097	6.273	4.538	2.284	1.122
B → Y↓	0.122	0.138	0.119	0.120	3.364	2.467	1.219	0.611
C → Y↑	0.121	0.138	0.114	0.104	6.271	4.541	2.284	1.121
C → Y↓	0.135	0.151	0.131	0.133	3.376	2.473	1.222	0.612
D → Y↑	0.125	0.142	0.117	0.108	6.272	4.538	2.284	1.122
D → Y↓	0.145	0.161	0.141	0.146	3.393	2.480	1.225	0.614

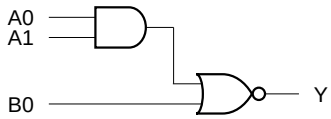
Delays at 25^{o}C, 1.8V, Typical Process

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0}$$

Logic Symbol



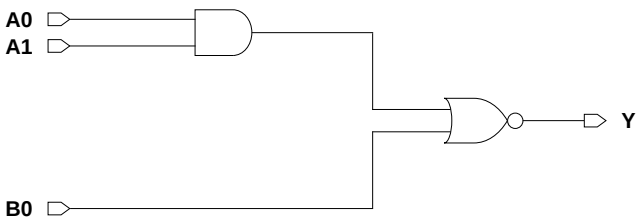
Functions

A0	A1	B0	Y
0	x	0	1
x	0	0	1
x	x	1	0
1	1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI21XL	5.0	2.6
AOI21X1	5.0	2.6
AOI21X2	5.0	4.6
AOI21X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0142	0.0196	0.0395	0.0737
A1	0.0182	0.0238	0.0505	0.0895
B0	0.0137	0.0185	0.0368	0.0679

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0032	0.0045	0.0094	0.0174
A1	0.0032	0.0044	0.0088	0.0174
B0	0.0032	0.0043	0.0083	0.0154

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.065	0.058	0.055	0.050	9.471	6.838	3.420	1.714
A0 → Y↓	0.032	0.029	0.028	0.026	3.945	2.729	1.365	0.684
A1 → Y↑	0.077	0.070	0.067	0.062	9.461	6.832	3.416	1.712
A1 → Y↓	0.037	0.034	0.032	0.030	3.947	2.730	1.365	0.684
B0 → Y↑	0.050	0.051	0.047	0.045	9.469	6.836	3.418	1.713
B0 → Y↓	0.020	0.020	0.018	0.017	3.248	2.405	1.196	0.602

Cell Description

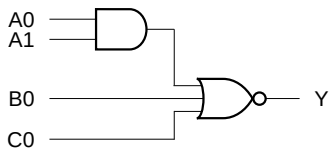
The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0 + C0}$$

Functions

A0	A1	B0	C0	Y
0	x	0	0	1
x	0	0	0	1
x	x	x	1	0
x	x	1	x	0
1	1	x	x	0

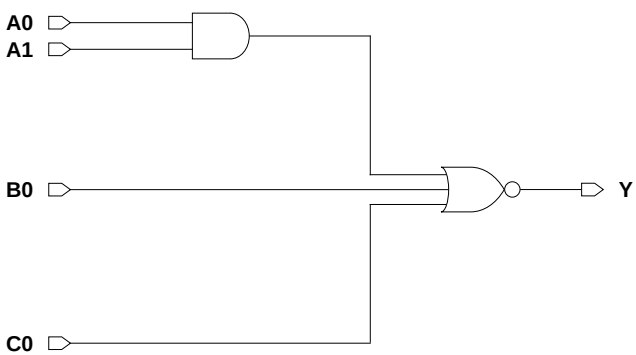
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI211XL	5.0	3.3
AOI211X1	5.0	3.3
AOI211X2	5.0	5.9
AOI211X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0225	0.0317	0.0629	0.0751
A1	0.0254	0.0358	0.0741	0.0823
B0	0.0165	0.0220	0.0451	0.0743
C0	0.0203	0.0276	0.0571	0.0779

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0036	0.0049	0.0098	0.0032
A1	0.0035	0.0048	0.0094	0.0032
B0	0.0034	0.0047	0.0089	0.0033
C0	0.0033	0.0045	0.0093	0.0031

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.104	0.098	0.094	0.262	12.248	8.497	4.269	1.109
A0 → Y↓	0.040	0.039	0.038	0.162	3.980	2.754	1.375	0.606
A1 → Y↑	0.121	0.113	0.110	0.281	12.234	8.491	4.265	1.109
A1 → Y↓	0.045	0.044	0.042	0.167	3.985	2.756	1.378	0.606
B0 → Y↑	0.077	0.071	0.067	0.237	12.249	8.496	4.269	1.109
B0 → Y↓	0.024	0.024	0.022	0.135	3.246	2.402	1.194	0.606
C0 → Y↑	0.101	0.095	0.093	0.262	12.237	8.495	4.267	1.109
C0 → Y↓	0.030	0.030	0.029	0.143	3.261	2.409	1.198	0.606

Cell Description

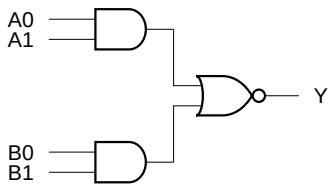
The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Functions

A0	A1	B0	B1	Y
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
x	x	1	1	0
1	1	x	x	0

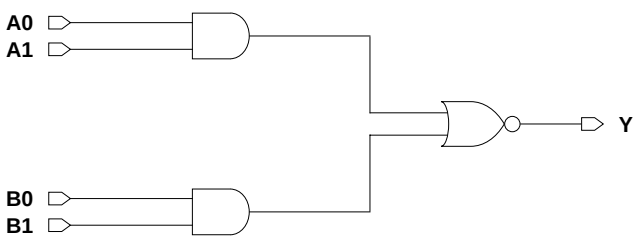
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI22XL	5.0	3.3
AOI22X1	5.0	3.3
AOI22X2	5.0	5.9
AOI22X4	5.0	9.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0155	0.0204	0.0406	0.0815
A1	0.0187	0.0255	0.0485	0.0975
B0	0.0207	0.0278	0.0543	0.1105
B1	0.0238	0.0324	0.0639	0.1269

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0035	0.0047	0.0091	0.0177
A1	0.0035	0.0046	0.0096	0.0181
B0	0.0033	0.0044	0.0088	0.0173
B1	0.0032	0.0044	0.0090	0.0174

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.058	0.055	0.055	0.055	9.473	6.726	3.419	1.697
A0 → Y↓	0.025	0.023	0.022	0.022	3.895	2.717	1.358	0.681
A1 → Y↑	0.072	0.068	0.068	0.065	9.466	6.722	3.417	1.648
A1 → Y↓	0.030	0.028	0.027	0.027	3.910	2.719	1.360	0.682
B0 → Y↑	0.090	0.085	0.079	0.074	9.469	6.725	3.418	1.648
B0 → Y↓	0.043	0.041	0.038	0.037	3.933	2.731	1.364	0.683
B1 → Y↑	0.102	0.097	0.092	0.086	9.458	6.720	3.417	1.647
B1 → Y↓	0.048	0.046	0.042	0.041	3.941	2.734	1.366	0.684

Cell Description

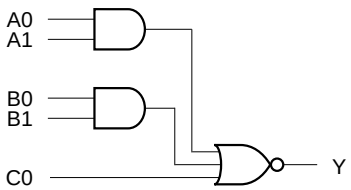
The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + C0}$$

Functions

A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	0	0	1
x	0	0	x	0	1
x	0	x	0	0	1
x	x	x	x	1	0
x	x	1	1	x	0
1	1	x	x	x	0

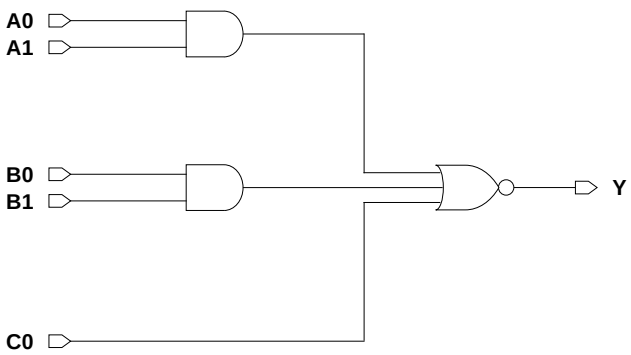
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI221XL	5.0	4.6
AOI221X1	5.0	4.6
AOI221X2	5.0	7.9
AOI221X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0228	0.0304	0.0577	0.0759
A1	0.0257	0.0350	0.0665	0.0806
B0	0.0291	0.0392	0.0754	0.0812
B1	0.0321	0.0429	0.0837	0.0854
C0	0.0204	0.0270	0.0510	0.0746

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0036	0.0050	0.0095	0.0034
A1	0.0036	0.0050	0.0098	0.0032
B0	0.0036	0.0049	0.0096	0.0033
B1	0.0036	0.0048	0.0097	0.0032
C0	0.0035	0.0048	0.0091	0.0032

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.127	0.113	0.104	0.284	12.018	8.621	4.311	1.138
A0 → Y↓	0.045	0.039	0.035	0.164	3.949	2.730	1.366	0.606
A1 → Y↑	0.144	0.128	0.119	0.302	12.004	8.614	4.307	1.139
A1 → Y↓	0.049	0.043	0.040	0.169	3.955	2.732	1.367	0.605
B0 → Y↑	0.149	0.130	0.121	0.306	12.019	8.623	4.311	1.138
B0 → Y↓	0.050	0.046	0.041	0.173	4.043	2.770	1.387	0.606
B1 → Y↑	0.164	0.145	0.137	0.324	12.004	8.614	4.308	1.139
B1 → Y↓	0.054	0.050	0.046	0.178	4.050	2.774	1.388	0.606
C0 → Y↑	0.082	0.085	0.075	0.241	12.012	8.620	4.309	1.139
C0 → Y↓	0.025	0.025	0.022	0.136	3.253	2.405	1.196	0.605

Cell Description

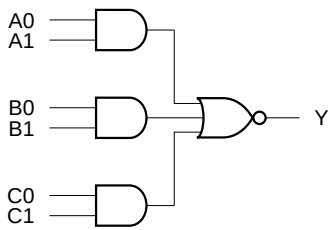
The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + (C0 \bullet C1)}$$

Functions

A0	A1	B0	B1	C0	C1	Y
0	x	0	x	0	x	1
0	x	0	x	x	0	1
0	x	x	0	0	x	1
0	x	x	0	x	0	1
x	0	0	x	0	x	1
x	0	0	x	x	0	1
x	0	x	0	0	x	1
x	0	x	0	x	0	1
x	x	x	x	1	1	0
x	x	1	1	x	x	0
1	1	x	x	x	x	0

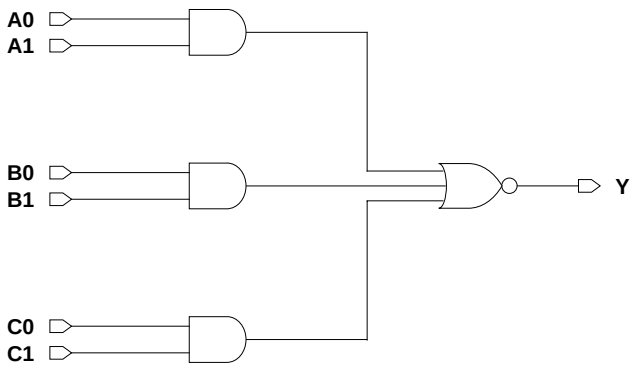
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI222XL	5.0	5.3
AOI222X1	5.0	5.3
AOI222X2	5.0	9.2
AOI222X4	5.0	7.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0242	0.0324	0.0575	0.0791
A1	0.0271	0.0366	0.0669	0.0814
B0	0.0303	0.0410	0.0758	0.0851
B1	0.0338	0.0455	0.0835	0.0888
C0	0.0364	0.0490	0.0922	0.0877
C1	0.0396	0.0533	0.1028	0.0918

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0051	0.0100	0.0034
A1	0.0037	0.0051	0.0103	0.0034
B0	0.0035	0.0050	0.0096	0.0032
B1	0.0035	0.0049	0.0098	0.0031
C0	0.0035	0.0049	0.0096	0.0032
C1	0.0034	0.0048	0.0097	0.0032

Delays at 25°C, 1.8V, Typical Process

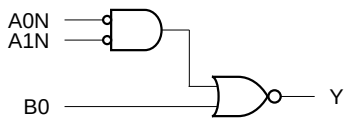
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.091	0.091	0.086	0.237	12.500	8.646	4.311	1.130
A0 → Y↓	0.032	0.030	0.028	0.155	3.906	2.715	1.358	0.610
A1 → Y↑	0.108	0.108	0.102	0.256	12.490	8.641	4.309	1.130
A1 → Y↓	0.037	0.035	0.033	0.159	3.921	2.724	1.361	0.610
B0 → Y↑	0.177	0.153	0.139	0.328	12.498	8.645	4.310	1.130
B0 → Y↓	0.057	0.049	0.045	0.181	3.948	2.729	1.364	0.610
B1 → Y↑	0.196	0.169	0.154	0.346	12.490	8.638	4.307	1.130
B1 → Y↓	0.063	0.054	0.050	0.187	3.956	2.733	1.366	0.610
C0 → Y↑	0.201	0.171	0.157	0.350	12.495	8.644	4.311	1.130
C0 → Y↓	0.068	0.061	0.057	0.194	4.030	2.766	1.383	0.610
C1 → Y↑	0.217	0.186	0.172	0.367	12.484	8.638	4.307	1.131
C1 → Y↓	0.074	0.067	0.063	0.200	4.024	2.765	1.382	0.610

Cell Description

The AOI2BB1 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + B0}$$

Logic Symbol



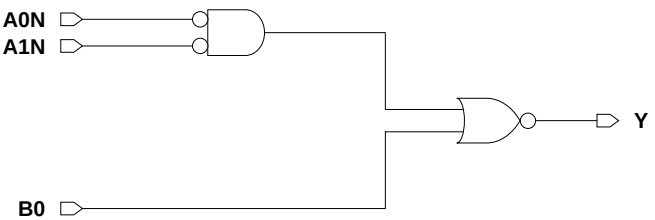
Functions

A0N	A1N	B0	Y
1	x	0	1
x	1	0	1
x	x	1	0
0	0	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI2BB1XL	5.0	3.3
AOI2BB1X1	5.0	3.3
AOI2BB1X2	5.0	4.6
AOI2BB1X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0195	0.0225	0.0343	0.0689
A1N	0.0212	0.0244	0.0401	0.0778
B0	0.0132	0.0175	0.0332	0.0664

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0025	0.0024	0.0042	0.0079
A1N	0.0022	0.0024	0.0043	0.0079
B0	0.0032	0.0041	0.0084	0.0156

Delays at 25°C, 1.8V, Typical Process

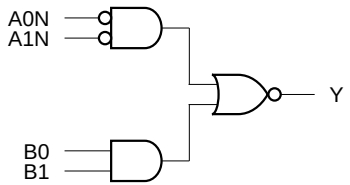
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.079	0.080	0.072	0.069	9.482	6.838	3.363	1.649
A0N → Y↓	0.135	0.154	0.130	0.126	3.187	2.566	1.229	0.613
A1N → Y↑	0.084	0.083	0.078	0.075	9.483	6.838	3.364	1.649
A1N → Y↓	0.145	0.166	0.141	0.135	3.188	2.566	1.229	0.613
B0 → Y↑	0.050	0.048	0.042	0.040	9.460	6.828	3.361	1.647
B0 → Y↓	0.021	0.023	0.020	0.020	3.041	2.494	1.199	0.600

Cell Description

The AOI2BB2 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and one AND group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + (B0 \bullet B1)}$$

Logic Symbol



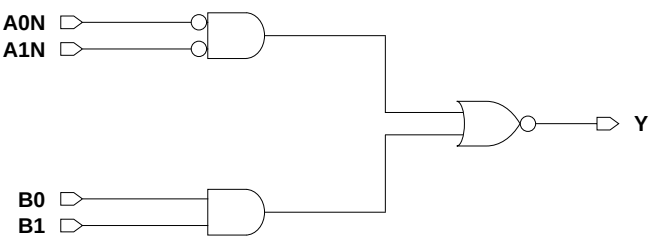
Functions

A0N	A1N	B0	B1	Y
1	x	0	x	1
1	x	x	0	1
x	1	0	x	1
x	1	x	0	1
x	x	1	1	0
0	0	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI2BB2XL	5.0	4.6
AOI2BB2X1	5.0	4.6
AOI2BB2X2	5.0	5.9
AOI2BB2X4	5.0	9.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0192	0.0205	0.0334	0.0643
A1N	0.0211	0.0225	0.0381	0.0736
B0	0.0154	0.0205	0.0413	0.0774
B1	0.0192	0.0249	0.0498	0.0934

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0025	0.0024	0.0043	0.0077
A1N	0.0023	0.0021	0.0041	0.0081
B0	0.0034	0.0046	0.0092	0.0171
B1	0.0033	0.0046	0.0098	0.0176

Delays at 25°C, 1.8V, Typical Process

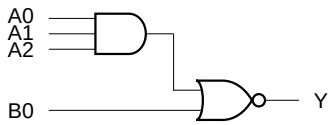
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.074	0.071	0.070	0.065	7.061	5.134	2.547	1.229
A0N → Y↓	0.143	0.148	0.133	0.120	3.410	2.475	1.268	0.610
A1N → Y↑	0.078	0.076	0.076	0.072	7.059	5.136	2.547	1.229
A1N → Y↓	0.152	0.157	0.142	0.130	3.410	2.475	1.267	0.610
B0 → Y↑	0.064	0.061	0.053	0.051	9.473	6.892	3.419	1.648
B0 → Y↓	0.032	0.030	0.026	0.026	3.933	2.729	1.363	0.684
B1 → Y↑	0.077	0.074	0.066	0.062	9.460	6.888	3.415	1.647
B1 → Y↓	0.037	0.034	0.031	0.031	3.935	2.731	1.364	0.684

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + B0}$$

Logic Symbol



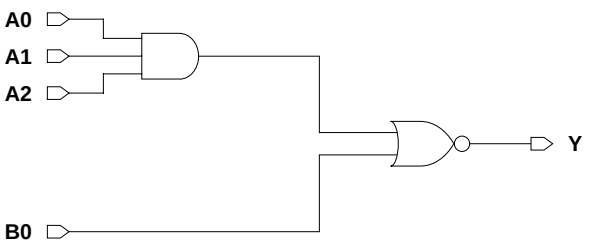
Functions

A0	A1	A2	B0	Y
0	x	x	0	1
x	0	x	0	1
x	x	0	0	1
x	x	x	1	0
1	1	1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI31XL	5.0	3.3
AOI31X1	5.0	3.3
AOI31X2	5.0	5.9
AOI31X4	5.0	5.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0162	0.0210	0.0478	0.0693
A1	0.0200	0.0269	0.0562	0.0740
A2	0.0236	0.0321	0.0654	0.0771
B0	0.0179	0.0247	0.0497	0.0704

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0035	0.0048	0.0107	0.0033
A1	0.0035	0.0048	0.0099	0.0032
A2	0.0034	0.0047	0.0095	0.0032
B0	0.0032	0.0044	0.0083	0.0031

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.066	0.063	0.064	0.199	9.474	6.727	3.421	1.109
A0 → Y↓	0.036	0.033	0.033	0.160	4.442	3.025	1.515	0.610
A1 → Y↑	0.082	0.079	0.079	0.216	9.466	6.723	3.418	1.109
A1 → Y↓	0.043	0.041	0.039	0.168	4.444	3.026	1.516	0.610
A2 → Y↑	0.096	0.092	0.093	0.232	9.468	6.723	3.419	1.109
A2 → Y↓	0.046	0.043	0.042	0.171	4.444	3.026	1.516	0.610
B0 → Y↑	0.071	0.071	0.066	0.209	9.475	6.729	3.421	1.108
B0 → Y↓	0.020	0.021	0.019	0.133	3.264	2.413	1.200	0.609

Cell Description

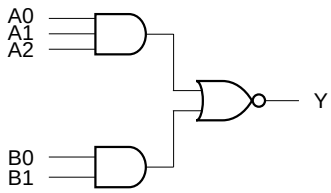
The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1)}$$

Functions

A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	x	0	1
x	0	x	0	x	1
x	0	x	x	0	1
x	x	0	0	x	1
x	x	0	x	0	1
x	x	x	1	1	0
1	1	1	x	x	0

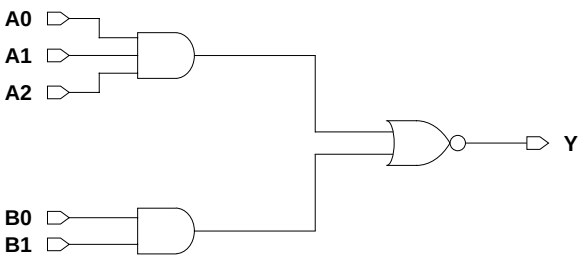
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI32XL	5.0	4.6
AOI32X1	5.0	4.6
AOI32X2	5.0	7.3
AOI32X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0227	0.0300	0.0594	0.0754
A1	0.0269	0.0349	0.0686	0.0797
A2	0.0294	0.0393	0.0784	0.0813
B0	0.0199	0.0272	0.0536	0.0710
B1	0.0240	0.0310	0.0613	0.0771

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0036	0.0048	0.0094	0.0033
A1	0.0036	0.0048	0.0098	0.0033
A2	0.0034	0.0047	0.0100	0.0032
B0	0.0035	0.0046	0.0092	0.0033
B1	0.0036	0.0047	0.0095	0.0032

Delays at 25°C, 1.8V, Typical Process

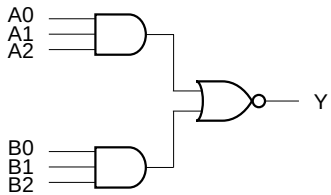
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.095	0.090	0.089	0.227	9.475	6.727	3.434	1.109
A0 → Y↓	0.050	0.046	0.045	0.174	4.443	3.026	1.513	0.606
A1 → Y↑	0.111	0.105	0.104	0.245	9.462	6.721	3.432	1.109
A1 → Y↓	0.058	0.053	0.052	0.183	4.450	3.030	1.515	0.606
A2 → Y↑	0.125	0.119	0.119	0.260	9.468	6.722	3.432	1.109
A2 → Y↓	0.061	0.056	0.055	0.186	4.451	3.030	1.515	0.606
B0 → Y↑	0.077	0.074	0.074	0.210	9.482	6.731	3.435	1.108
B0 → Y↓	0.026	0.024	0.023	0.149	3.912	2.725	1.363	0.606
B1 → Y↑	0.090	0.087	0.087	0.224	9.474	6.726	3.433	1.109
B1 → Y↓	0.031	0.029	0.028	0.152	3.928	2.729	1.364	0.606

Cell Description

The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1 \bullet B2)}$$

Logic Symbol



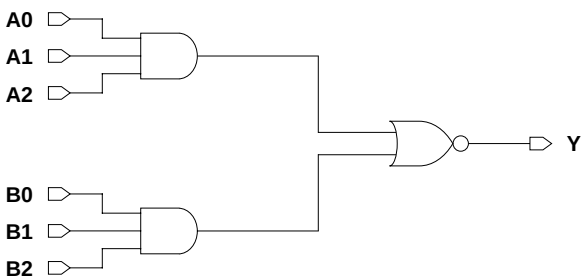
Functions

A0	A1	A2	B0	B1	B2	Y
0	x	x	0	x	x	1
0	x	x	x	0	x	1
0	x	x	x	x	0	1
x	0	x	0	x	x	1
x	0	x	x	0	x	1
x	0	x	x	x	0	1
x	x	0	0	x	x	1
x	x	0	x	0	x	1
x	x	0	x	x	0	1
x	x	x	1	1	1	0
1	1	1	x	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AOI33XL	5.0	5.3
AOI33X1	5.0	5.3
AOI33X2	5.0	8.6
AOI33X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0213	0.0305	0.0610	0.0746
A1	0.0254	0.0353	0.0701	0.0782
A2	0.0288	0.0398	0.0793	0.0833
B0	0.0284	0.0389	0.0784	0.0866
B1	0.0325	0.0445	0.0914	0.0880
B2	0.0361	0.0494	0.1016	0.0916

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0036	0.0049	0.0098	0.0033
A1	0.0036	0.0050	0.0103	0.0034
A2	0.0036	0.0050	0.0108	0.0036
B0	0.0034	0.0048	0.0092	0.0033
B1	0.0034	0.0047	0.0098	0.0033
B2	0.0034	0.0046	0.0102	0.0031

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.091	0.088	0.083	0.229	9.480	6.731	3.437	1.109
A0 → Y↓	0.034	0.032	0.029	0.172	4.422	3.018	1.542	0.610
A1 → Y↑	0.106	0.104	0.098	0.246	9.472	6.726	3.435	1.109
A1 → Y↓	0.042	0.039	0.036	0.178	4.434	3.024	1.545	0.610
A2 → Y↑	0.121	0.118	0.114	0.263	9.476	6.726	3.433	1.109
A2 → Y↓	0.045	0.042	0.040	0.182	4.435	3.024	1.544	0.610
B0 → Y↑	0.126	0.122	0.120	0.268	9.478	6.728	3.436	1.109
B0 → Y↓	0.062	0.059	0.059	0.196	4.442	3.023	1.545	0.610
B1 → Y↑	0.141	0.136	0.135	0.285	9.467	6.726	3.433	1.109
B1 → Y↓	0.071	0.066	0.066	0.204	4.442	3.027	1.547	0.610
B2 → Y↑	0.155	0.150	0.150	0.300	9.473	6.726	3.433	1.109
B2 → Y↓	0.074	0.069	0.070	0.207	4.442	3.027	1.547	0.610

Cell Description

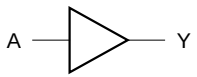
The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
BUFXL	5.0	2.6
BUFX1	5.0	2.6
BUFX2	5.0	2.6
BUFX3	5.0	2.6
BUFX4	5.0	3.3
BUFX8	5.0	5.9
BUFX12	5.0	6.6
BUFX16	5.0	8.6
BUFX20	5.0	10.6

Functional Schematic

AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0146	0.0168	0.0283	0.0374	0.0481	0.0920	0.1401	0.1845	0.2186

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0021	0.0021	0.0032	0.0043	0.0056	0.0107	0.0160	0.0211	0.0265

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.052	0.055	0.058	0.056	0.053	0.049	0.050	0.050	0.049
A → Y↓	0.074	0.084	0.083	0.082	0.077	0.074	0.074	0.073	0.071

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6.232	4.514	2.248	1.497	1.124	0.554	0.370	0.277	0.222
A → Y↓	3.294	2.430	1.209	0.809	0.605	0.304	0.203	0.151	0.122

Cell Description

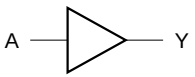
The CLKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = A$$

Functions

A	Y
0	0
1	1

Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
CLKBUFXL	5.0	2.6
CLKBUFX1	5.0	2.6
CLKBUFX2	5.0	2.6
CLKBUFX3	5.0	2.6
CLKBUFX4	5.0	3.3
CLKBUFX8	5.0	4.6
CLKBUFX12	5.0	10.6
CLKBUFX16	5.0	12.5
CLKBUFX20	5.0	15.8

Functional Schematic

AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0159	0.0201	0.0246	0.0298	0.0377	0.0754	0.1778	0.2394	0.2860

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0019	0.0033	0.0029	0.0032	0.0040	0.0078	0.0189	0.0225	0.0311

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.050	0.056	0.064	0.071	0.073	0.067	0.065	0.069	0.064
A → Y↓	0.106	0.059	0.079	0.086	0.084	0.079	0.075	0.078	0.073

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	4.083	4.160	2.247	1.549	1.125	0.555	0.222	0.171	0.139
A → Y↓	4.225	4.176	2.260	1.403	1.065	0.502	0.203	0.156	0.121

Cell Description

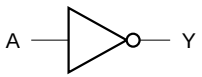
The CLKINV cell provides the logical inversion of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = \overline{A}$$

Functions

A	Y
0	1
1	0

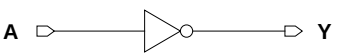
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
CLKINVXL	5.0	2.0
CLKINVX1	5.0	2.0
CLKINVX2	5.0	2.0
CLKINVX3	5.0	2.0
CLKINVX4	5.0	2.6
CLKINVX8	5.04	3.96
CLKINVX12	5.04	12.54
CLKINVX16	5.04	16.50
CLKINVX20	5.04	19.14

Functional Schematic



AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0088	0.0104	0.0183	0.0264	0.0322	0.0695	0.2398	0.3204	0.3952

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0026	0.0031	0.0058	0.0084	0.0108	0.0228	0.0069	0.0087	0.0107

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.024	0.022	0.017	0.016	0.015	0.017	0.144	0.142	0.139
A → Y↓	0.020	0.019	0.017	0.015	0.015	0.017	0.137	0.148	0.143

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	5.723	4.509	2.254	1.504	1.116	0.518	0.209	0.157	0.126
A → Y↓	4.367	3.649	2.251	1.394	1.059	0.627	0.240	0.180	0.144

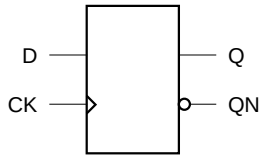
Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

Function Table

D	CK	Q[n+1]	QN[n+1]
0	⎍	0	1
1	⎍	1	0
x	⎎	Q[n]	QN[n]

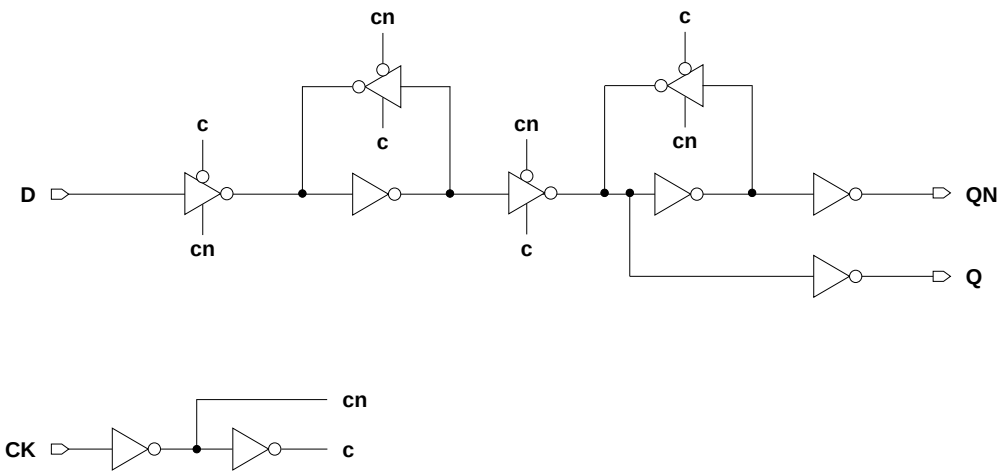
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFXL	5.0	11.2
DFFX1	5.0	11.2
DFFX2	5.0	13.9
DFFX4	5.0	16.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0306	0.0276	0.0368	0.0606
CK	0.0335	0.0318	0.0396	0.0579
Q	0.0260	0.0346	0.0614	0.1091

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0033	0.0020	0.0024	0.0038
CK	0.0020	0.0026	0.0038	0.0059

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.219	0.197	0.180	0.155	5.696	4.288	2.261	1.139
CK → Q↓	0.179	0.166	0.153	0.132	3.406	2.469	1.234	0.611
CK → QN↑	0.238	0.221	0.196	0.179	6.239	4.518	2.259	1.138
CK → QN↓	0.304	0.280	0.251	0.219	3.342	2.444	1.219	0.605

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.04	0.06	0.06	0.06
	setup↓ → CK	0.10	0.15	0.15	0.14
	hold↑ → CK	-0.02	-0.04	-0.04	-0.03
	hold↓ → CK	0.01	-0.04	-0.04	-0.04
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25

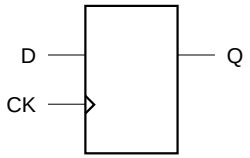
Cell Description

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Functions

D	CK	Q[n+1]
0	⎍	0
1	⎍	1
x	⎎	Q[n]

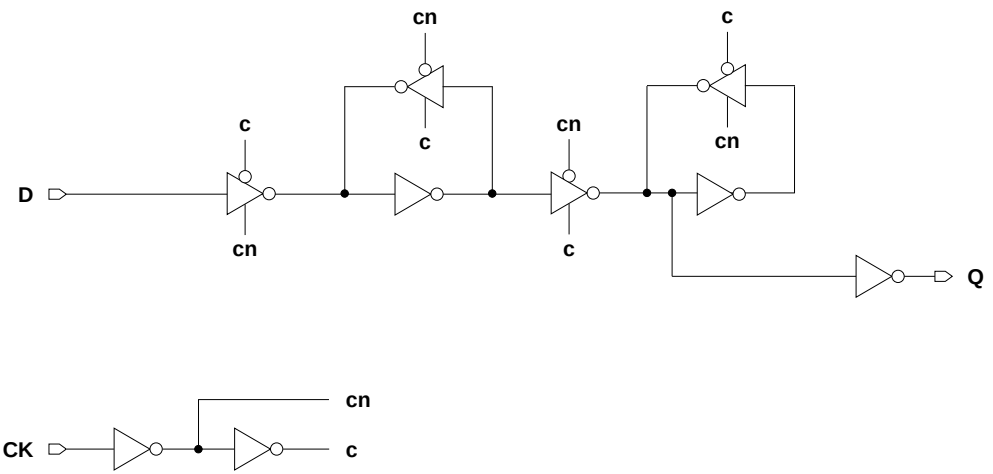
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFHQXL	5.0	10.6
DFFHQX1	5.0	10.6
DFFHQX2	5.0	13.2
DFFHQX4	5.0	14.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0354	0.0355	0.0514	0.0669
CK	0.0346	0.0328	0.0388	0.0496
Q	0.0133	0.0176	0.0285	0.0422

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0035	0.0022	0.0022	0.0031
CK	0.0022	0.0029	0.0036	0.0052

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.204	0.170	0.166	0.144	6.246	4.283	2.261	1.118
CK → Q↓	0.206	0.161	0.156	0.133	3.517	2.593	1.297	0.611

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.05	0.08	0.09	0.08
	setup↓ → CK	0.14	0.18	0.20	0.18
	hold↑ → CK	-0.02	-0.04	-0.04	-0.04
	hold↓ → CK	0.01	-0.04	-0.05	-0.04
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25

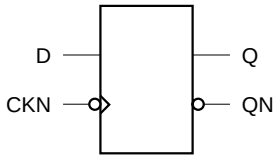
Cell Description

The DFFN cell is a negative-edge triggered, static D-type flip-flop.

Function

D	CKN	Q[n+1]	QN[n+1]
0	↓	0	1
1	↓	1	0
x	↑	Q[n]	QN[n]

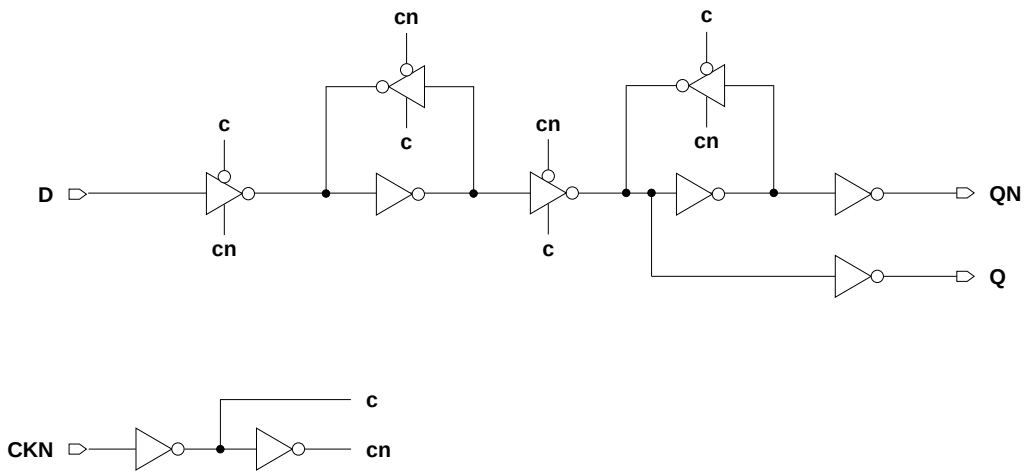
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNXL	5.0	11.2
DFFNX1	5.0	11.2
DFFNX2	5.0	13.9
DFFNX4	5.0	15.8

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0319	0.0285	0.0370	0.0565
CKN	0.0314	0.0347	0.0487	0.0739
Q	0.0370	0.0420	0.0695	0.1176

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0029	0.0018	0.0022	0.0028
CKN	0.0021	0.0028	0.0037	0.0061

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.183	0.143	0.128	0.108	5.709	4.289	2.263	1.190
CKN → Q↓	0.305	0.261	0.240	0.202	3.420	2.552	1.276	0.621
CKN → QN↑	0.358	0.315	0.283	0.253	6.243	4.519	2.259	1.189
CKN → QN↓	0.263	0.226	0.199	0.176	3.334	2.444	1.219	0.615

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.05	0.08	0.09	0.09
	setup↓ → CKN	0.07	0.12	0.12	0.12
	hold↑ → CKN	0.08	0.04	0.04	0.02
	hold↓ → CKN	-0.05	-0.09	-0.09	-0.09
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25

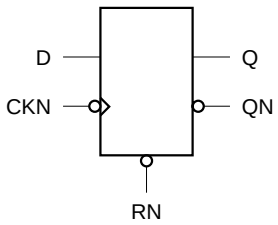
Cell Description

The DFFNR cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Function

RN	D	CKN	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	↓	0	1
1	1	↓	1	0
1	x	↑	Q[n]	QN[n]

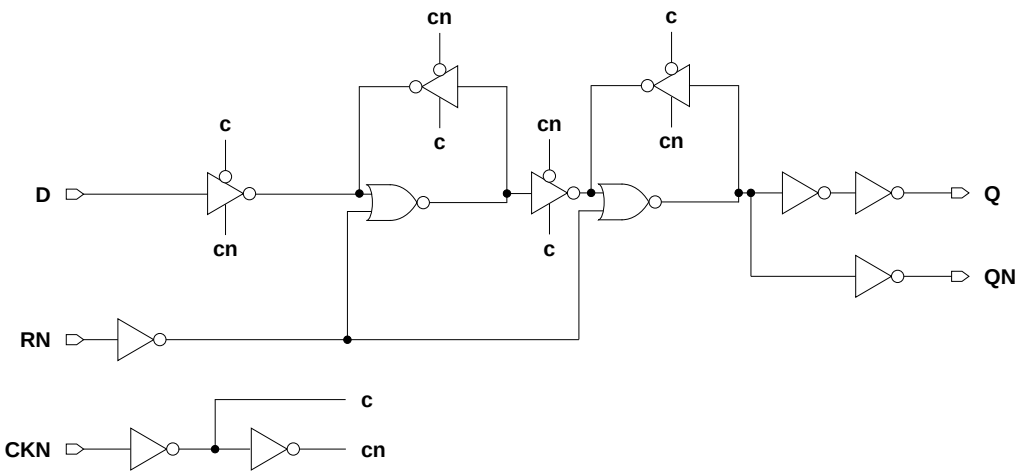
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNRXL	5.0	15.8
DFFNRX1	5.0	15.2
DFFNRX2	5.04	17.16
DFFNRX4	5.0	20.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0334	0.0265	0.0342	0.0414
CKN	0.0360	0.0343	0.0444	0.0523
RN	0.0164	0.0182	0.0216	0.0328
Q	0.0445	0.0517	0.0810	0.1344

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0033	0.0020	0.0021	0.0027
CKN	0.0023	0.0028	0.0030	0.0038
RN	0.0021	0.0026	0.0033	0.0055

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.360	0.319	0.323	0.281	6.237	4.515	2.077	1.137
CKN → Q↓	0.418	0.413	0.435	0.368	3.301	2.433	1.442	0.615
RN → Q↓	0.238	0.242	0.240	0.208	3.301	2.434	1.442	0.615
CKN → QN↑	0.368	0.349	0.357	0.300	6.239	4.517	2.079	1.138
CKN → QN↓	0.332	0.284	0.275	0.230	3.519	2.491	1.463	0.625
RN → QN↑	0.187	0.178	0.162	0.141	6.245	4.518	2.080	1.139

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.05	0.08	0.11	0.10
	setup↓ → CKN	0.06	0.13	0.15	0.12
	hold↑ → CKN	0.09	0.04	0.04	0.04
	hold↓ → CKN	-0.04	-0.09	-0.09	-0.08
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.05	0.08	0.10	0.09

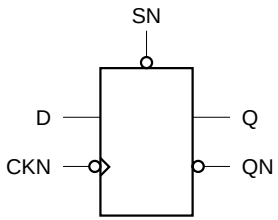
Cell Description

The DFFNS cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Function

SN	D	CKN	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	↓	0	1
1	1	↓	1	0
1	x	↑	Q[n]	QN[n]

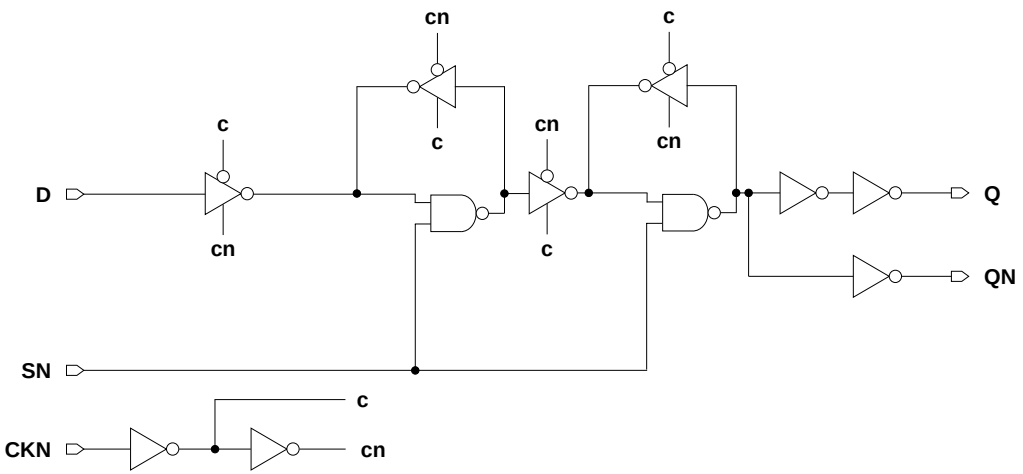
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNSXL	5.0	13.9
DFFNSX1	5.0	13.9
DFFNSX2	5.0	13.9
DFFNSX4	5.0	19.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0315	0.0243	0.0282	0.0359
CKN	0.0338	0.0324	0.0359	0.0461
SN	0.0050	0.0059	0.0092	0.0166
Q	0.0422	0.0501	0.0812	0.1325

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0028	0.0017	0.0017	0.0020
CKN	0.0020	0.0025	0.0028	0.0033
SN	0.0047	0.0052	0.0069	0.0117

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.289	0.266	0.266	0.253	6.240	4.516	2.277	1.137
CKN → Q↓	0.397	0.389	0.376	0.362	3.298	2.430	1.211	0.606
SN → Q↑	0.157	0.146	0.152	0.142	6.240	4.518	2.276	1.137
CKN → QN↑	0.350	0.328	0.307	0.295	6.255	4.522	2.280	1.139
CKN → QN↓	0.260	0.230	0.216	0.204	3.363	2.441	1.214	0.608
SN → QN↓	0.127	0.110	0.101	0.093	3.343	2.439	1.216	0.610

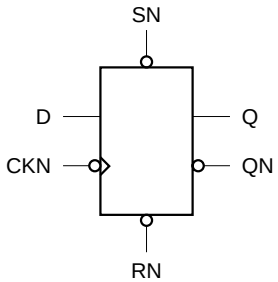
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.03	0.06	0.06	0.07
	setup↓ → CKN	0.07	0.12	0.13	0.12
	hold↑ → CKN	0.08	0.04	0.04	0.04
	hold↓ → CKN	-0.05	-0.09	-0.10	-0.10
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.09	-0.05	-0.04	-0.04

Cell Description

The DFFNSR cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Logic Symbol



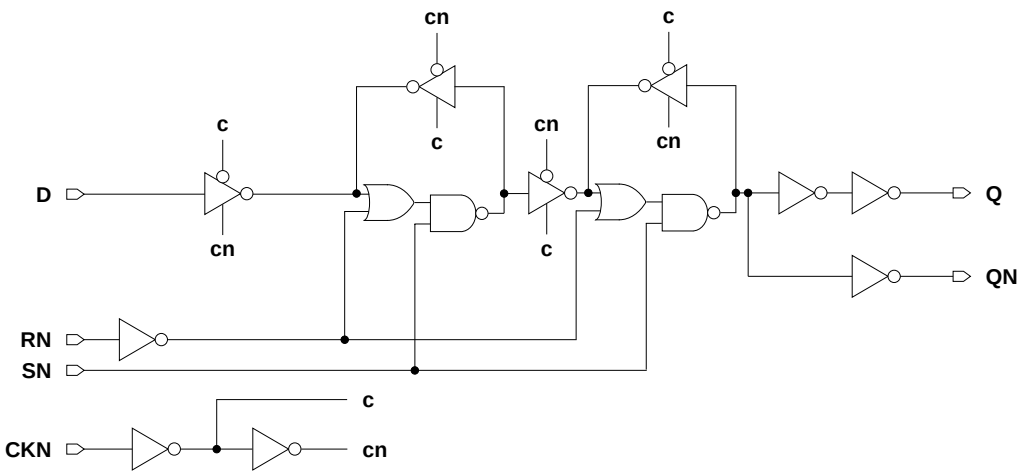
Functions

RN	SN	D	CKN	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	↓	0	1
1	1	1	↓	1	0
1	1	x	↑	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFNSRXL	5.0	17.2
DFFNSRX1	5.0	16.5
DFFNSRX2	5.0	17.2
DFFNSRX4	5.0	23.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0390	0.0318	0.0360	0.0500
CKN	0.0344	0.0342	0.0392	0.0551
SN	0.0051	0.0056	0.0092	0.0170
RN	0.0182	0.0197	0.0234	0.0397
Q	0.0453	0.0539	0.0814	0.1465

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0031	0.0019	0.0018	0.0030
CKN	0.0019	0.0027	0.0027	0.0039
SN	0.0061	0.0065	0.0088	0.0149
RN	0.0022	0.0025	0.0035	0.0057

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.364	0.328	0.310	0.292	6.238	4.515	2.276	1.137
CKN → Q↓	0.428	0.422	0.392	0.371	3.093	2.436	1.212	0.610
SN → Q↑	0.183	0.171	0.167	0.156	6.237	4.515	2.276	1.137
SN → Q↓	0.186	0.178	0.161	0.155	3.093	2.436	1.211	0.610
RN → Q↓	0.271	0.265	0.232	0.222	3.094	2.436	1.211	0.610
CKN → QN↑	0.369	0.352	0.323	0.303	6.260	4.522	2.279	1.140
CKN → QN↓	0.329	0.290	0.256	0.244	3.581	2.501	1.234	0.624
SN → QN↑	0.127	0.109	0.093	0.088	6.278	4.533	2.284	1.142
SN → QN↓	0.145	0.130	0.113	0.109	3.387	2.455	1.221	0.619
RN → QN↑	0.212	0.196	0.164	0.154	6.279	4.531	2.284	1.142

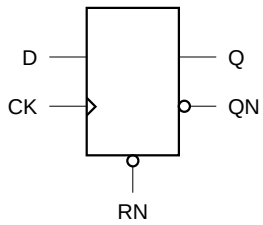
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CKN	0.08	0.15	0.13	0.11
	setup↓ → CKN	0.10	0.17	0.18	0.14
	hold↑ → CKN	0.06	0.02	0.02	0.03
	hold↓ → CKN	-0.07	-0.11	-0.13	-0.09
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.07	-0.04	-0.04	-0.04
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.07	0.12	0.10	0.09

Cell Description

The DFFR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Logic Symbol



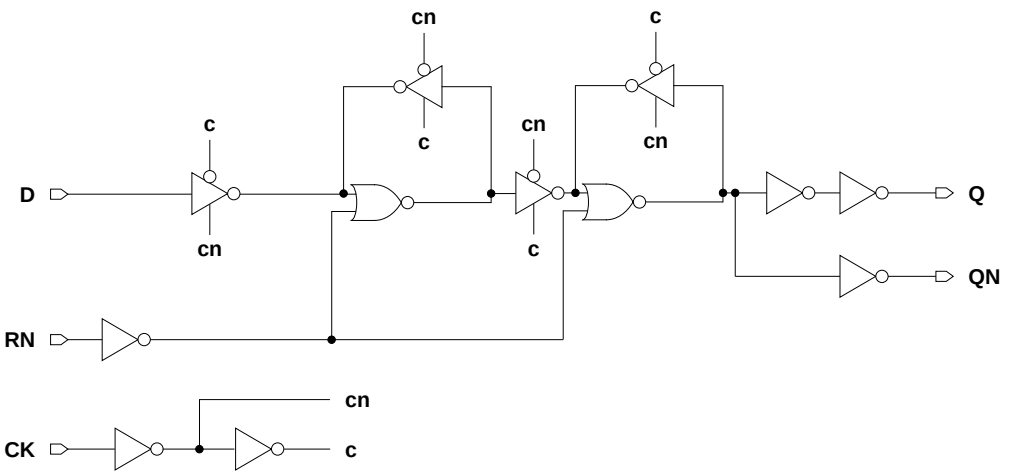
Functions

RN	D	CK	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	↑	0	1
1	1	↑	1	0
1	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFRXL	5.0	15.2
DFFRX1	5.0	15.2
DFFRX2	5.04	17.16
DFFRX4	5.0	19.8

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0326	0.0276	0.0331	0.0417
CK	0.0365	0.0349	0.0395	0.0444
RN	0.0162	0.0183	0.0213	0.0321
Q	0.0347	0.0403	0.0817	0.1302

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0032	0.0021	0.0021	0.0027
CK	0.0021	0.0028	0.0030	0.0038
RN	0.0020	0.0026	0.0033	0.0055

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.406	0.379	0.390	0.335	6.238	4.515	2.077	1.137
CK → Q↓	0.283	0.312	0.307	0.271	3.300	2.434	1.387	0.615
RN → Q↓	0.237	0.242	0.239	0.208	3.301	2.434	1.386	0.615
CK → QN↑	0.232	0.247	0.230	0.202	6.240	4.519	2.078	1.138
CK → QN↓	0.378	0.344	0.341	0.284	3.519	2.492	1.408	0.625
RN → QN↑	0.186	0.179	0.163	0.140	6.244	4.518	2.079	1.139

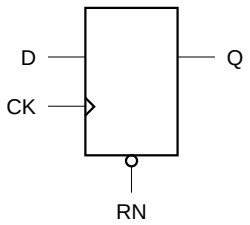
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.05	0.07	0.09	0.07
	setup↓ → CK	0.09	0.14	0.17	0.14
	hold↑ → CK	-0.03	-0.05	-0.06	-0.05
	hold↓ → CK	0.02	-0.04	-0.05	-0.03
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.04	0.05	0.08	0.05

Cell Description

The DFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



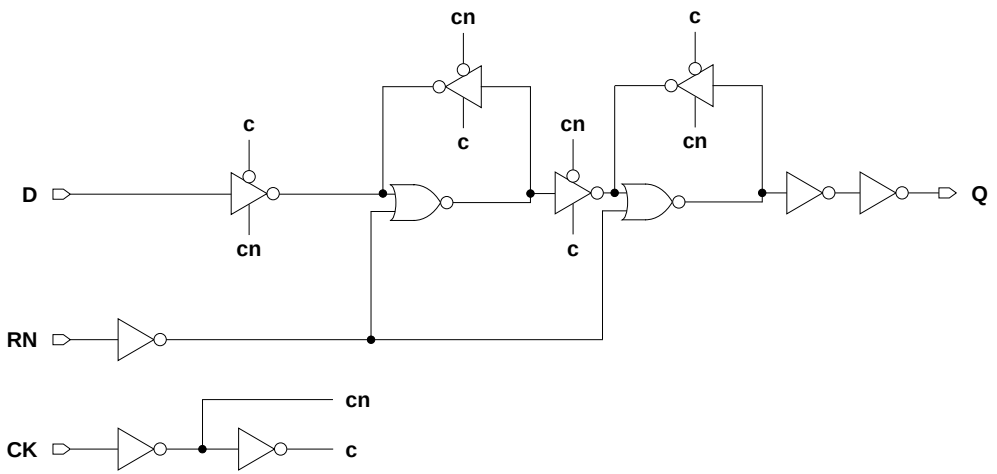
Functions

RN	D	CK	Q[n+1]
0	x	x	0
1	0	↑	0
1	1	↑	1
1	x	↓	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFRHQXL	5.0	13.9
DFFRHQX1	5.0	13.9
DFFRHQX2	5.0	17.2
DFFRHQX4	5.0	21.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0332	0.0381	0.0586	0.0913
CK	0.0337	0.0340	0.0432	0.0615
RN	0.0210	0.0252	0.0354	0.0548
Q	0.0218	0.0266	0.0374	0.0592

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0032	0.0019	0.0026	0.0043
CK	0.0020	0.0030	0.0041	0.0062
RN	0.0024	0.0039	0.0054	0.0093

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.233	0.192	0.168	0.155	9.482	6.727	3.364	1.832
CK → Q↓	0.247	0.173	0.150	0.137	3.620	2.468	1.225	0.676
RN → Q↓	0.171	0.137	0.117	0.097	2.887	1.947	1.081	0.645

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.07	0.12	0.12	0.11
	setup↓ → CK	0.14	0.20	0.20	0.18
	hold↑ → CK	-0.02	-0.05	-0.05	-0.04
	hold↓ → CK	0.02	-0.03	-0.02	-0.02
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.09	0.11	0.12	0.10

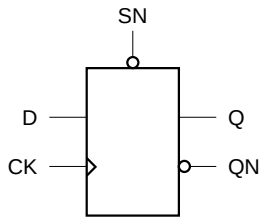
Cell Description

The DFFS cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Functions

SN	D	CK	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	↑	0	1
1	1	↑	1	0
1	x	↓	Q[n]	QN[n]

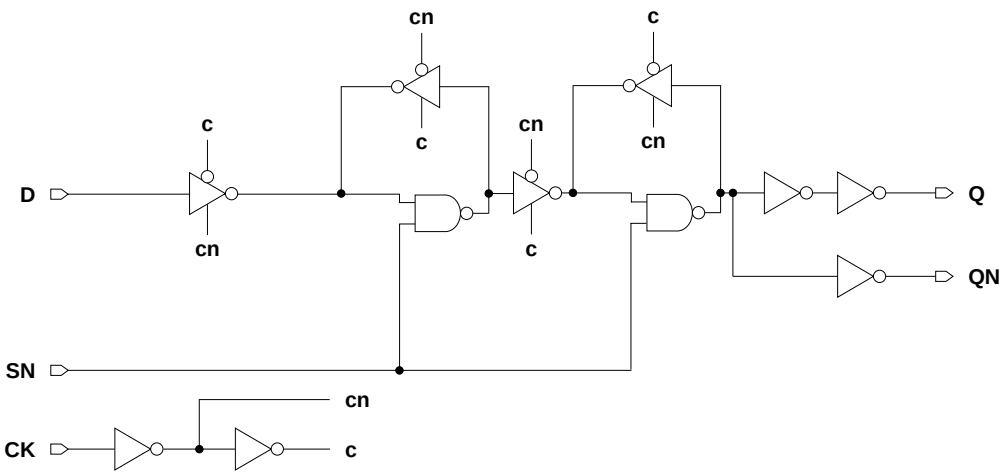
Logic Symbol



Cell Size

Drive Strength	Height (μm)	Width (μm)
DFFSXL	5.0	12.5
DFFSX1	5.0	12.5
DFFSX2	5.0	13.9
DFFSX4	5.0	18.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0311	0.0242	0.0275	0.0340
CK	0.0318	0.0293	0.0307	0.0380
SN	0.0053	0.0060	0.0102	0.0168
Q	0.0335	0.0385	0.0706	0.1293

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0032	0.0019	0.0019	0.0022
CK	0.0021	0.0027	0.0028	0.0034
SN	0.0050	0.0054	0.0073	0.0121

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.333	0.307	0.322	0.304	6.241	4.518	2.194	1.097
CK → Q↓	0.274	0.284	0.287	0.266	3.301	2.432	1.210	0.606
SN → Q↑	0.156	0.141	0.153	0.142	6.243	4.516	2.193	1.097
CK → QN↑	0.227	0.226	0.216	0.198	6.254	4.718	2.197	1.099
CK → QN↓	0.304	0.274	0.271	0.256	3.364	2.611	1.214	0.608
SN → QN↓	0.127	0.108	0.103	0.094	3.345	2.609	1.217	0.610

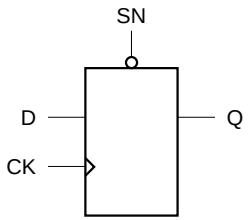
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.04	0.05	0.05	0.05
	setup↓ → CK	0.09	0.14	0.15	0.14
	hold↑ → CK	-0.02	-0.04	-0.04	-0.04
	hold↓ → CK	0.00	-0.05	-0.05	-0.04
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.02	-0.01	0.00	0.00

Cell Description

The DFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



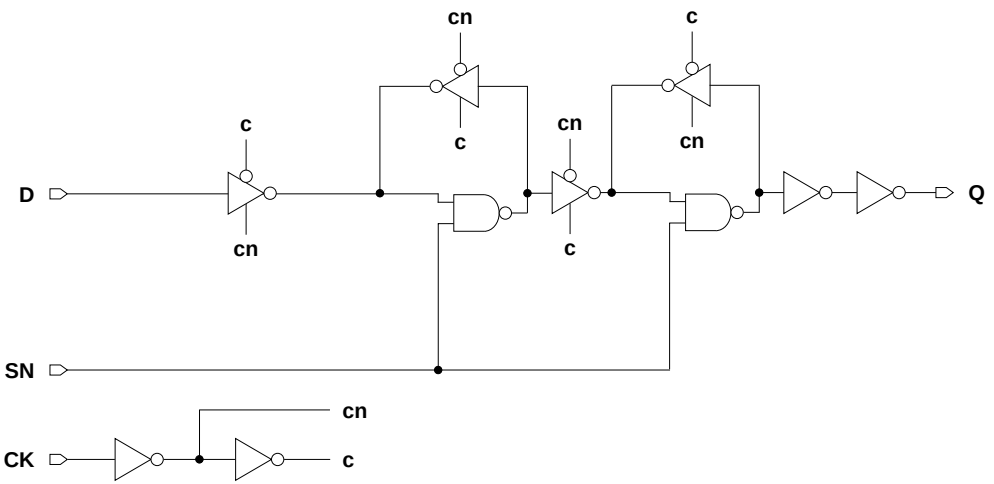
Functions

SN	D	CK	Q[n+1]
0	x	x	1
1	0	↑	0
1	1	↑	1
1	x	↓	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFSHQXL	5.0	13.2
DFFSHQX1	5.0	13.2
DFFSHQX2	5.0	15.8
DFFSHQX4	5.0	18.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0352	0.0378	0.0538	0.0822
CK	0.0333	0.0335	0.0393	0.0590
SN	0.0091	0.0102	0.0173	0.0315
Q	0.0214	0.0238	0.0333	0.0560

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0033	0.0019	0.0025	0.0037
CK	0.0021	0.0028	0.0037	0.0055
SN	0.0079	0.0085	0.0135	0.0214

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.224	0.191	0.171	0.154	6.271	4.522	2.251	1.125
CK → Q↓	0.237	0.171	0.148	0.135	4.218	2.773	1.383	0.690
SN → Q↑	0.072	0.081	0.082	0.087	3.455	2.426	1.251	0.665

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.05	0.09	0.09	0.09
	setup↓ → CK	0.16	0.23	0.21	0.19
	hold↑ → CK	-0.02	-0.05	-0.04	-0.04
	hold↓ → CK	0.00	-0.07	-0.05	-0.04
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.05	0.05	0.07	0.06

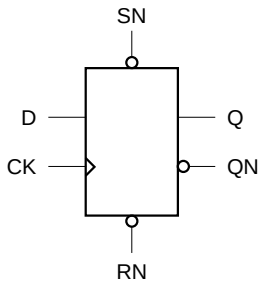
Cell Description

The DFFSR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Functions

RN	SN	D	CK	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	x	↓	Q[n]	QN[n]

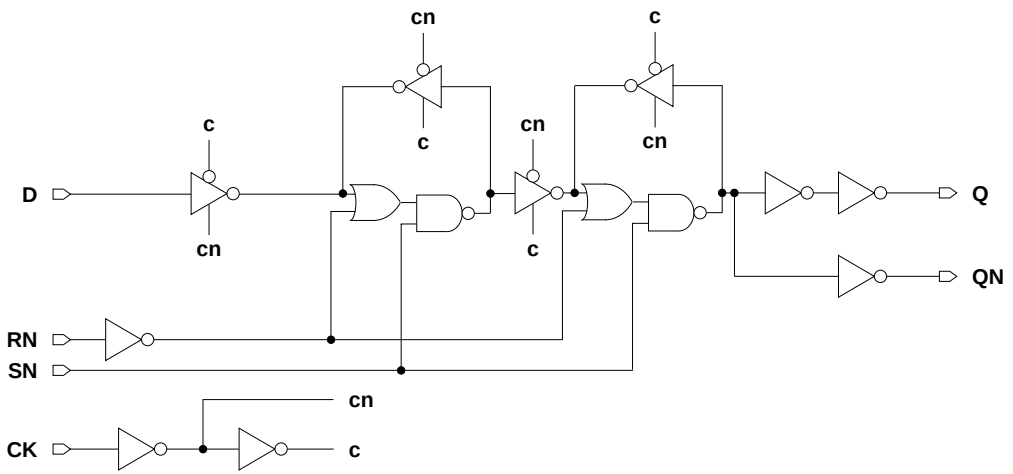
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFSRXL	5.0	17.2
DFFSRX1	5.0	17.2
DFFSRX2	5.0	17.2
DFFSRX4	5.0	23.8

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0378	0.0309	0.0353	0.0497
CK	0.0362	0.0336	0.0356	0.0466
SN	0.0058	0.0062	0.0098	0.0177
RN	0.0174	0.0192	0.0231	0.0396
Q	0.0339	0.0432	0.0756	0.1400

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0030	0.0019	0.0019	0.0030
CK	0.0024	0.0029	0.0030	0.0039
SN	0.0060	0.0065	0.0087	0.0149
RN	0.0022	0.0024	0.0036	0.0059

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.401	0.370	0.354	0.339	6.236	4.515	2.276	1.137
CK → Q↓	0.307	0.319	0.288	0.276	3.310	2.436	1.211	0.610
SN → Q↑	0.181	0.171	0.167	0.156	6.233	4.515	2.276	1.137
SN → Q↓	0.184	0.179	0.161	0.155	3.311	2.437	1.211	0.610
RN → Q↓	0.276	0.263	0.232	0.222	3.311	2.437	1.211	0.610
CK → QN↑	0.248	0.248	0.218	0.207	6.258	4.525	2.279	1.139
CK → QN↓	0.368	0.332	0.299	0.291	3.576	2.501	1.233	0.624
SN → QN↑	0.126	0.108	0.092	0.088	6.278	4.531	2.285	1.142
SN → QN↓	0.144	0.130	0.112	0.109	3.386	2.455	1.221	0.619
RN → QN↑	0.218	0.192	0.163	0.155	6.275	4.532	2.284	1.142

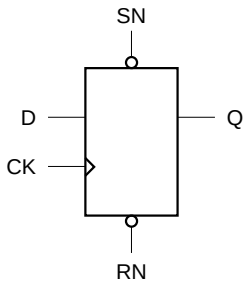
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.08	0.13	0.12	0.09
	setup↓ → CK	0.12	0.18	0.20	0.16
	hold↑ → CK	-0.05	-0.09	-0.08	-0.05
	hold↓ → CK	-0.01	-0.05	-0.06	-0.04
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.01	0.01	0.02	0.01
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.06	0.11	0.09	0.07

Cell Description

The DFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



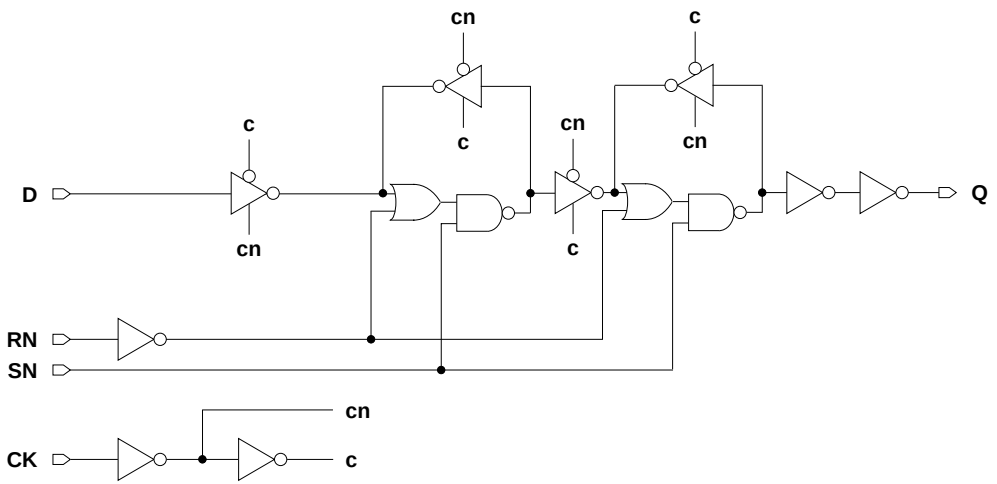
Functions

RN	SN	D	CK	Q[n+1]
0	1	x	x	0
1	0	x	x	1
0	0	x	x	1
1	1	0	↑	0
1	1	1	↑	1
1	1	x	↓	Q[n]

Cell Size

Drive Strength	Height (μm)	Width (μm)
DFFSRHQXL	5.0	15.8
DFFSRHQX1	5.0	15.8
DFFSRHQX2	5.0	22.4
DFFSRHQX4	5.0	30.4

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0358	0.0401	0.0657	0.1125
CK	0.0352	0.0343	0.0456	0.0669
SN	0.0093	0.0104	0.0172	0.0316
RN	0.0246	0.0278	0.0421	0.0675
Q	0.0234	0.0257	0.0434	0.0734

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0034	0.0023	0.0031	0.0049
CK	0.0021	0.0031	0.0045	0.0065
SN	0.0105	0.0115	0.0167	0.0276
RN	0.0025	0.0038	0.0058	0.0101

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.240	0.198	0.184	0.169	9.490	6.732	3.366	1.683
CK → Q↓	0.241	0.165	0.154	0.141	4.187	2.761	1.396	0.694
SN → Q↑	0.077	0.083	0.088	0.091	4.001	2.834	1.452	0.773
SN → Q↓	0.050	0.052	0.046	0.038	3.731	2.480	1.332	0.692
RN → Q↓	0.178	0.131	0.113	0.099	3.768	2.481	1.332	0.692

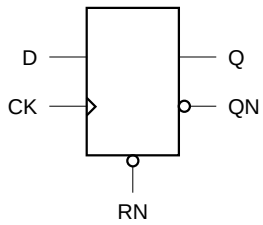
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.09	0.12	0.13	0.12
	setup↓ → CK	0.16	0.20	0.20	0.20
	hold↑ → CK	-0.02	-0.05	-0.05	-0.03
	hold↓ → CK	0.02	-0.02	-0.02	-0.02
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.06	0.06	0.08	0.09
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.10	0.12	0.12	0.12

Cell Description

The DFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-low reset (RN).

Logic Symbol



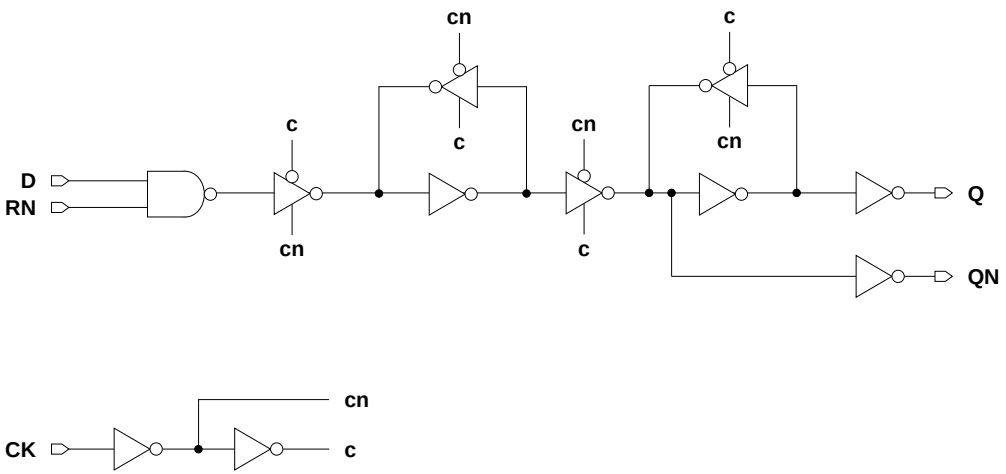
Functions

RN	D	CK	Q[n+1]	QN[n+1]
0	x	↑	0	1
x	x	↓	Q[n]	QN[n]
1	0	↑	0	1
1	1	↑	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
DFFTRXL	5.0	11.2
DFFTRX1	5.0	11.2
DFFTRX2	5.0	13.9
DFFTRX4	5.0	16.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0300	0.0286	0.0351	0.0575
CK	0.0332	0.0340	0.0406	0.0578
RN	0.0325	0.0303	0.0373	0.0593
Q	0.0237	0.0293	0.0606	0.1067

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0029	0.0022	0.0021	0.0032
CK	0.0021	0.0029	0.0040	0.0062
RN	0.0025	0.0019	0.0019	0.0028

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.217	0.198	0.193	0.156	6.245	4.520	2.250	1.125
CK → Q↓	0.174	0.159	0.147	0.133	3.396	2.461	1.226	0.612
CK → QN↑	0.218	0.206	0.204	0.181	6.246	4.519	2.249	1.124
CK → QN↓	0.285	0.270	0.269	0.223	3.330	2.440	1.213	0.606

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.08	0.09	0.10	0.09
	setup↓ → CK	0.14	0.22	0.22	0.19
	hold↑ → CK	-0.05	-0.07	-0.07	-0.06
	hold↓ → CK	-0.05	-0.12	-0.11	-0.09
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	setup↑ → CK	0.08	0.09	0.10	0.10
	setup↓ → CK	0.16	0.23	0.23	0.20
	hold↑ → CK	-0.06	-0.07	-0.08	-0.07
	hold↓ → CK	-0.05	-0.12	-0.12	-0.09

Cell Description

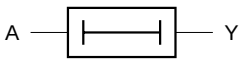
The DLY1 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY1X1	5.0	4.0

Functional Schematic

AC Power

Pin	Power (µW/MHz)
	X1
A	0.0304

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0018

Delays at 25°C, 1.8V, Typical Process

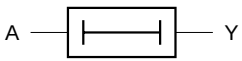
Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.135	4.518
A → Y↓	0.162	2.435

Cell Description

The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



Functions

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY2X1	5.0	4.0

Functional Schematic

AC Power

Pin	Power (µW/MHz)
	X1
A	0.0347

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0018

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.283	4.527
A → Y↓	0.311	2.515

Cell Description

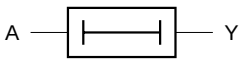
The DLY3 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Functions

A	Y
0	0
1	1

Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY3X1	5.0	4.6

Functional Schematic

AC Power

Pin	Power (µW/MHz)
	X1
A	0.0416

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0018

Delays at 25°C, 1.8V, Typical Process

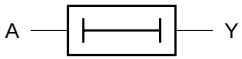
Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.476	4.541
A → Y↓	0.469	2.628

Cell Description

The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



Functions

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
DLY4X1	5.0	4.6

Functional Schematic

AC Power

Pin	Power (µW/MHz)
	X1
A	0.0490

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0018

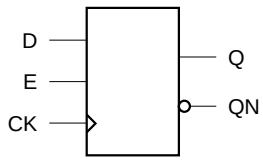
Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → Y↑	0.708	4.564
A → Y↓	0.648	2.771

Cell Description

The EDFF cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E).

Logic Symbol



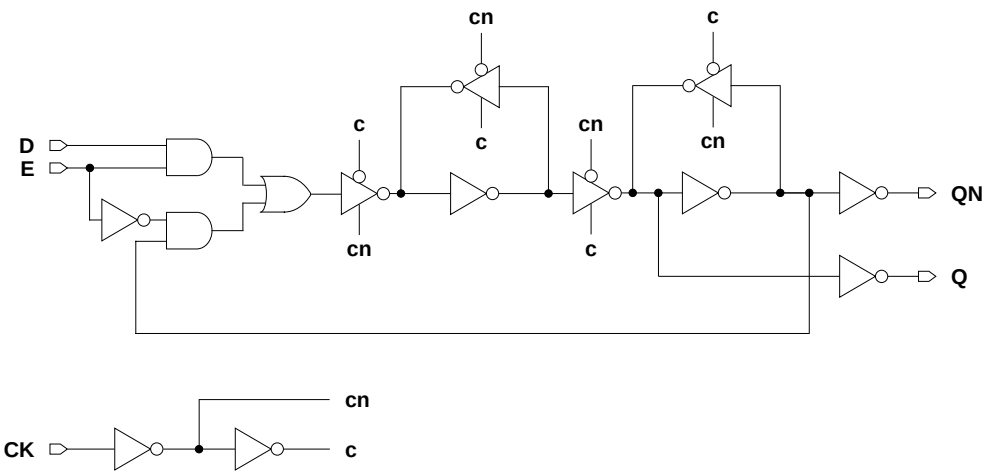
Functions

E	D	CK	Q[n+1]	QN[n+1]
0	x	x	Q[n]	QN[n]
1	0	↑	0	1
1	1	↑	1	0
1	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
EDFFXL	5.0	15.2
EDFFX1	5.0	15.2
EDFFX2	5.0	17.8
EDFFX4	5.0	20.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0342	0.0342	0.0446	0.0691
CK	0.0400	0.0389	0.0455	0.0645
E	0.0499	0.0467	0.0580	0.0865
Q	0.0265	0.0353	0.0624	0.1137

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0028	0.0019	0.0023	0.0035
CK	0.0022	0.0029	0.0041	0.0066
E	0.0052	0.0043	0.0046	0.0058

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.231	0.205	0.180	0.159	6.242	5.051	2.246	1.138
CK → Q↓	0.182	0.160	0.147	0.135	3.396	2.717	1.262	0.616
CK → QN↑	0.257	0.221	0.207	0.187	6.249	4.522	2.246	1.138
CK → QN↓	0.340	0.293	0.264	0.233	3.427	2.456	1.256	0.611

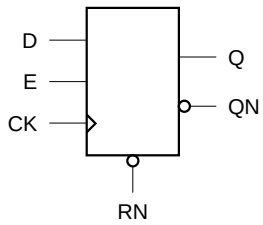
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.09	0.10	0.12	0.12
	setup↓ → CK	0.23	0.38	0.34	0.30
	hold↑ → CK	-0.07	-0.08	-0.09	-0.09
	hold↓ → CK	-0.12	-0.26	-0.22	-0.18
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
E	setup↑ → CK	0.27	0.42	0.38	0.34
	setup↓ → CK	0.15	0.30	0.27	0.22
	hold↑ → CK	-0.08	-0.09	-0.10	-0.10
	hold↓ → CK	-0.11	-0.13	-0.15	-0.16

Cell Description

The EDFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E) and synchronous active-low reset (RN).

Logic Symbol



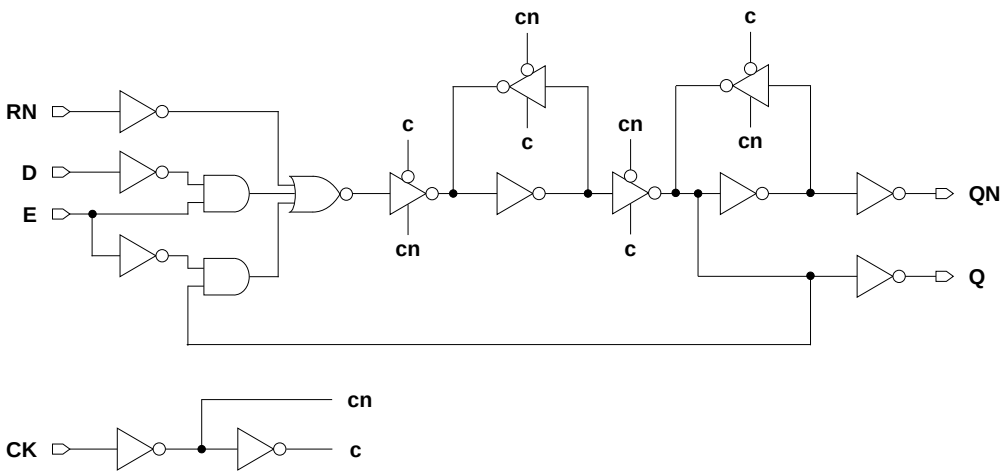
Functions

RN	E	D	CK	Q[n+1]	QN[n+1]
0	x	x	↑	0	1
x	x	x	↓	Q[n]	QN[n]
1	0	x	↑	Q[n]	QN[n]
1	1	0	↑	0	1
1	1	1	↑	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
EDFFTRXL	5.0	16.5
EDFFTRX1	5.0	16.5
EDFFTRX2	5.0	17.8
EDFFTRX4	5.0	21.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0380	0.0370	0.0474	0.0742
CK	0.0432	0.0421	0.0503	0.0724
E	0.0548	0.0490	0.0624	0.0948
RN	0.0438	0.0408	0.0530	0.0813
Q	0.0254	0.0333	0.0615	0.1082

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0029	0.0019	0.0023	0.0037
CK	0.0023	0.0031	0.0042	0.0064
E	0.0056	0.0045	0.0049	0.0061
RN	0.0027	0.0020	0.0023	0.0036

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.236	0.210	0.190	0.168	6.254	4.522	2.251	1.138
CK → Q↓	0.190	0.170	0.150	0.134	3.205	2.467	1.224	0.616
CK → QN↑	0.275	0.238	0.210	0.188	6.253	4.523	2.232	1.137
CK → QN↓	0.345	0.305	0.272	0.243	3.422	2.459	1.217	0.612

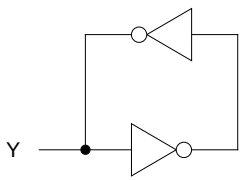
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	0.12	0.15	0.16	0.15
	setup↓ → CK	0.26	0.42	0.37	0.31
	hold↑ → CK	-0.09	-0.12	-0.12	-0.11
	hold↓ → CK	-0.13	-0.30	-0.25	-0.20
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
E	setup↑ → CK	0.29	0.45	0.40	0.34
	setup↓ → CK	0.18	0.35	0.30	0.23
	hold↑ → CK	-0.12	-0.13	-0.14	-0.12
	hold↓ → CK	-0.13	-0.17	-0.19	-0.19
RN	setup↑ → CK	0.14	0.16	0.17	0.16
	setup↓ → CK	0.23	0.34	0.31	0.27
	hold↑ → CK	-0.11	-0.13	-0.14	-0.12
	hold↓ → CK	-0.08	-0.20	-0.18	-0.13

Cell Description

The HOLD cell holds data at a known value. This cell is often used for holding data on a tri-state bus.

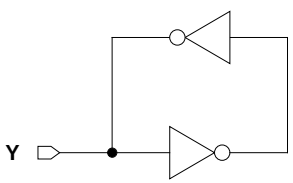
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
HOLDX1	5.0	2.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
Y	0.0209

Pin Capacitance

Pin	Capacitance (pF)
	X1
Y	0.0428

Cell Description

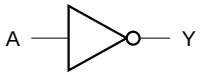
The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Functions

A	Y
0	1
1	0

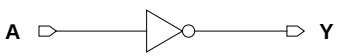
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
INVXL	5.0	1.3
INVX1	5.0	1.3
INVX2	5.0	2.0
INVX3	5.0	2.6
INVX4	5.0	2.6
INVX8	5.04	3.96
INVX12	5.04	8.58
INVX16	5.04	11.22
INVX20	5.04	12.54

Functional Schematic



AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0087	0.0114	0.0209	0.0315	0.0378	0.0775	0.1665	0.2250	0.2804

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0026	0.0036	0.0070	0.0100	0.0129	0.0267	0.0067	0.0088	0.0109

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.023	0.023	0.020	0.022	0.018	0.018	0.122	0.119	0.117
A → Y↓	0.015	0.014	0.012	0.013	0.011	0.012	0.119	0.113	0.110

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6.229	4.512	2.256	1.507	1.137	0.519	0.346	0.260	0.208
A → Y↓	3.237	2.401	1.195	0.798	0.598	0.356	0.240	0.180	0.144

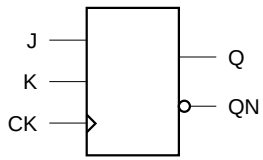
Cell Description

The JKFF cell is a positive-edge triggered JK-type flip-flop.

Function

J	K	CK	Q[n+1]	QN[n+1]
x	x	↓	Q[n]	QN[n]
0	0	↑	Q[n]	QN[n]
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	QN[n]	Q[n]

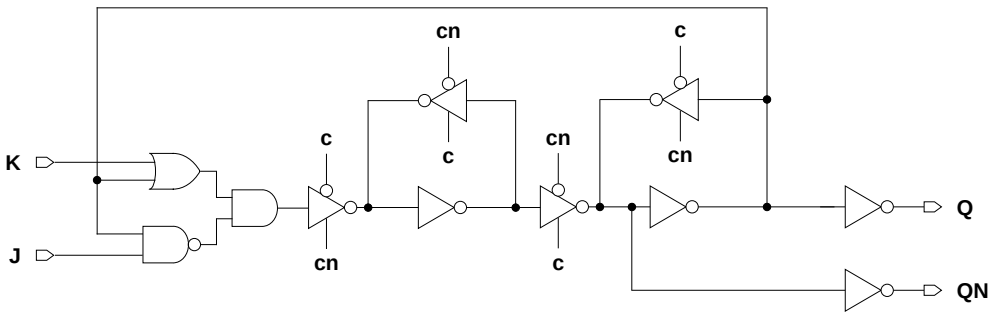
Logic Symbol

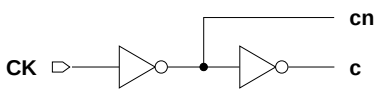


Cell Size

Drive Strength	Height (μm)	Width (μm)
JKFFXL	5.0	13.9
JKFFX1	5.0	13.9
JKFFX2	5.0	16.5
JKFFX4	5.04	19.80

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0295	0.0290	0.0395	0.0661
K	0.0261	0.0261	0.0359	0.0561
CK	0.0363	0.0350	0.0432	0.0638
Q	0.0351	0.0402	0.0785	0.1293

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0022	0.0019	0.0019	0.0024
K	0.0028	0.0018	0.0022	0.0035
CK	0.0020	0.0028	0.0037	0.0068

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.259	0.219	0.218	0.190	6.261	4.522	2.218	1.040
CK → Q↓	0.342	0.293	0.278	0.248	3.460	2.463	1.216	0.722
CK → QN↑	0.220	0.196	0.197	0.170	6.246	4.936	2.219	1.040
CK → QN↓	0.171	0.153	0.158	0.138	3.395	2.884	1.227	0.726

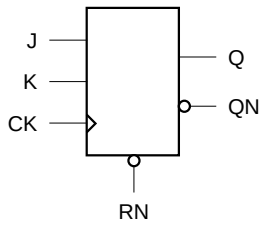
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.16	0.23	0.22	0.22
	setup↓ → CK	0.12	0.13	0.15	0.17
	hold↑ → CK	-0.09	-0.16	-0.16	-0.15
	hold↓ → CK	-0.12	-0.12	-0.13	-0.16
K	setup↑ → CK	0.09	0.09	0.11	0.10
	setup↓ → CK	0.14	0.30	0.24	0.20
	hold↑ → CK	-0.08	-0.08	-0.09	-0.09
	hold↓ → CK	-0.12	-0.26	-0.20	-0.17
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25

Cell Description

The JKFFR cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low reset (RN).

Logic Symbol



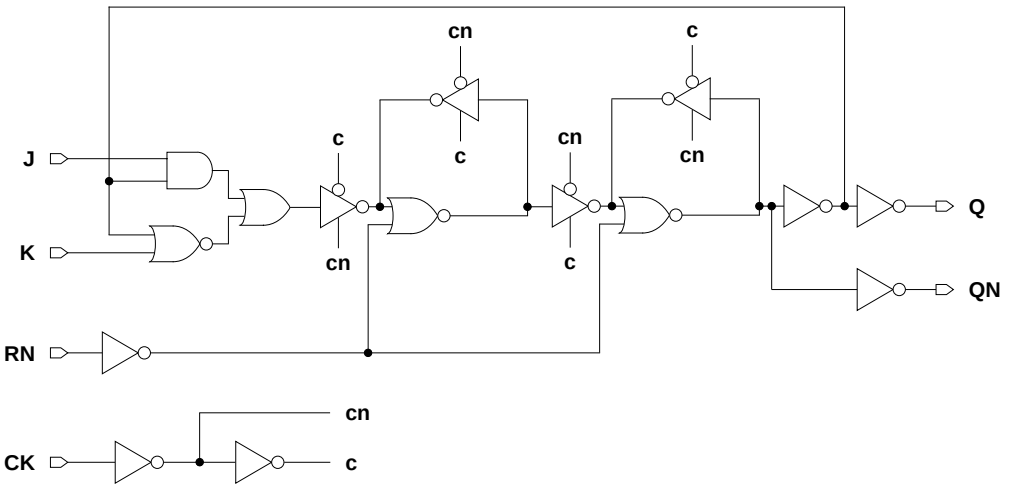
Function

RN	J	K	CK	Q[n+1]	QN[n+1]
1	x	x	↓	Q[n]	QN[n]
0	x	x	x	0	1
1	0	0	↑	Q[n]	QN[n]
1	0	1	↑	0	1
1	1	0	↑	1	0
1	1	1	↑	QN[n]	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
JKFFRXL	5.0	17.2
JKFFRX1	5.0	18.5
JKFFRX2	5.0	18.5
JKFFRX4	5.0	23.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0278	0.0258	0.0272	0.0388
K	0.0335	0.0298	0.0332	0.0454
CK	0.0373	0.0366	0.0381	0.0456
RN	0.0164	0.0175	0.0213	0.0349
Q	0.0527	0.0562	0.0919	0.1493

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0028	0.0019	0.0018	0.0023
K	0.0025	0.0023	0.0023	0.0024
CK	0.0020	0.0025	0.0029	0.0039
RN	0.0021	0.0026	0.0033	0.0056

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.462	0.421	0.398	0.341	6.254	4.523	2.219	1.110
CK → Q↓	0.356	0.361	0.326	0.280	3.465	2.487	1.241	0.603
RN → Q↓	0.318	0.299	0.263	0.233	3.459	2.484	1.240	0.602
CK → QN↑	0.222	0.234	0.225	0.197	6.237	4.515	2.219	1.110
CK → QN↓	0.361	0.332	0.321	0.277	3.512	2.608	1.255	0.610
RN → QN↑	0.180	0.169	0.160	0.149	6.238	4.517	2.220	1.110

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.11	0.11	0.13	0.14
	setup↓ → CK	0.12	0.25	0.26	0.22
	hold↑ → CK	-0.09	-0.10	-0.11	-0.12
	hold↓ → CK	-0.09	-0.20	-0.20	-0.16
K	setup↑ → CK	0.16	0.23	0.25	0.24
	setup↓ → CK	0.16	0.15	0.16	0.17
	hold↑ → CK	-0.09	-0.17	-0.19	-0.16
	hold↓ → CK	-0.15	-0.13	-0.14	-0.16
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.05	0.05	0.08	0.07

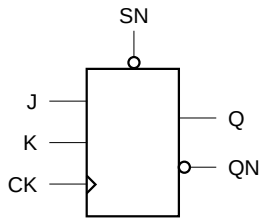
Cell Description

The JKFFS cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low set (SN).

Function

SN	J	K	CK	Q[n+1]	QN[n+1]
1	x	x	⌐	Q[n]	QN[n]
0	x	x	x	1	0
1	0	0	⌐	Q[n]	QN[n]
1	0	1	⌐	0	1
1	1	0	⌐	1	0
1	1	1	⌐	QN[n]	Q[n]

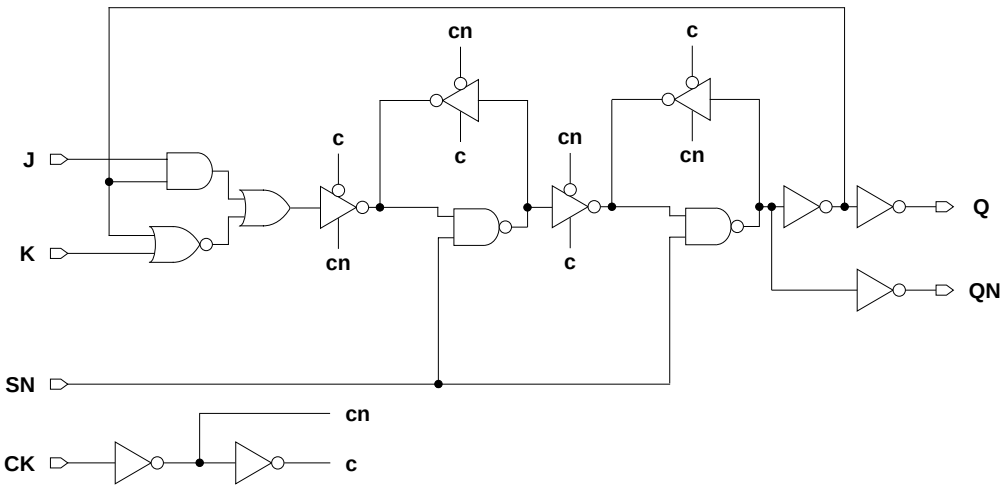
Logic Symbol



Cell Size

Drive Strength	Height (μm)	Width (μm)
JKFFSXL	5.0	16.5
JKFFSX1	5.0	17.2
JKFFSX2	5.0	17.8
JKFFSX4	5.04	20.46

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0274	0.0240	0.0263	0.0302
K	0.0387	0.0325	0.0360	0.0451
CK	0.0384	0.0361	0.0365	0.0447
SN	0.0051	0.0066	0.0095	0.0156
Q	0.0489	0.0579	0.0851	0.1570

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0026	0.0017	0.0017	0.0020
K	0.0023	0.0023	0.0023	0.0025
CK	0.0021	0.0025	0.0028	0.0036
SN	0.0051	0.0060	0.0079	0.0127

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.413	0.370	0.356	0.347	6.256	4.520	2.319	1.040
CK → Q↓	0.379	0.344	0.316	0.285	3.468	2.462	1.241	0.722
SN → Q↑	0.221	0.182	0.176	0.165	6.250	4.523	2.319	1.039
CK → QN↑	0.238	0.240	0.215	0.205	6.263	4.726	2.320	1.041
CK → QN↓	0.316	0.296	0.280	0.281	3.386	2.532	1.233	0.723
SN → QN↓	0.127	0.109	0.101	0.100	3.363	2.531	1.235	0.725

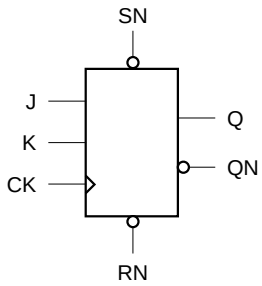
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.10	0.11	0.12	0.12
	setup↓ → CK	0.15	0.31	0.33	0.25
	hold↑ → CK	-0.09	-0.10	-0.10	-0.12
	hold↓ → CK	-0.12	-0.27	-0.29	-0.21
K	setup↑ → CK	0.19	0.30	0.32	0.27
	setup↓ → CK	0.16	0.14	0.14	0.16
	hold↑ → CK	-0.11	-0.23	-0.24	-0.19
	hold↓ → CK	-0.15	-0.13	-0.13	-0.15
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.02	-0.01	0.00	-0.01

Cell Description

The JKFFSR cell is a positive-edge triggered JK-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Logic Symbol



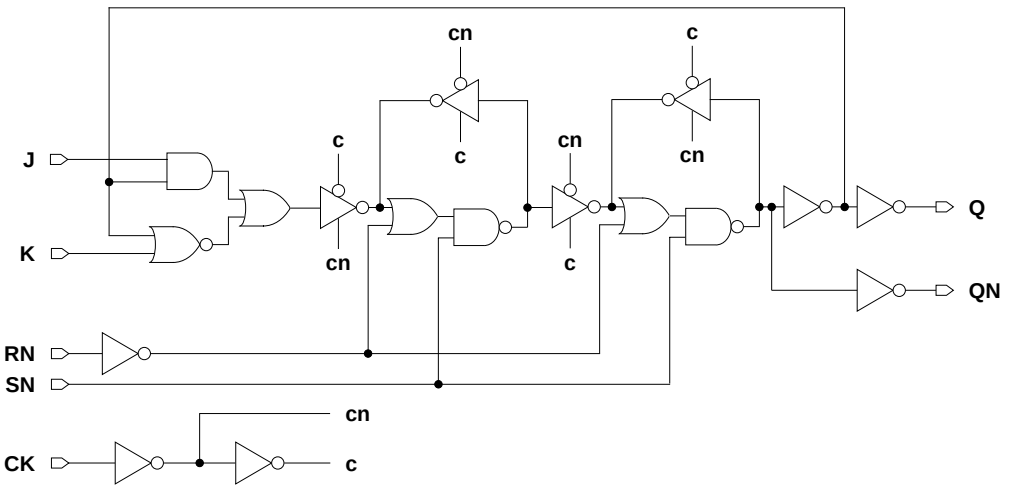
Function

RN	SN	J	K	CK	Q[n+1]	QN[n+1]
1	1	x	x	↓	Q[n]	QN[n]
1	0	x	x	x	1	0
0	1	x	x	x	0	1
0	0	x	x	x	1	0
1	1	0	0	↑	Q[n]	QN[n]
1	1	0	1	↑	0	1
1	1	1	0	↑	1	0
1	1	1	1	↑	QN[n]	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
JKFFSRXL	5.0	19.8
JKFFSRX1	5.0	19.8
JKFFSRX2	5.0	20.5
JKFFSRX4	5.0	21.8

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
J	0.0318	0.0277	0.0302	0.0302
K	0.0367	0.0314	0.0369	0.0370
CK	0.0382	0.0368	0.0388	0.0390
SN	0.0051	0.0060	0.0099	0.0099
RN	0.0138	0.0157	0.0210	0.0210
Q	0.0604	0.0672	0.1016	0.1515

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
J	0.0027	0.0017	0.0019	0.0019
K	0.0026	0.0026	0.0026	0.0026
CK	0.0019	0.0024	0.0028	0.0028
SN	0.0043	0.0049	0.0070	0.0070
RN	0.0023	0.0027	0.0038	0.0038

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.522	0.446	0.429	0.470	6.259	4.524	2.249	1.125
CK → Q↓	0.414	0.366	0.346	0.378	3.490	2.463	1.219	0.611
SN → Q↑	0.243	0.206	0.184	0.212	6.260	4.523	2.250	1.125
SN → Q↓	0.279	0.216	0.205	0.235	3.479	2.460	1.218	0.611
RN → Q↓	0.352	0.287	0.270	0.300	3.478	2.459	1.219	0.611
CK → QN↑	0.274	0.267	0.254	0.275	6.265	5.059	2.254	1.130
CK → QN↓	0.418	0.374	0.360	0.396	3.607	2.799	1.243	0.633
SN → QN↑	0.136	0.116	0.113	0.132	6.286	5.068	2.258	1.131
SN → QN↓	0.152	0.137	0.118	0.143	3.394	2.756	1.224	0.617
RN → QN↑	0.209	0.186	0.177	0.197	6.284	5.070	2.258	1.131

Timing Constraints at 25°C, 1.8V, Typical Process

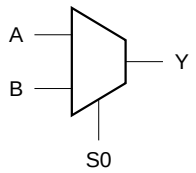
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
J	setup↑ → CK	0.12	0.16	0.15	0.14
	setup↓ → CK	0.12	0.27	0.23	0.23
	hold↑ → CK	-0.11	-0.14	-0.12	-0.12
	hold↓ → CK	-0.08	-0.20	-0.17	-0.17
K	setup↑ → CK	0.17	0.27	0.25	0.24
	setup↓ → CK	0.16	0.19	0.17	0.17
	hold↑ → CK	-0.09	-0.19	-0.16	-0.16
	hold↓ → CK	-0.16	-0.16	-0.16	-0.16
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.02	0.00	0.00	0.00
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.06	0.11	0.08	0.08

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y).The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

Logic Symbol



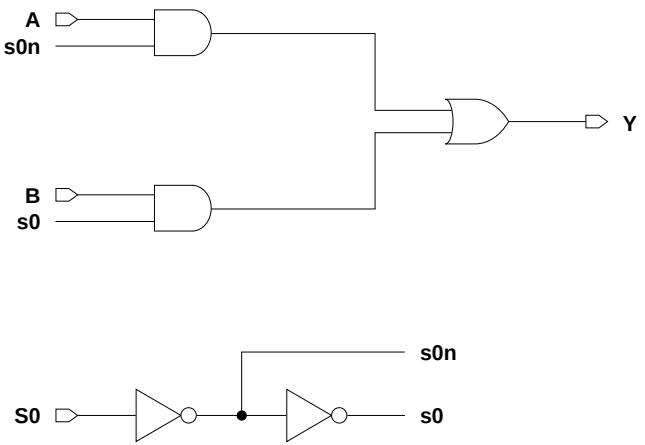
Functions

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
MX2XL	5.0	5.3
MX2X1	5.0	5.3
MX2X2	5.0	5.9
MX2X4	5.04	6.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0331	0.0339	0.0571	0.0856
A	0.0223	0.0269	0.0476	0.0697
B	0.0254	0.0294	0.0522	0.0770

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0060	0.0056	0.0085	0.0103
A	0.0022	0.0032	0.0057	0.0071
B	0.0023	0.0033	0.0052	0.0061

Delay Tables at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
S0 → Y↑	0.125	0.120	0.121	0.136
S0 → Y↓	0.127	0.118	0.110	0.134
A → Y↑	0.097	0.087	0.078	0.096
A → Y↓	0.147	0.119	0.109	0.126
B → Y↑	0.098	0.086	0.080	0.086
B → Y↓	0.153	0.124	0.115	0.140

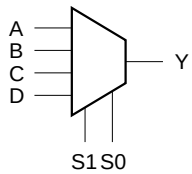
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
S0 → Y↑	6.249	4.520	2.236	1.126
S0 → Y↓	3.493	2.469	1.228	0.736
A → Y↑	6.250	4.518	2.236	1.127
A → Y↓	3.497	2.476	1.229	0.733
B → Y↑	6.250	4.521	2.236	1.126
B → Y↓	3.506	2.477	1.229	0.737

Cell Description

The MX4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (\overline{S0} \bullet S1 \bullet C) + (S0 \bullet S1 \bullet D)$$

Logic Symbol



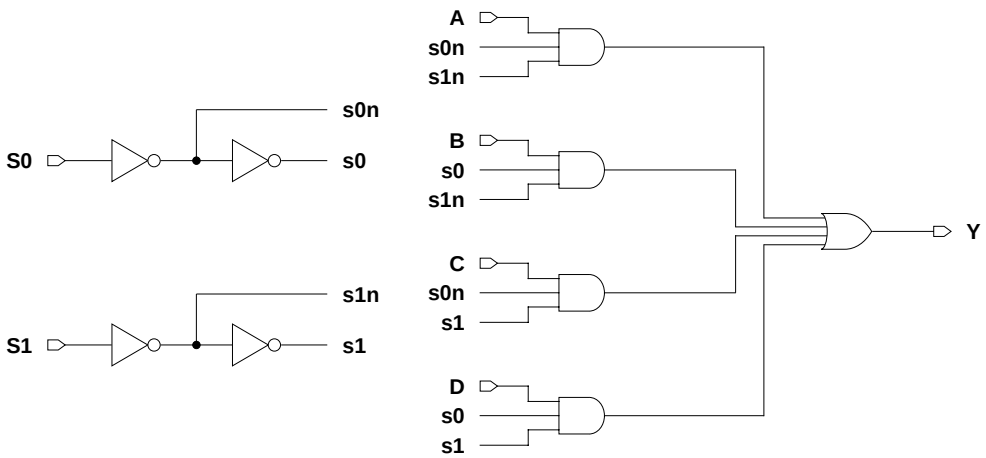
Functions

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
MX4XL	5.0	13.2
MX4X1	5.0	13.2
MX4X2	5.04	15.18
MX4X4	5.04	15.84

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0544	0.0678	0.1150	0.1397
S1	0.0318	0.0399	0.0645	0.0792
A	0.0333	0.0444	0.0713	0.0981
B	0.0367	0.0480	0.0799	0.1091
C	0.0388	0.0506	0.0824	0.1120
D	0.0432	0.0555	0.0909	0.1207

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0102	0.0133	0.0228	0.0228
S1	0.0059	0.0067	0.0110	0.0111
A	0.0020	0.0043	0.0067	0.0067
B	0.0021	0.0042	0.0065	0.0065
C	0.0019	0.0042	0.0068	0.0068
D	0.0021	0.0043	0.0066	0.0066

Delays at 25°C, 1.8V, Typical Process

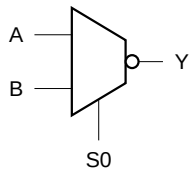
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S0 → Y↑	0.229	0.172	0.159	0.170	6.284	4.526	2.239	1.044
S0 → Y↓	0.256	0.193	0.187	0.217	3.953	2.582	1.278	0.764
S1 → Y↑	0.137	0.132	0.127	0.138	6.283	4.527	2.239	1.044
S1 → Y↓	0.125	0.123	0.120	0.150	3.835	2.566	1.270	0.759
A → Y↑	0.170	0.129	0.120	0.133	6.282	4.530	2.240	1.043
A → Y↓	0.248	0.175	0.166	0.195	3.928	2.575	1.272	0.761
B → Y↑	0.169	0.128	0.125	0.138	6.281	4.526	2.240	1.044
B → Y↓	0.252	0.179	0.173	0.203	3.933	2.577	1.272	0.761
C → Y↑	0.176	0.131	0.125	0.136	6.290	4.528	2.241	1.044
C → Y↓	0.259	0.184	0.178	0.208	3.974	2.585	1.279	0.764
D → Y↑	0.176	0.130	0.125	0.136	6.288	4.530	2.240	1.044
D → Y↓	0.266	0.188	0.182	0.212	3.983	2.587	1.279	0.764

Cell Description

The MXI2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet A) + (S0 \bullet B)}$$

Logic Symbol



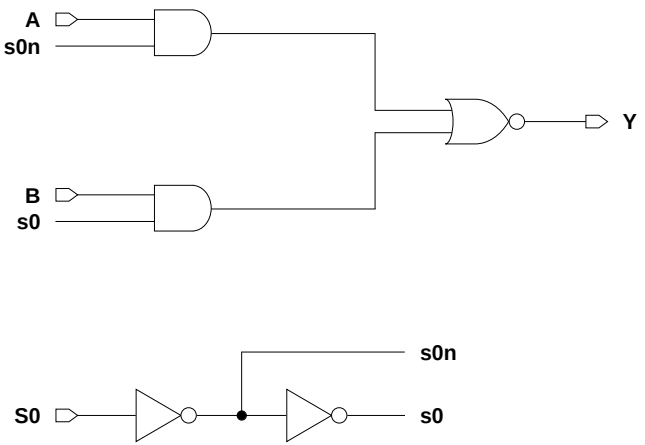
Functions

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
MXI2XL	5.0	4.6
MXI2X1	5.0	4.6
MXI2X2	5.04	5.28
MXI2X4	5.04	9.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0254	0.0288	0.0517	0.0954
A	0.0167	0.0204	0.0354	0.0755
B	0.0173	0.0249	0.0429	0.0891

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0061	0.0067	0.0100	0.0207
A	0.0027	0.0039	0.0068	0.0133
B	0.0020	0.0039	0.0062	0.0134

Delay Tables at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
S0 → Y↑	0.051	0.053	0.058	0.053
S0 → Y↓	0.056	0.068	0.057	0.062
A → Y↑	0.060	0.049	0.049	0.046
A → Y↓	0.043	0.038	0.042	0.041
B → Y↑	0.081	0.052	0.051	0.051
B → Y↓	0.047	0.035	0.044	0.038

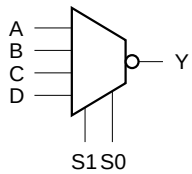
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
S0 → Y↑	9.538	4.872	2.729	1.305
S0 → Y↓	4.415	2.791	2.058	0.884
A → Y↑	7.047	4.901	2.739	1.312
A → Y↓	3.894	2.852	1.772	0.903
B → Y↑	9.706	4.900	2.786	1.309
B → Y↓	4.701	2.850	2.136	0.900

Cell Description

The MXI4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (\overline{S0} \bullet S1 \bullet C) + (S0 \bullet S1 \bullet D)}$$

Logic Symbol



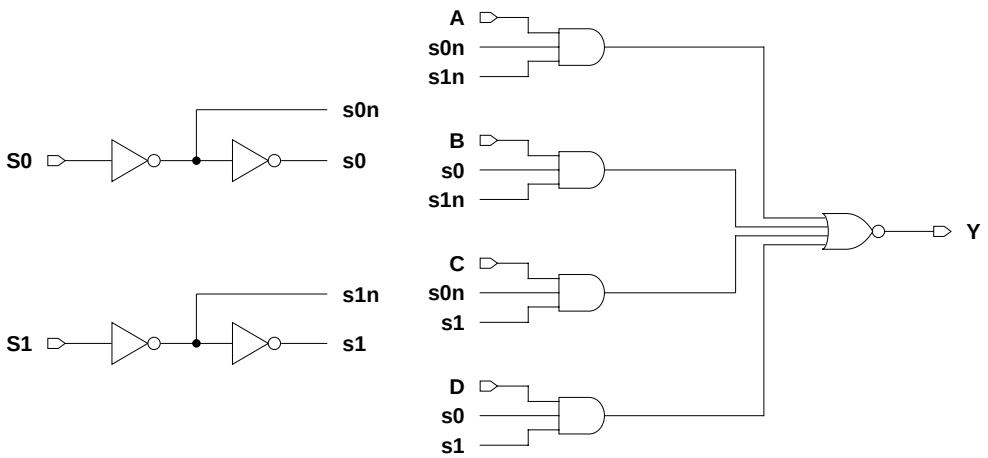
Functions

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	1
0	0	1	x	x	x	0
0	1	x	0	x	x	1
0	1	x	1	x	x	0
1	0	x	x	0	x	1
1	0	x	x	1	x	0
1	1	x	x	x	0	1
1	1	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
MXI4XL	5.0	15.2
MXI4X1	5.0	15.2
MXI4X2	5.0	15.8
MXI4X4	5.04	16.50

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S0	0.0642	0.0615	0.1027	0.1431
S1	0.0341	0.0348	0.0586	0.0825
A	0.0440	0.0465	0.0835	0.1149
B	0.0477	0.0489	0.0898	0.1200
C	0.0383	0.0400	0.0665	0.0937
D	0.0395	0.0417	0.0704	0.1006

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S0	0.0101	0.0084	0.0138	0.0169
S1	0.0044	0.0042	0.0052	0.0062
A	0.0021	0.0026	0.0045	0.0055
B	0.0020	0.0025	0.0045	0.0057
C	0.0021	0.0026	0.0046	0.0057
D	0.0021	0.0025	0.0044	0.0054

Delays at 25°C, 1.8V, Typical Process

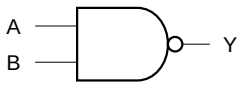
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S0 → Y↑	0.251	0.229	0.201	0.208	6.253	4.522	2.307	1.120
S0 → Y↓	0.302	0.259	0.230	0.252	3.534	2.487	1.232	0.620
S1 → Y↑	0.136	0.129	0.123	0.134	6.250	4.519	2.307	1.119
S1 → Y↓	0.138	0.121	0.107	0.119	3.525	2.478	1.226	0.618
A → Y↑	0.263	0.225	0.199	0.207	6.252	4.521	2.308	1.120
A → Y↓	0.247	0.209	0.188	0.216	3.534	2.488	1.232	0.620
B → Y↑	0.265	0.227	0.205	0.211	6.253	4.521	2.308	1.120
B → Y↓	0.246	0.207	0.188	0.213	3.534	2.488	1.232	0.620
C → Y↑	0.243	0.208	0.176	0.174	6.251	4.521	2.307	1.119
C → Y↓	0.236	0.199	0.171	0.190	3.526	2.486	1.227	0.618
D → Y↑	0.247	0.210	0.177	0.178	6.253	4.520	2.307	1.119
D → Y↓	0.235	0.198	0.172	0.187	3.525	2.486	1.227	0.618

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B)}$$

Logic Symbol



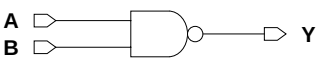
Functions

A	B	Y
0	x	1
x	0	1
1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND2XL	5.0	2.0
NAND2X1	5.0	2.0
NAND2X2	5.0	3.3
NAND2X4	5.0	4.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0098	0.0135	0.0260	0.0508
B	0.0123	0.0169	0.0338	0.0660

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0031	0.0040	0.0079	0.0158
B	0.0029	0.0038	0.0082	0.0154

Delay at 25^{O}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.028	0.027	0.025	0.025
A → Y↓	0.018	0.017	0.016	0.015
B → Y↑	0.035	0.034	0.033	0.033
B → Y↓	0.023	0.021	0.021	0.020

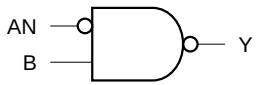
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.234	4.512	2.211	1.179
A → Y↓	3.893	2.782	1.356	0.680
B → Y↑	6.229	4.512	2.211	1.178
B → Y↓	3.901	2.786	1.358	0.681

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B)}$$

Logic Symbol



Functions

AN	B	Y
1	x	1
x	0	1
0	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND2BXL	5.0	2.6
NAND2BX1	5.0	2.6
NAND2BX2	5.0	4.0
NAND2BX4	5.0	5.3

Functional Schematic

AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0156	0.0184	0.0336	0.0657
B	0.0101	0.0138	0.0252	0.0488

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0017	0.0017	0.0026	0.0047
B	0.0030	0.0040	0.0083	0.0157

Delays at 25°C, 1.8V, Typical Process

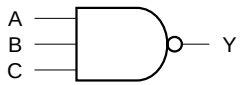
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.059	0.064	0.066	0.065	6.240	4.518	2.244	1.180
AN → Y↓	0.081	0.090	0.088	0.083	3.937	2.738	1.369	0.686
B → Y↑	0.035	0.034	0.032	0.032	6.234	4.516	2.252	1.179
B → Y↓	0.025	0.024	0.024	0.023	3.912	2.724	1.362	0.683

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C)}$$

Logic Symbol



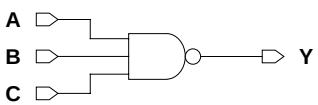
Functions

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND3XL	5.0	2.6
NAND3X1	5.0	2.6
NAND3X2	5.0	4.6
NAND3X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0111	0.0168	0.0279	0.0461
B	0.0153	0.0216	0.0369	0.0637
C	0.0186	0.0253	0.0496	0.0774

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0034	0.0048	0.0084	0.0144
B	0.0032	0.0047	0.0088	0.0139
C	0.0032	0.0045	0.0094	0.0142

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.041	0.034	0.031	0.032
A → Y↓	0.029	0.024	0.020	0.020
B → Y↑	0.050	0.043	0.040	0.042
B → Y↓	0.036	0.031	0.027	0.027
C → Y↑	0.059	0.051	0.050	0.051
C → Y↓	0.039	0.033	0.031	0.031

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.234	4.151	2.209	1.449
A → Y↓	4.396	3.005	1.503	0.961
B → Y↑	6.233	4.150	2.209	1.447
B → Y↓	4.403	3.009	1.504	0.962
C → Y↑	6.236	4.152	2.211	1.448
C → Y↓	4.404	3.009	1.505	0.962

Cell Description

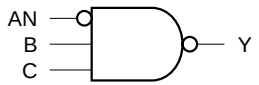
The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C)}$$

Functions

AN	B	C	Y
1	x	x	1
x	0	x	1
x	x	0	1
0	1	1	0

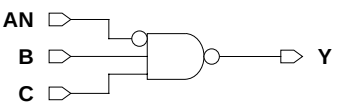
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND3BXL	5.0	3.3
NAND3BX1	5.0	3.3
NAND3BX2	5.0	5.3
NAND3BX4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0228	0.0242	0.0388	0.0635
B	0.0128	0.0168	0.0295	0.0485
C	0.0153	0.0221	0.0407	0.0657

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0017	0.0017	0.0028	0.0049
B	0.0033	0.0047	0.0088	0.0138
C	0.0032	0.0047	0.0096	0.0143

Delays at 25^{o}C, 1.8V, Typical Process

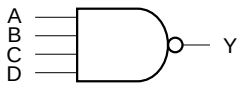
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.078	0.075	0.071	0.067	6.246	4.156	2.212	1.410
AN → Y↓	0.100	0.101	0.087	0.081	4.429	3.025	1.512	0.972
B → Y↑	0.049	0.042	0.040	0.039	6.239	4.153	2.211	1.410
B → Y↓	0.038	0.034	0.030	0.030	4.413	3.016	1.508	0.970
C → Y↑	0.058	0.050	0.049	0.049	6.240	4.154	2.212	1.415
C → Y↓	0.041	0.037	0.034	0.033	4.413	3.016	1.508	0.970

Cell Description

The NAND4 cell provides a logical NAND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C \bullet D)}$$

Logic Symbol



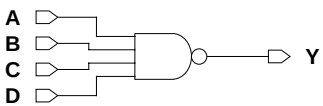
Functions

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND4XL	5.0	3.3
NAND4X1	5.0	3.3
NAND4X2	5.0	5.9
NAND4X4	5.0	11.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0127	0.0177	0.0320	0.0648
B	0.0170	0.0229	0.0452	0.0911
C	0.0202	0.0286	0.0542	0.1096
D	0.0239	0.0330	0.0646	0.1305

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0033	0.0048	0.0089	0.0185
B	0.0035	0.0047	0.0091	0.0189
C	0.0035	0.0047	0.0095	0.0194
D	0.0032	0.0046	0.0098	0.0204

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.040	0.037	0.035	0.035
A → Y↓	0.028	0.025	0.024	0.024
B → Y↑	0.052	0.048	0.046	0.046
B → Y↓	0.040	0.035	0.033	0.033
C → Y↑	0.062	0.057	0.056	0.056
C → Y↓	0.045	0.041	0.039	0.039
D → Y↑	0.069	0.066	0.065	0.066
D → Y↓	0.048	0.044	0.043	0.043

Delays at 25°C, 1.8V, Typical Process

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.236	4.372	2.211	1.106
A → Y↓	5.028	3.459	1.730	0.865
B → Y↑	6.231	4.366	2.208	1.104
B → Y↓	5.037	3.464	1.732	0.866
C → Y↑	6.236	4.371	2.210	1.105
C → Y↓	5.038	3.463	1.732	0.866
D → Y↑	6.256	4.380	2.215	1.107
D → Y↓	5.036	3.463	1.732	0.866

Cell Description

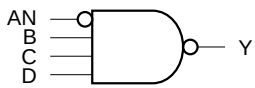
The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C \bullet D)}$$

Functions

AN	B	C	D	Y
1	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
0	1	1	1	0

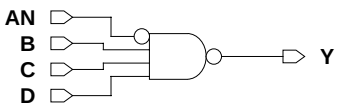
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND4BXL	5.0	4.0
NAND4BX1	5.0	4.6
NAND4BX2	5.0	6.6
NAND4BX4	5.0	11.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0201	0.0238	0.0420	0.0841
B	0.0145	0.0196	0.0350	0.0699
C	0.0179	0.0252	0.0456	0.0850
D	0.0213	0.0290	0.0540	0.1080

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0017	0.0017	0.0029	0.0052
B	0.0034	0.0047	0.0091	0.0188
C	0.0033	0.0047	0.0095	0.0194
D	0.0031	0.0045	0.0100	0.0206

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.079	0.081	0.076	0.075	6.245	4.375	2.213	1.106
AN → Y↓	0.099	0.104	0.092	0.090	5.051	3.475	1.737	0.869
B → Y↑	0.054	0.050	0.045	0.045	6.236	4.369	2.210	1.105
B → Y↓	0.044	0.040	0.036	0.036	5.044	3.469	1.734	0.867
C → Y↑	0.064	0.059	0.055	0.055	6.239	4.374	2.211	1.106
C → Y↓	0.050	0.046	0.042	0.042	5.043	3.470	1.734	0.867
D → Y↑	0.073	0.068	0.065	0.066	6.255	4.380	2.215	1.107
D → Y↓	0.053	0.049	0.046	0.046	5.044	3.469	1.735	0.868

Cell Description

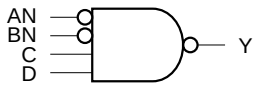
The NAND4BB cell provides a logical NAND of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet \overline{BN} \bullet C \bullet D)}$$

Functions

AN	BN	C	D	Y
1	x	x	x	1
x	1	x	x	1
x	x	0	x	1
x	x	x	0	1
0	0	1	1	0

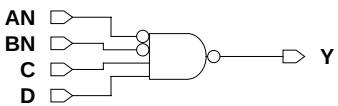
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NAND4BBXL	5.0	5.3
NAND4BBX1	5.0	5.3
NAND4BBX2	5.0	7.3
NAND4BBX4	5.0	12.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0207	0.0247	0.0435	0.0859
BN	0.0246	0.0305	0.0533	0.1054
C	0.0153	0.0199	0.0370	0.0724
D	0.0184	0.0245	0.0470	0.0934

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0017	0.0017	0.0029	0.0052
BN	0.0017	0.0017	0.0029	0.0054
C	0.0034	0.0048	0.0096	0.0194
D	0.0033	0.0047	0.0101	0.0204

Delays at 25°C, 1.8V, Typical Process

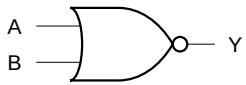
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.079	0.081	0.077	0.076	6.245	4.375	2.211	1.106
AN → Y↓	0.099	0.103	0.093	0.091	5.051	3.475	1.737	0.869
BN → Y↑	0.089	0.092	0.089	0.088	6.242	4.374	2.212	1.106
BN → Y↓	0.108	0.114	0.104	0.100	5.063	3.485	1.740	0.870
C → Y↑	0.063	0.058	0.055	0.055	6.245	4.377	2.214	1.106
C → Y↓	0.051	0.047	0.044	0.044	5.049	3.475	1.736	0.868
D → Y↑	0.072	0.067	0.065	0.065	6.260	4.383	2.217	1.108
D → Y↓	0.054	0.051	0.049	0.049	5.048	3.474	1.737	0.868

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B)}$$

Logic Symbol



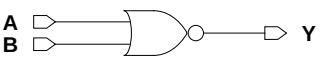
Functions

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR2XL	5.0	2.0
NOR2X1	5.0	2.0
NOR2X2	5.0	3.3
NOR2X4	5.0	4.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0099	0.0131	0.0249	0.0498
B	0.0130	0.0166	0.0340	0.0668

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0032	0.0043	0.0081	0.0165
B	0.0028	0.0039	0.0082	0.0155

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.038	0.037	0.031	0.031
A → Y↓	0.019	0.018	0.015	0.016
B → Y↑	0.047	0.045	0.040	0.039
B → Y↓	0.023	0.022	0.020	0.020

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	9.465	6.723	3.361	1.649
A → Y↓	3.366	2.403	1.195	0.597
B → Y↑	9.455	6.720	3.360	1.648
B → Y↓	3.386	2.410	1.199	0.599

Cell Description

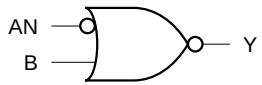
The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B)}$$

Functions

AN	B	Y
1	0	1
x	1	0
0	x	0

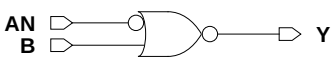
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR2BXL	5.0	2.6
NOR2BX1	5.0	2.6
NOR2BX2	5.0	4.0
NOR2BX4	5.0	5.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0173	0.0203	0.0307	0.0631
B	0.0126	0.0178	0.0331	0.0658

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0017	0.0017	0.0028	0.0049
B	0.0031	0.0042	0.0084	0.0158

Delays at 25°C, 1.8V, Typical Process

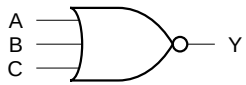
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.069	0.073	0.066	0.066	9.473	6.726	3.363	1.642
AN → Y↓	0.087	0.099	0.086	0.088	3.302	2.435	1.210	0.605
B → Y↑	0.049	0.048	0.042	0.042	9.460	6.722	3.361	1.641
B → Y↓	0.022	0.022	0.020	0.020	3.263	2.411	1.199	0.600

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C)}$$

Logic Symbol



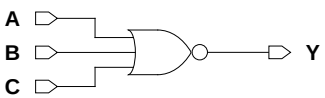
Functions

A	B	C	Y
0	0	0	1
x	x	1	0
x	1	x	0
1	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR3XL	5.0	2.6
NOR3X1	5.0	2.6
NOR3X2	5.0	4.6
NOR3X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0126	0.0171	0.0329	0.0521
B	0.0164	0.0223	0.0432	0.0649
C	0.0197	0.0280	0.0546	0.0872

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0035	0.0047	0.0090	0.0158
B	0.0033	0.0045	0.0094	0.0150
C	0.0032	0.0043	0.0095	0.0147

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.055	0.051	0.044	0.043
A → Y↓	0.022	0.022	0.020	0.019
B → Y↑	0.080	0.075	0.069	0.067
B → Y↓	0.028	0.028	0.026	0.025
C → Y↑	0.088	0.082	0.077	0.074
C → Y↓	0.030	0.031	0.030	0.029

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	12.252	8.498	4.248	2.579
A → Y↓	3.238	2.398	1.193	0.703
B → Y↑	12.237	8.494	4.247	2.578
B → Y↓	3.257	2.407	1.197	0.705
C → Y↑	12.235	8.493	4.247	2.578
C → Y↓	3.302	2.429	1.207	0.709

Cell Description

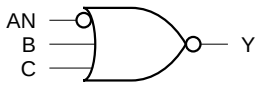
The NOR3B cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C)}$$

Functions

AN	B	C	Y
1	0	0	1
x	x	1	0
x	1	x	0
0	x	x	0

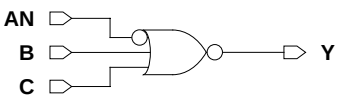
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR3BXL	5.0	4.0
NOR3BX1	5.0	4.0
NOR3BX2	5.0	5.3
NOR3BX4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0185	0.0232	0.0352	0.0655
B	0.0166	0.0227	0.0424	0.0692
C	0.0208	0.0272	0.0545	0.0911

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0015	0.0016	0.0029	0.0047
B	0.0033	0.0045	0.0090	0.0156
C	0.0032	0.0044	0.0096	0.0157

Delays at 25°C, 1.8V, Typical Process

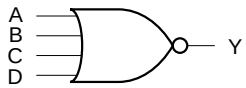
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.088	0.088	0.079	0.079	12.258	8.499	4.250	2.435
AN → Y↓	0.095	0.102	0.092	0.095	3.300	2.431	1.209	0.711
B → Y↑	0.082	0.077	0.069	0.067	12.237	8.493	4.247	2.433
B → Y↓	0.028	0.028	0.025	0.026	3.258	2.408	1.198	0.705
C → Y↑	0.089	0.083	0.077	0.075	12.234	8.493	4.248	2.433
C → Y↓	0.030	0.031	0.030	0.030	3.301	2.429	1.207	0.709

Cell Description

The NOR4 cell provides a logical NOR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C + D)}$$

Logic Symbol



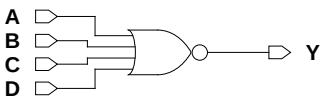
Functions

A	B	C	D	Y
0	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
1	x	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR4XL	5.0	4.0
NOR4X1	5.0	4.0
NOR4X2	5.0	5.9
NOR4X4	5.0	11.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0149	0.0198	0.0366	0.0678
B	0.0195	0.0265	0.0487	0.0920
C	0.0237	0.0324	0.0613	0.1110
D	0.0277	0.0386	0.0756	0.1388

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0039	0.0052	0.0099	0.0187
B	0.0038	0.0051	0.0100	0.0194
C	0.0037	0.0050	0.0105	0.0192
D	0.0035	0.0048	0.0109	0.0193

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.062	0.054	0.043	0.048
A → Y↓	0.025	0.024	0.020	0.021
B → Y↑	0.101	0.094	0.081	0.088
B → Y↓	0.033	0.033	0.030	0.031
C → Y↑	0.124	0.115	0.102	0.108
C → Y↓	0.037	0.039	0.034	0.035
D → Y↑	0.131	0.121	0.110	0.117
D → Y↓	0.037	0.039	0.036	0.036

Delays at 25°C, 1.8V, Typical Process

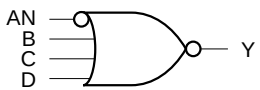
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	13.903	9.471	4.736	2.743
A → Y↓	3.239	2.402	1.195	0.664
B → Y↑	13.889	9.468	4.735	2.743
B → Y↓	3.266	2.413	1.200	0.667
C → Y↑	13.895	9.468	4.734	2.743
C → Y↓	3.299	2.428	1.208	0.671
D → Y↑	13.890	9.467	4.735	2.743
D → Y↓	3.351	2.454	1.221	0.677

Cell Description

The NOR4B cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C + D)}$$

Logic Symbol



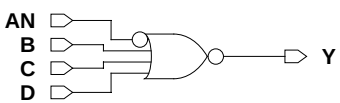
Functions

AN	B	C	D	Y
1	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
0	x	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR4BXL	5.0	4.0
NOR4BX1	5.0	4.0
NOR4BX2	5.0	6.6
NOR4BX4	5.0	11.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0216	0.0261	0.0414	0.0734
B	0.0198	0.0268	0.0513	0.0921
C	0.0237	0.0323	0.0637	0.1137
D	0.0279	0.0400	0.0768	0.1377

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0016	0.0019	0.0033	0.0052
B	0.0037	0.0050	0.0100	0.0191
C	0.0037	0.0050	0.0105	0.0192
D	0.0037	0.0051	0.0107	0.0196

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.097	0.092	0.082	0.083	13.912	9.475	4.737	2.745
AN → Y↓	0.108	0.108	0.098	0.100	3.307	2.430	1.208	0.671
B → Y↑	0.103	0.096	0.084	0.089	13.893	9.469	4.735	2.743
B → Y↓	0.033	0.033	0.030	0.030	3.266	2.411	1.199	0.666
C → Y↑	0.125	0.117	0.106	0.109	13.894	9.468	4.736	2.743
C → Y↓	0.037	0.039	0.035	0.035	3.299	2.429	1.208	0.671
D → Y↑	0.132	0.123	0.112	0.118	13.889	9.468	4.735	2.743
D → Y↓	0.037	0.040	0.036	0.036	3.351	2.454	1.220	0.677

Cell Description

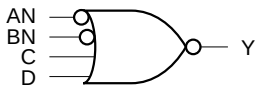
The NOR4BB cell provides a logical NOR of two inverted inputs (AN, BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + \overline{BN} + C + D)}$$

Functions

AN	BN	C	D	Y
1	1	0	0	1
x	x	x	1	0
x	x	1	x	0
x	0	x	x	0
0	x	x	x	0

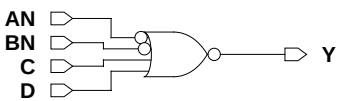
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
NOR4BBXL	5.0	5.3
NOR4BBX1	5.0	5.3
NOR4BBX2	5.0	7.3
NOR4BBX4	5.0	13.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
AN	0.0209	0.0266	0.0412	0.0733
BN	0.0228	0.0304	0.0526	0.0950
C	0.0253	0.0336	0.0653	0.1158
D	0.0294	0.0405	0.0774	0.1377

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
AN	0.0017	0.0019	0.0033	0.0052
BN	0.0020	0.0023	0.0037	0.0052
C	0.0037	0.0050	0.0105	0.0192
D	0.0037	0.0050	0.0110	0.0194

Delays at 25°C, 1.8V, Typical Process

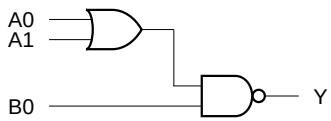
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
AN → Y↑	0.101	0.095	0.084	0.084	13.905	9.474	4.738	2.745
AN → Y↓	0.108	0.108	0.099	0.100	3.301	2.429	1.208	0.671
BN → Y↑	0.147	0.137	0.122	0.128	13.902	9.472	4.735	2.745
BN → Y↓	0.119	0.120	0.110	0.115	3.303	2.429	1.208	0.671
C → Y↑	0.132	0.120	0.108	0.112	13.892	9.468	4.734	2.743
C → Y↓	0.038	0.039	0.035	0.035	3.302	2.428	1.208	0.671
D → Y↑	0.140	0.127	0.115	0.121	13.891	9.467	4.735	2.743
D → Y↓	0.039	0.040	0.037	0.037	3.350	2.453	1.220	0.677

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0}$$

Logic Symbol



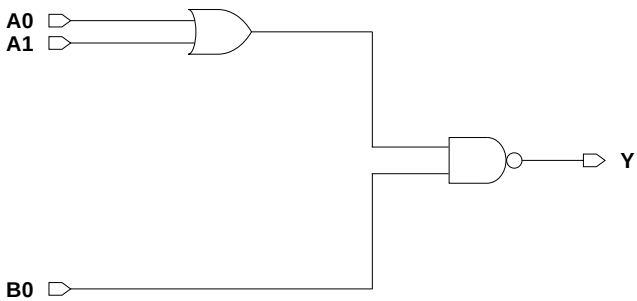
Functions

A0	A1	B0	Y
0	0	x	1
x	x	0	1
x	1	1	0
1	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI21XL	5.0	2.6
OAI21X1	5.0	3.3
OAI21X2	5.0	5.3
OAI21X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0165	0.0222	0.0417	0.0783
A1	0.0188	0.0257	0.0515	0.0954
B0	0.0133	0.0174	0.0323	0.0676

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0033	0.0045	0.0094	0.0183
A1	0.0032	0.0043	0.0086	0.0174
B0	0.0030	0.0040	0.0078	0.0152

Delays at 25^{o}C, 1.8V, Typical Process

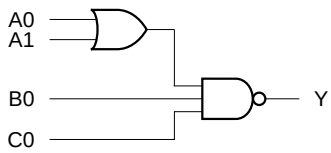
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.067	0.064	0.065	0.053	9.468	6.723	3.362	1.627
A0 → Y↓	0.030	0.028	0.030	0.025	3.903	2.717	1.376	0.682
A1 → Y↑	0.078	0.074	0.073	0.062	9.463	6.722	3.361	1.626
A1 → Y↓	0.037	0.035	0.036	0.031	3.915	2.722	1.378	0.683
B0 → Y↑	0.031	0.029	0.030	0.026	6.243	4.520	2.260	1.161
B0 → Y↓	0.027	0.026	0.026	0.023	3.908	2.718	1.376	0.682

Cell Description

The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0 \bullet C0}$$

Logic Symbol



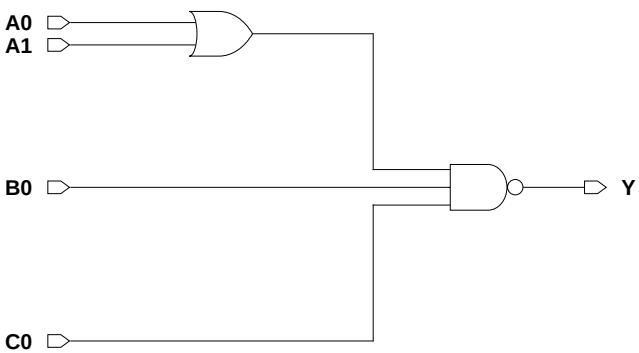
Functions

A0	A1	B0	C0	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
x	1	1	1	0
1	x	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI211XL	5.0	4.0
OAI211X1	5.0	4.0
OAI211X2	5.0	6.6
OAI211X4	5.0	5.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0230	0.0296	0.0568	0.0791
A1	0.0252	0.0345	0.0675	0.0833
B0	0.0146	0.0210	0.0379	0.0674
C0	0.0199	0.0267	0.0484	0.0715

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0035	0.0049	0.0100	0.0032
A1	0.0034	0.0046	0.0092	0.0032
B0	0.0032	0.0043	0.0082	0.0032
C0	0.0032	0.0043	0.0085	0.0029

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.099	0.096	0.092	0.243	9.481	6.730	3.365	1.109
A0 → Y↓	0.044	0.041	0.040	0.173	4.407	3.034	1.510	0.610
A1 → Y↑	0.109	0.106	0.100	0.254	9.477	6.726	3.364	1.109
A1 → Y↓	0.052	0.049	0.047	0.183	4.417	3.040	1.517	0.610
B0 → Y↑	0.040	0.039	0.037	0.158	6.238	4.519	2.338	1.109
B0 → Y↓	0.035	0.033	0.031	0.167	4.411	3.036	1.516	0.610
C0 → Y↑	0.050	0.049	0.047	0.169	6.240	4.520	2.337	1.109
C0 → Y↓	0.044	0.041	0.039	0.175	4.419	3.040	1.518	0.610

Cell Description

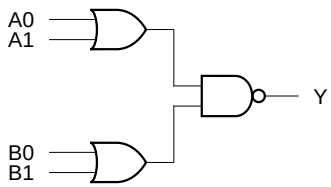
The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1)}$$

Functions

A0	A1	B0	B1	Y
0	0	x	x	1
x	x	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	x	1	0
1	x	1	x	0

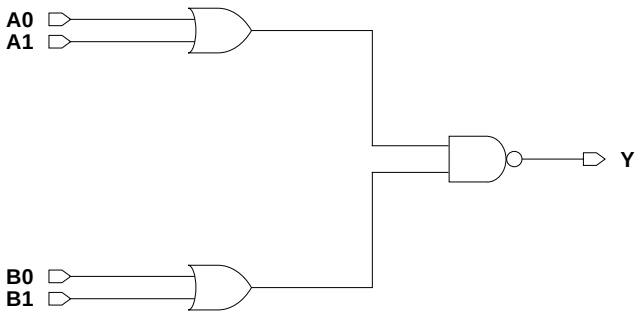
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI22XL	5.0	4.0
OAI22X1	5.0	4.0
OAI22X2	5.0	5.9
OAI22X4	5.0	9.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0156	0.0202	0.0411	0.0832
A1	0.0188	0.0256	0.0513	0.1014
B0	0.0231	0.0301	0.0577	0.1155
B1	0.0266	0.0355	0.0682	0.1336

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0034	0.0047	0.0095	0.0182
A1	0.0034	0.0046	0.0087	0.0174
B0	0.0034	0.0046	0.0092	0.0181
B1	0.0032	0.0043	0.0086	0.0175

Delays at 25^{o}C, 1.8V, Typical Process

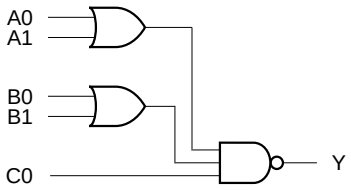
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.048	0.045	0.050	0.046	9.495	6.742	3.370	1.631
A0 → Y↓	0.030	0.028	0.032	0.031	3.910	2.720	1.395	0.701
A1 → Y↑	0.059	0.055	0.059	0.054	9.492	6.738	3.368	1.631
A1 → Y↓	0.037	0.035	0.038	0.037	3.922	2.724	1.397	0.702
B0 → Y↑	0.089	0.082	0.082	0.075	9.470	6.725	3.362	1.627
B0 → Y↓	0.043	0.040	0.042	0.040	3.917	2.723	1.397	0.701
B1 → Y↑	0.098	0.091	0.091	0.083	9.463	6.721	3.360	1.626
B1 → Y↓	0.050	0.046	0.048	0.046	3.923	2.726	1.398	0.702

Cell Description

The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet C0}$$

Logic Symbol



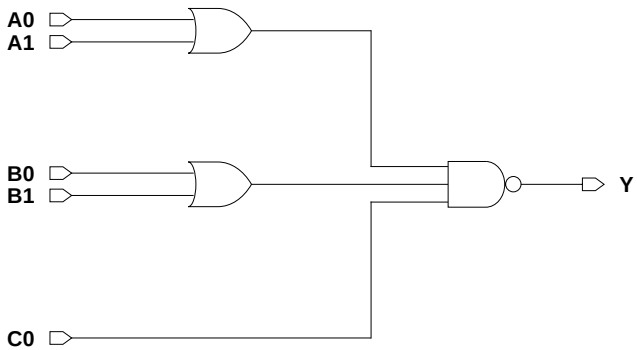
Functions

A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
x	1	x	1	1	0
x	1	1	x	1	0
1	x	x	1	1	0
1	x	1	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI221XL	5.0	4.6
OAI221X1	5.0	5.3
OAI221X2	5.0	8.6
OAI221X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0234	0.0311	0.0587	0.0730
A1	0.0262	0.0351	0.0690	0.0776
B0	0.0299	0.0402	0.0773	0.0831
B1	0.0337	0.0444	0.0846	0.0880
C0	0.0191	0.0262	0.0477	0.0664

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0051	0.0097	0.0034
A1	0.0036	0.0048	0.0097	0.0033
B0	0.0037	0.0050	0.0098	0.0033
B1	0.0034	0.0046	0.0095	0.0031
C0	0.0033	0.0043	0.0087	0.0031

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.088	0.083	0.078	0.228	9.494	6.738	3.370	1.168
A0 → Y↓	0.051	0.047	0.045	0.170	4.420	3.016	1.525	0.605
A1 → Y↑	0.099	0.092	0.087	0.238	9.489	6.737	3.368	1.168
A1 → Y↓	0.059	0.054	0.052	0.179	4.426	3.019	1.527	0.605
B0 → Y↑	0.124	0.117	0.109	0.261	9.499	6.736	3.369	1.168
B0 → Y↓	0.060	0.054	0.051	0.179	4.420	3.016	1.525	0.605
B1 → Y↑	0.133	0.125	0.118	0.271	9.497	6.735	3.368	1.168
B1 → Y↓	0.067	0.062	0.059	0.188	4.427	3.019	1.527	0.605
C0 → Y↑	0.041	0.040	0.034	0.154	6.252	4.528	2.265	1.168
C0 → Y↓	0.044	0.041	0.038	0.163	4.420	3.016	1.525	0.605

Cell Description

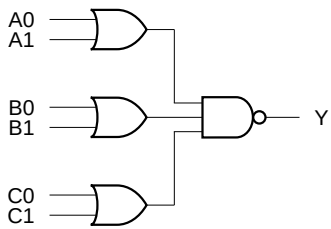
The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet (C0 + C1)}$$

Functions

A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
x	1	x	1	1	x	0
x	1	x	1	x	1	0
x	1	1	x	1	x	0
x	1	1	x	x	1	0
1	x	x	1	1	x	0
1	x	x	1	x	1	0
1	x	1	x	1	x	0
1	x	1	x	x	1	0

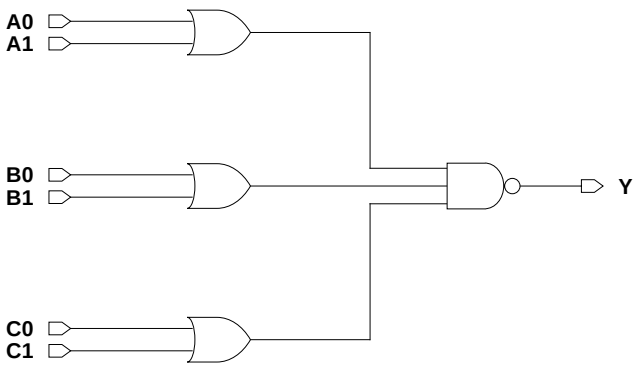
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI222XL	5.0	5.3
OAI222X1	5.0	5.9
OAI222X2	5.0	9.9
OAI222X4	5.0	7.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0303	0.0405	0.0795	0.0807
A1	0.0336	0.0442	0.0874	0.0866
B0	0.0372	0.0482	0.0973	0.0895
B1	0.0404	0.0534	0.1057	0.0936
C0	0.0208	0.0293	0.0559	0.0701
C1	0.0249	0.0326	0.0647	0.0746

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0035	0.0048	0.0098	0.0034
A1	0.0036	0.0048	0.0097	0.0033
B0	0.0037	0.0050	0.0097	0.0033
B1	0.0035	0.0047	0.0096	0.0032
C0	0.0037	0.0051	0.0097	0.0035
C1	0.0035	0.0048	0.0100	0.0033

Delays at 25°C, 1.8V, Typical Process

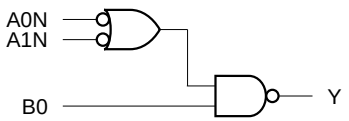
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.112	0.104	0.100	0.250	9.476	6.731	3.365	1.168
A0 → Y↓	0.068	0.062	0.059	0.193	4.428	3.020	1.512	0.605
A1 → Y↑	0.122	0.113	0.109	0.259	9.475	6.730	3.364	1.167
A1 → Y↓	0.076	0.070	0.066	0.203	4.434	3.022	1.513	0.605
B0 → Y↑	0.150	0.141	0.135	0.288	9.489	6.731	3.366	1.168
B0 → Y↓	0.076	0.069	0.066	0.201	4.429	3.020	1.512	0.605
B1 → Y↑	0.159	0.149	0.144	0.297	9.483	6.731	3.365	1.167
B1 → Y↓	0.084	0.077	0.073	0.211	4.434	3.022	1.513	0.605
C0 → Y↑	0.067	0.063	0.058	0.207	9.518	6.754	3.378	1.168
C0 → Y↓	0.049	0.045	0.042	0.175	4.423	3.017	1.510	0.605
C1 → Y↑	0.075	0.072	0.067	0.216	9.519	6.754	3.378	1.168
C1 → Y↓	0.055	0.052	0.050	0.182	4.438	3.025	1.512	0.605

Cell Description

The OAI2BB1 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet B0}$$

Logic Symbol



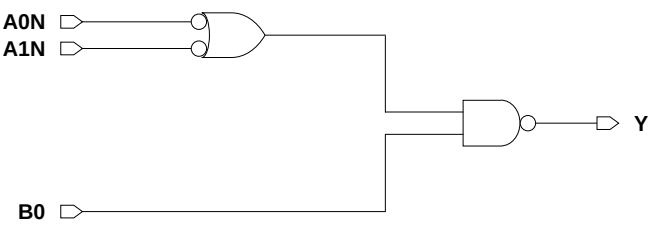
Functions

A0N	A1N	B0	Y
1	1	x	1
x	x	0	1
x	0	1	0
0	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI2BB1XL	5.0	3.3
OAI2BB1X1	5.0	3.3
OAI2BB1X2	5.0	4.6
OAI2BB1X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0205	0.0229	0.0395	0.0739
A1N	0.0176	0.0203	0.0333	0.0657
B0	0.0101	0.0138	0.0235	0.0516

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0019	0.0018	0.0033	0.0056
A1N	0.0015	0.0015	0.0026	0.0043
B0	0.0026	0.0034	0.0070	0.0126

Delays at 25°C, 1.8V, Typical Process

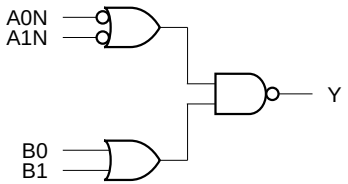
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.080	0.085	0.076	0.079	6.252	4.523	2.220	1.110
A0N → Y↓	0.100	0.111	0.099	0.091	3.952	2.746	1.372	0.694
A1N → Y↑	0.077	0.082	0.073	0.076	6.254	4.524	2.220	1.110
A1N → Y↓	0.090	0.101	0.089	0.084	3.947	2.744	1.371	0.694
B0 → Y↑	0.036	0.034	0.030	0.032	6.232	4.514	2.215	1.108
B0 → Y↓	0.025	0.024	0.022	0.024	3.914	2.725	1.363	0.691

Cell Description

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and one OR group of two non-inverted inputs (B0, B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet (B0 + B1)}$$

Logic Symbol



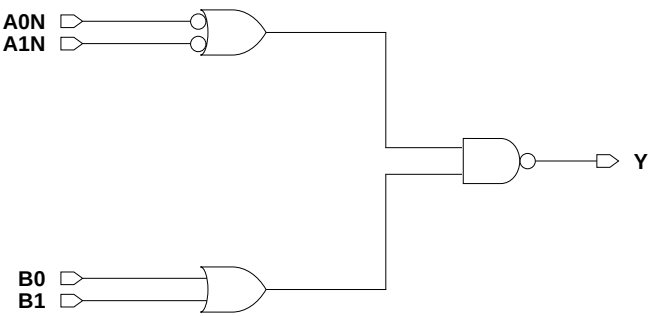
Functions

A0N	A1N	B0	B1	Y
1	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
0	x	x	1	0
0	x	1	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI2BB2XL	5.0	4.6
OAI2BB2X1	5.0	4.6
OAI2BB2X2	5.0	6.6
OAI2BB2X4	5.0	9.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0N	0.0224	0.0255	0.0471	0.0941
A1N	0.0185	0.0212	0.0387	0.0713
B0	0.0139	0.0182	0.0354	0.0634
B1	0.0171	0.0226	0.0446	0.0792

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0020	0.0019	0.0035	0.0078
A1N	0.0022	0.0022	0.0038	0.0072
B0	0.0035	0.0047	0.0095	0.0187
B1	0.0034	0.0045	0.0097	0.0176

Delays at 25°C, 1.8V, Typical Process

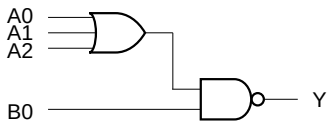
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0N → Y↑	0.083	0.088	0.087	0.081	6.261	4.530	2.264	1.113
A0N → Y↓	0.112	0.122	0.117	0.111	3.946	2.742	1.387	0.696
A1N → Y↑	0.080	0.085	0.083	0.077	6.251	4.525	2.262	1.111
A1N → Y↓	0.093	0.104	0.099	0.092	3.943	2.742	1.387	0.696
B0 → Y↑	0.070	0.064	0.061	0.055	9.472	6.725	3.363	1.627
B0 → Y↓	0.034	0.032	0.032	0.031	3.916	2.725	1.380	0.693
B1 → Y↑	0.079	0.073	0.071	0.064	9.469	6.722	3.362	1.627
B1 → Y↓	0.040	0.038	0.038	0.037	3.924	2.729	1.382	0.694

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet B0}$$

Logic Symbol



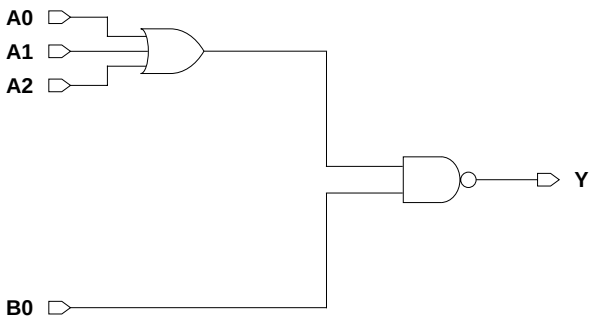
Functions

A0	A1	A2	B0	Y
0	0	0	x	1
x	x	x	0	1
x	x	1	1	0
x	1	x	1	0
1	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI31XL	5.0	4.0
OAI31X1	5.0	4.0
OAI31X2	5.0	5.9
OAI31X4	5.0	5.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0171	0.0228	0.0454	0.0758
A1	0.0213	0.0287	0.0574	0.0781
A2	0.0253	0.0333	0.0671	0.0826
B0	0.0176	0.0242	0.0460	0.0700

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0049	0.0097	0.0035
A1	0.0036	0.0048	0.0097	0.0033
A2	0.0035	0.0047	0.0100	0.0034
B0	0.0031	0.0040	0.0077	0.0029

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.084	0.077	0.077	0.253	12.246	8.497	4.249	1.109
A0 → Y↓	0.032	0.030	0.030	0.152	3.905	2.717	1.359	0.610
A1 → Y↑	0.110	0.102	0.101	0.278	12.242	8.494	4.247	1.109
A1 → Y↓	0.041	0.038	0.038	0.162	3.916	2.723	1.361	0.610
A2 → Y↑	0.116	0.108	0.108	0.286	12.240	8.496	4.248	1.109
A2 → Y↓	0.044	0.042	0.042	0.168	3.954	2.741	1.371	0.610
B0 → Y↑	0.031	0.030	0.028	0.150	6.246	4.521	2.261	1.109
B0 → Y↓	0.034	0.033	0.031	0.157	3.947	2.737	1.369	0.610

Cell Description

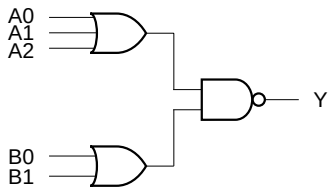
The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1)}$$

Functions

A0	A1	A2	B0	B1	Y
0	0	0	x	x	1
x	x	x	0	0	1
x	x	1	x	1	0
x	x	1	1	x	0
x	1	x	1	x	0
x	1	x	x	1	0
1	x	x	1	x	0
1	x	x	x	1	0

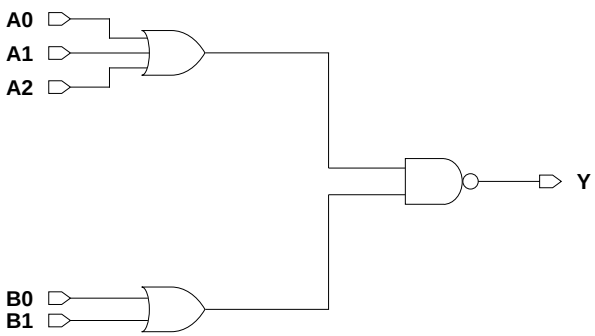
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI32XL	5.0	4.6
OAI32X1	5.0	4.6
OAI32X2	5.04	7.26
OAI32X4	5.0	6.6

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0253	0.0330	0.0661	0.0827
A1	0.0295	0.0385	0.0781	0.0900
A2	0.0333	0.0431	0.0887	0.0943
B0	0.0203	0.0273	0.0576	0.0711
B1	0.0237	0.0324	0.0689	0.0735

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0037	0.0050	0.0095	0.0034
A1	0.0037	0.0049	0.0098	0.0034
A2	0.0035	0.0048	0.0099	0.0032
B0	0.0034	0.0047	0.0087	0.0034
B1	0.0034	0.0045	0.0091	0.0032

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.117	0.105	0.104	0.289	12.252	8.499	4.247	1.109
A0 → Y↓	0.046	0.042	0.053	0.168	3.918	2.724	1.735	0.610
A1 → Y↑	0.143	0.129	0.128	0.314	12.241	8.494	4.246	1.109
A1 → Y↓	0.055	0.051	0.065	0.178	3.925	2.727	1.737	0.610
A2 → Y↑	0.150	0.135	0.136	0.321	12.241	8.495	4.245	1.109
A2 → Y↓	0.060	0.056	0.071	0.184	3.957	2.742	1.746	0.610
B0 → Y↑	0.051	0.048	0.053	0.196	9.497	6.743	3.371	1.109
B0 → Y↓	0.038	0.036	0.048	0.161	3.949	2.738	1.744	0.610
B1 → Y↑	0.062	0.057	0.063	0.206	9.490	6.740	3.370	1.109
B1 → Y↓	0.045	0.043	0.058	0.168	3.955	2.741	1.744	0.610

Cell Description

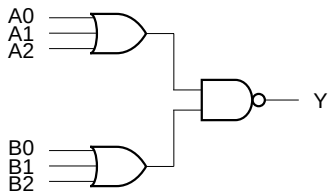
The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1 + B2)}$$

Functions

A0	A1	A2	B0	B1	B2	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
x	x	1	x	x	1	0
x	x	1	x	1	x	0
x	x	1	1	x	x	0
x	1	x	x	x	1	0
x	1	x	x	1	x	0
x	1	x	1	x	x	0
1	x	x	x	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

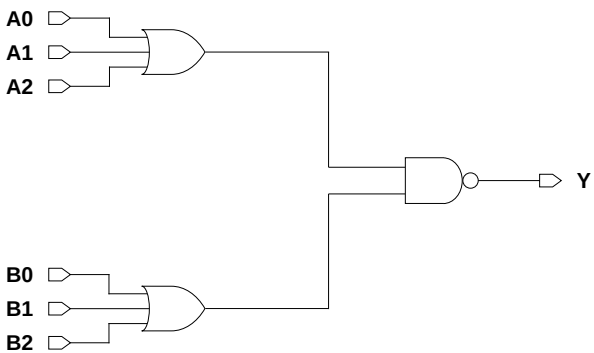
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
OAI33XL	5.0	5.3
OAI33X1	5.0	5.3
OAI33X2	5.04	8.58
OAI33X4	5.0	7.3

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A0	0.0247	0.0328	0.0650	0.0777
A1	0.0283	0.0383	0.0763	0.0833
A2	0.0320	0.0429	0.0882	0.0864
B0	0.0330	0.0432	0.0874	0.0915
B1	0.0372	0.0488	0.0996	0.0933
B2	0.0413	0.0541	0.1107	0.0981

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0038	0.0051	0.0097	0.0036
A1	0.0036	0.0050	0.0099	0.0033
A2	0.0037	0.0050	0.0108	0.0032
B0	0.0037	0.0050	0.0095	0.0035
B1	0.0036	0.0049	0.0099	0.0033
B2	0.0035	0.0048	0.0099	0.0034

Delays at 25°C, 1.8V, Typical Process

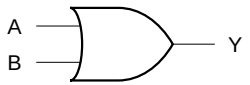
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A0 → Y↑	0.074	0.066	0.067	0.242	12.294	8.527	4.262	1.109
A0 → Y↓	0.043	0.041	0.051	0.169	3.938	2.736	1.743	0.610
A1 → Y↑	0.099	0.093	0.091	0.269	12.290	8.524	4.260	1.109
A1 → Y↓	0.052	0.051	0.063	0.178	3.947	2.738	1.744	0.610
A2 → Y↑	0.107	0.102	0.100	0.275	12.286	8.524	4.261	1.109
A2 → Y↓	0.058	0.057	0.072	0.186	3.978	2.753	1.751	0.610
B0 → Y↑	0.142	0.128	0.127	0.317	12.247	8.498	4.248	1.109
B0 → Y↓	0.057	0.054	0.068	0.184	3.954	2.744	1.745	0.610
B1 → Y↑	0.168	0.152	0.152	0.343	12.242	8.493	4.246	1.109
B1 → Y↓	0.067	0.064	0.080	0.196	3.955	2.744	1.746	0.610
B2 → Y↑	0.174	0.159	0.159	0.350	12.241	8.494	4.246	1.109
B2 → Y↓	0.072	0.069	0.088	0.201	3.981	2.756	1.753	0.610

Cell Description

The OR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A + B)$$

Logic Symbol



Functions

A	B	Y
0	0	0
x	1	1
1	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
OR2XL	5.0	2.6
OR2X1	5.0	2.6
OR2X2	5.0	2.6
OR2X4	5.0	4.0

Functional Schematic

AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0163	0.0191	0.0309	0.0553
B	0.0190	0.0214	0.0356	0.0620

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0024	0.0024	0.0035	0.0061
B	0.0024	0.0025	0.0034	0.0061

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.059	0.062	0.064	0.057
A → Y↓	0.117	0.134	0.125	0.126
B → Y↑	0.065	0.069	0.070	0.063
B → Y↓	0.130	0.146	0.135	0.136

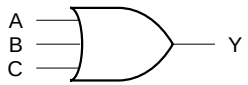
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.238	4.516	2.336	1.122
A → Y↓	3.383	2.475	1.228	0.625
B → Y↑	6.243	4.517	2.336	1.122
B → Y↓	3.384	2.474	1.228	0.625

Cell Description

The OR3 cell provides the logical OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (A + B + C)$$

Logic Symbol



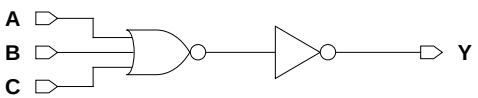
Functions

A	B	C	Y
0	0	0	0
x	x	1	1
x	1	x	1
1	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
OR3XL	5.0	3.3
OR3X1	5.0	4.0
OR3X2	5.0	4.0
OR3X4	5.04	5.94

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0170	0.0210	0.0349	0.0633
B	0.0202	0.0232	0.0410	0.0730
C	0.0215	0.0254	0.0450	0.0829

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0025	0.0025	0.0038	0.0076
B	0.0025	0.0025	0.0037	0.0079
C	0.0024	0.0024	0.0037	0.0081

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.063	0.067	0.068	0.061
A → Y↓	0.155	0.177	0.165	0.155
B → Y↑	0.070	0.074	0.077	0.070
B → Y↓	0.181	0.203	0.190	0.180
C → Y↑	0.071	0.076	0.080	0.074
C → Y↓	0.188	0.210	0.197	0.189

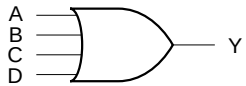
Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.238	4.516	2.277	1.057
A → Y↓	3.517	2.539	1.257	0.626
B → Y↑	6.237	4.519	2.278	1.057
B → Y↓	3.516	2.540	1.257	0.626
C → Y↑	6.246	4.520	2.279	1.058
C → Y↓	3.516	2.540	1.257	0.626

Cell Description

The OR4 cell provides the logical OR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (A + B + C + D)$$

Logic Symbol



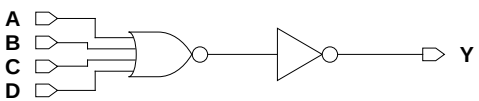
Functions

A	B	C	D	Y
0	0	0	0	0
x	x	x	1	1
x	x	1	x	1
x	1	x	x	1
1	x	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
OR4XL	5.0	4.0
OR4X1	5.0	4.0
OR4X2	5.0	4.0
OR4X4	5.04	7.26

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0191	0.0234	0.0369	0.0681
B	0.0224	0.0260	0.0416	0.0793
C	0.0249	0.0294	0.0462	0.0904
D	0.0278	0.0322	0.0523	0.1025

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0028	0.0028	0.0043	0.0084
B	0.0025	0.0025	0.0041	0.0087
C	0.0028	0.0028	0.0040	0.0088
D	0.0028	0.0028	0.0040	0.0099

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			
	XL	X1	X2	X4
A → Y↑	0.069	0.073	0.071	0.066
A → Y↓	0.187	0.215	0.182	0.178
B → Y↑	0.077	0.081	0.081	0.077
B → Y↓	0.228	0.256	0.220	0.219
C → Y↑	0.082	0.086	0.086	0.082
C → Y↓	0.253	0.282	0.243	0.239
D → Y↑	0.083	0.088	0.088	0.085
D → Y↓	0.261	0.289	0.249	0.250

Delay Table at 25°C, 1.8V, Typical Process

Description	K_{load} (ns/pF)			
	XL	X1	X2	X4
A → Y↑	6.238	4.517	2.277	1.077
A → Y↓	3.696	2.633	1.285	0.700
B → Y↑	6.242	4.519	2.278	1.077
B → Y↓	3.697	2.632	1.286	0.699
C → Y↑	6.247	4.523	2.279	1.078
C → Y↓	3.697	2.634	1.285	0.699
D → Y↑	6.262	4.527	2.284	1.080
D → Y↓	3.696	2.632	1.285	0.699

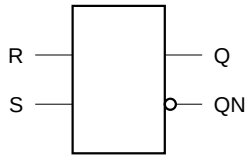
Cell Description

The RSLAT cell is an RS-type latch with active-high set (S) and reset (R).

Function

R	S	Q[n+1]	QN[n+1]
0	0	Q[n]	QN[n]
0	1	1	0
1	0	0	1
1	1	IL	IL

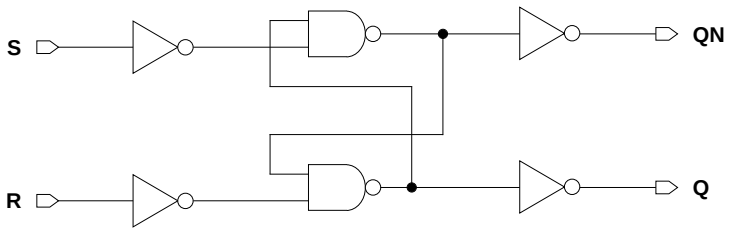
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RSLATXL	5.0	6.6
RSLATX1	5.0	6.6
RSLATX2	5.0	7.9
RSLATX4	5.0	11.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
S	0.0082	0.0090	0.0114	0.0211
R	0.0092	0.0099	0.0127	0.0224
Q	0.0338	0.0449	0.0826	0.1450

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
S	0.0020	0.0021	0.0025	0.0045
R	0.0022	0.0022	0.0026	0.0046

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
S → Q↑	0.214	0.201	0.189	0.177	6.253	4.522	2.250	1.110
R → Q↑	0.150	0.150	0.144	0.131	6.251	4.522	2.251	1.110
R → Q↓	0.146	0.138	0.131	0.124	3.350	2.441	1.211	0.610
S → QN↑	0.140	0.141	0.143	0.127	6.252	4.523	2.251	1.110
S → QN↓	0.138	0.132	0.132	0.121	3.346	2.440	1.211	0.610
R → QN↑	0.221	0.206	0.192	0.179	6.256	4.524	2.251	1.110

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
S	minpwh	0.18	0.18	0.18	0.18
R	minpwh	0.18	0.18	0.18	0.18

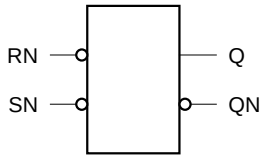
Cell Description

The RSLATN cell is an RS-type latch with active-low set (SN) and reset (RN).

Function

RN	SN	Q[n+1]	QN[n+1]
0	0	IL	IL
0	1	0	1
1	0	1	0
1	1	Q[n]	QN[n]

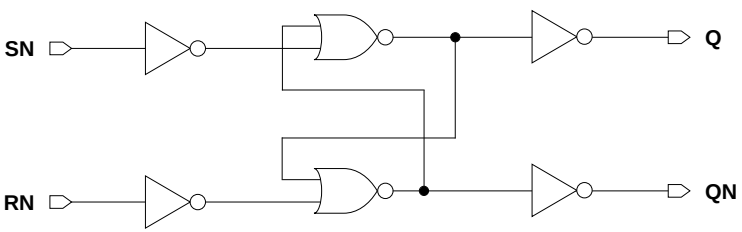
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RSLATNXL	5.0	6.6
RSLATNX1	5.0	7.3
RSLATNX2	5.0	7.3
RSLATNX4	5.0	11.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SN	0.0099	0.0111	0.0146	0.0287
RN	0.0101	0.0103	0.0159	0.0286
Q	0.0389	0.0498	0.0856	0.1488

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SN	0.0020	0.0021	0.0027	0.0049
RN	0.0022	0.0022	0.0029	0.0050

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
SN → Q↑	0.138	0.147	0.138	0.127	6.250	4.519	2.250	1.125
SN → Q↓	0.192	0.176	0.159	0.146	3.276	2.484	1.228	0.612
RN → Q↓	0.286	0.283	0.253	0.231	3.277	2.484	1.228	0.613
SN → QN↓	0.288	0.277	0.248	0.230	3.285	2.485	1.227	0.613
RN → QN↑	0.142	0.154	0.140	0.128	6.248	4.522	2.250	1.125
RN → QN↓	0.197	0.182	0.160	0.146	3.285	2.486	1.228	0.613

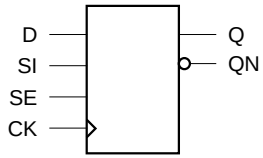
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SN	minpwl	0.18	0.18	0.18	0.18
RN	minpwl	0.18	0.18	0.18	0.18

Cell Description

The SDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Logic Symbol



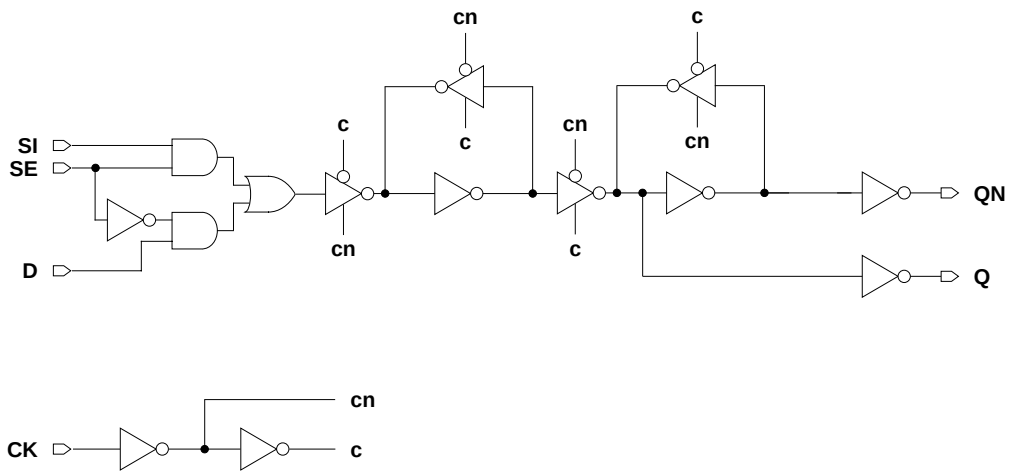
Functions

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	↑	1	0
0	x	0	↑	0	1
x	x	x	↓	Q[n]	QN[n]
x	1	1	↑	1	0
x	0	1	↑	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFXL	5.0	13.2
SDFFX1	5.0	13.9
SDFFX2	5.0	16.5
SDFFX4	5.0	19.1

Functional Schematic



AC Power

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
SI	0.0399	0.0381	0.0466	0.0749
SE	0.0468	0.0433	0.0523	0.0767
D	0.0344	0.0329	0.0415	0.0638
CK	0.0400	0.0390	0.0446	0.0621
Q	0.0208	0.0279	0.0531	0.1023

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0023	0.0021	0.0022	0.0021
SE	0.0046	0.0039	0.0041	0.0048
D	0.0028	0.0017	0.0021	0.0032
CK	0.0020	0.0027	0.0038	0.0060

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.227	0.200	0.184	0.155	5.696	4.287	2.262	1.140
CK → Q↓	0.188	0.170	0.154	0.134	3.407	2.551	1.275	0.611
CK → QN↑	0.246	0.225	0.197	0.180	6.241	4.521	2.258	1.139
CK → QN↓	0.312	0.282	0.255	0.219	3.340	2.442	1.219	0.605

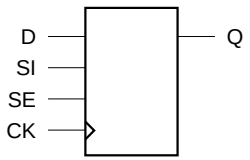
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.12	0.12	0.14	0.17
	setup↓ → CK	0.31	0.34	0.37	0.43
	hold↑ → CK	-0.10	-0.09	-0.10	-0.12
	hold↓ → CK	-0.20	-0.23	-0.24	-0.30
SE	setup↑ → CK	0.33	0.36	0.38	0.45
	setup↓ → CK	0.20	0.35	0.32	0.27
	hold↑ → CK	-0.09	-0.07	-0.09	-0.12
	hold↓ → CK	-0.09	-0.12	-0.14	-0.13
D	setup↑ → CK	0.08	0.10	0.12	0.11
	setup↓ → CK	0.20	0.35	0.31	0.27
	hold↑ → CK	-0.06	-0.07	-0.09	-0.08
	hold↓ → CK	-0.09	-0.25	-0.20	-0.16
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25

Cell Description

The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



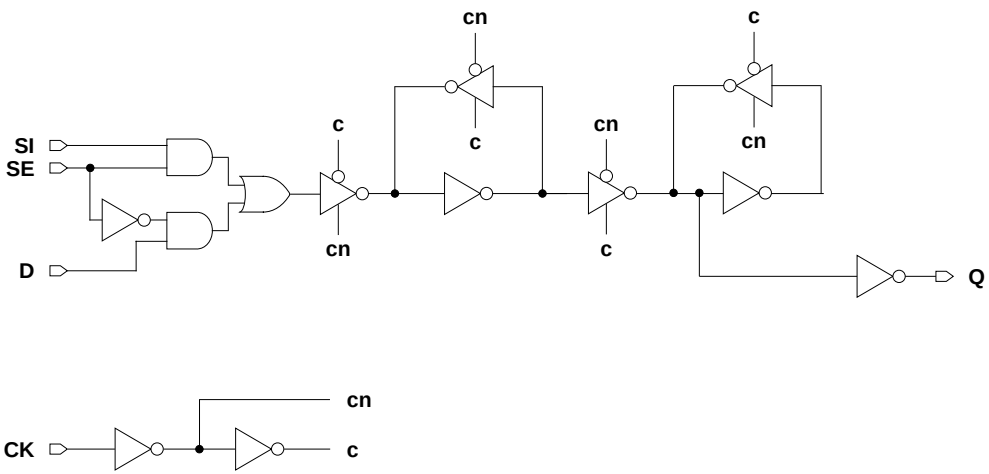
Functions

D	SI	SE	CK	Q[n+1]
1	x	0	↑	1
0	x	0	↑	0
x	x	x	↓	Q[n]
x	1	1	↑	1
x	0	1	↑	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFHQXL	5.0	13.2
SDFFHQX1	5.0	13.2
SDFFHQX2	5.0	15.8
SDFFHQX4	5.0	17.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0440	0.0476	0.0623	0.0837
SE	0.0499	0.0528	0.0696	0.0897
D	0.0387	0.0434	0.0562	0.0754
CK	0.0404	0.0406	0.0456	0.0566
Q	0.0086	0.0105	0.0225	0.0380

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0022	0.0022	0.0022	0.0021
SE	0.0044	0.0039	0.0040	0.0045
D	0.0025	0.0018	0.0020	0.0027
CK	0.0021	0.0028	0.0035	0.0050

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.207	0.175	0.174	0.148	6.252	4.282	2.261	1.118
CK → Q↓	0.209	0.167	0.162	0.136	3.518	2.594	1.298	0.611

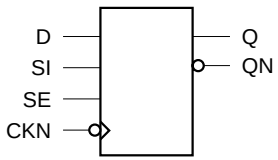
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.12	0.13	0.14	0.17
	setup↓ → CK	0.36	0.39	0.41	0.45
	hold↑ → CK	-0.09	-0.09	-0.09	-0.12
	hold↓ → CK	-0.19	-0.23	-0.25	-0.28
SE	setup↑ → CK	0.38	0.41	0.43	0.46
	setup↓ → CK	0.28	0.39	0.39	0.33
	hold↑ → CK	-0.08	-0.08	-0.08	-0.10
	hold↓ → CK	-0.11	-0.13	-0.13	-0.14
D	setup↑ → CK	0.09	0.12	0.12	0.13
	setup↓ → CK	0.28	0.40	0.39	0.33
	hold↑ → CK	-0.05	-0.08	-0.08	-0.08
	hold↓ → CK	-0.11	-0.24	-0.23	-0.17
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25

Cell Description

The SDFFN cell is a negative-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Logic Symbol



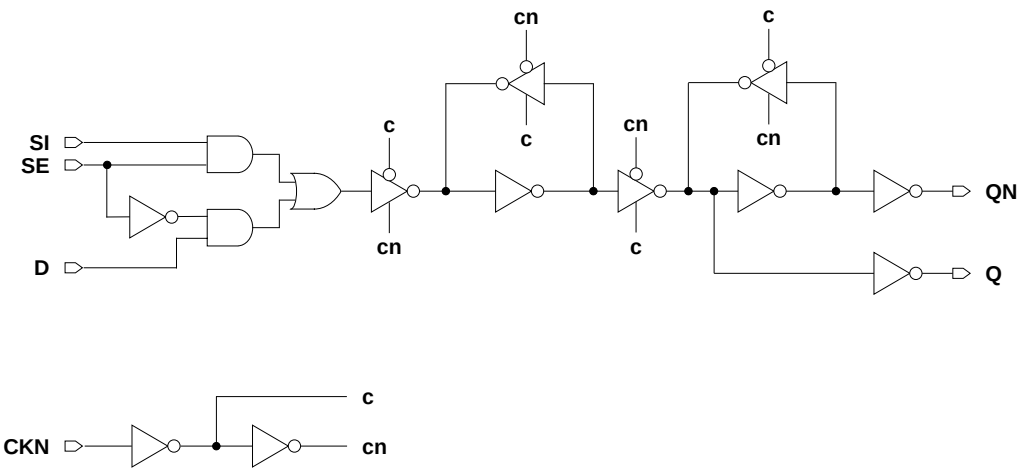
Function

D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	x	0	↓	1	0
0	x	0	↓	0	1
x	x	x	↑	Q[n]	QN[n]
x	1	1	↓	1	0
x	0	1	↓	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNXL	5.0	13.9
SDFFNX1	5.0	13.9
SDFFNX2	5.0	16.5
SDFFNX4	5.0	18.5

Functional Schematic



AC Power

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
SI	0.0404	0.0391	0.0475	0.0745
SE	0.0479	0.0444	0.0532	0.0764
D	0.0350	0.0338	0.0424	0.0634
CKN	0.0336	0.0362	0.0501	0.0758
Q	0.0372	0.0426	0.0671	0.1159

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0022	0.0020	0.0021	0.0020
SE	0.0044	0.0038	0.0039	0.0045
D	0.0025	0.0016	0.0019	0.0029
CKN	0.0020	0.0027	0.0038	0.0060

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.179	0.145	0.131	0.110	5.701	4.288	2.261	1.140
CKN → Q↓	0.299	0.263	0.241	0.205	3.406	2.552	1.276	0.612
CKN → QN↑	0.357	0.317	0.283	0.252	6.241	4.520	2.260	1.139
CKN → QN↓	0.264	0.227	0.201	0.174	3.341	2.443	1.219	0.605

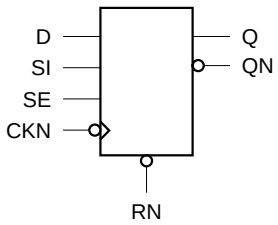
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.11	0.13	0.16	0.19
	setup↓ → CKN	0.30	0.34	0.35	0.41
	hold↑ → CKN	0.03	0.01	-0.01	-0.04
	hold↓ → CKN	-0.27	-0.29	-0.30	-0.34
SE	setup↑ → CKN	0.32	0.35	0.36	0.44
	setup↓ → CKN	0.19	0.34	0.30	0.24
	hold↑ → CKN	0.04	0.02	0.01	-0.03
	hold↓ → CKN	-0.01	-0.04	-0.05	-0.06
D	setup↑ → CKN	0.08	0.12	0.14	0.13
	setup↓ → CKN	0.18	0.34	0.30	0.24
	hold↑ → CKN	0.05	0.02	0.00	-0.01
	hold↓ → CKN	-0.16	-0.29	-0.25	-0.20
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25

Cell Description

The SDFFNR cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol



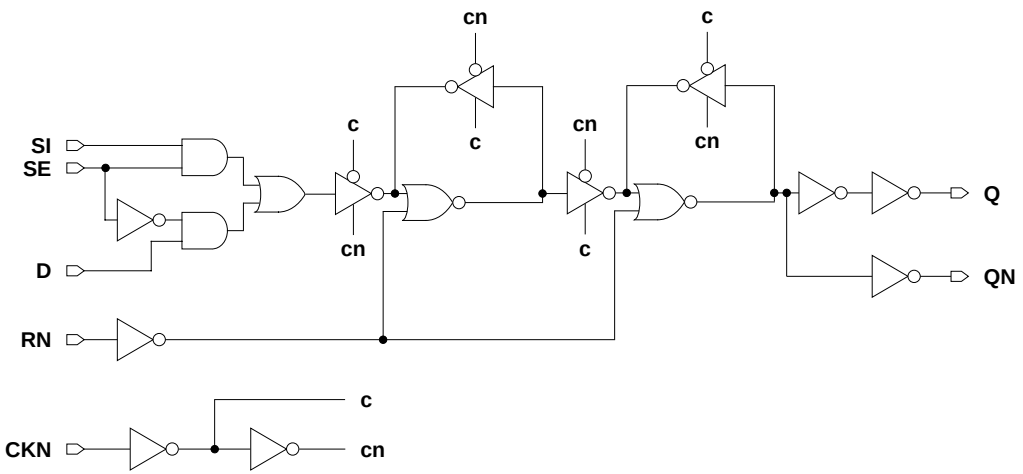
Function

RN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	x	0	↓	1	0
1	0	x	0	↓	0	1
1	x	x	x	↑	Q[n]	QN[n]
1	x	1	1	↓	1	0
1	x	0	1	↓	0	1
0	x	x	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNRXL	5.0	18.5
SDFFNRX1	5.0	17.8
SDFFNRX2	5.04	19.80
SDFFNRX4	5.0	23.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0429	0.0391	0.0457	0.0536
SE	0.0494	0.0445	0.0542	0.0590
D	0.0369	0.0334	0.0409	0.0465
CKN	0.0374	0.0366	0.0464	0.0546
RN	0.0167	0.0184	0.0216	0.0323
Q	0.0448	0.0516	0.0811	0.1348

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0019	0.0021	0.0020
SE	0.0045	0.0039	0.0043	0.0045
D	0.0026	0.0018	0.0018	0.0023
CKN	0.0022	0.0027	0.0032	0.0037
RN	0.0021	0.0026	0.0033	0.0054

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.368	0.324	0.328	0.284	6.240	4.517	2.077	1.137
CKN → Q↓	0.426	0.418	0.440	0.374	3.300	2.434	1.345	0.615
RN → Q↓	0.238	0.243	0.239	0.212	3.301	2.434	1.344	0.615
CKN → QN↑	0.375	0.353	0.362	0.305	6.237	4.516	2.078	1.138
CKN → QN↓	0.340	0.289	0.278	0.235	3.516	2.490	1.366	0.625
RN → QN↑	0.187	0.179	0.161	0.144	6.242	4.518	2.080	1.139

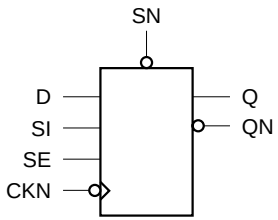
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.12	0.13	0.17	0.17
	setup↓ → CKN	0.32	0.34	0.41	0.38
	hold↑ → CKN	0.04	0.01	0.00	-0.02
	hold↓ → CKN	-0.27	-0.30	-0.35	-0.31
SE	setup↑ → CKN	0.33	0.37	0.41	0.39
	setup↓ → CKN	0.20	0.34	0.41	0.29
	hold↑ → CKN	0.05	0.02	0.02	-0.01
	hold↓ → CKN	0.00	-0.05	-0.05	-0.06
D	setup↑ → CKN	0.09	0.12	0.16	0.15
	setup↓ → CKN	0.20	0.34	0.41	0.29
	hold↑ → CKN	0.05	0.01	0.01	-0.01
	hold↓ → CKN	-0.16	-0.29	-0.34	-0.23
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.04	0.07	0.09	0.08

Cell Description

The SDFFNS cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Logic Symbol



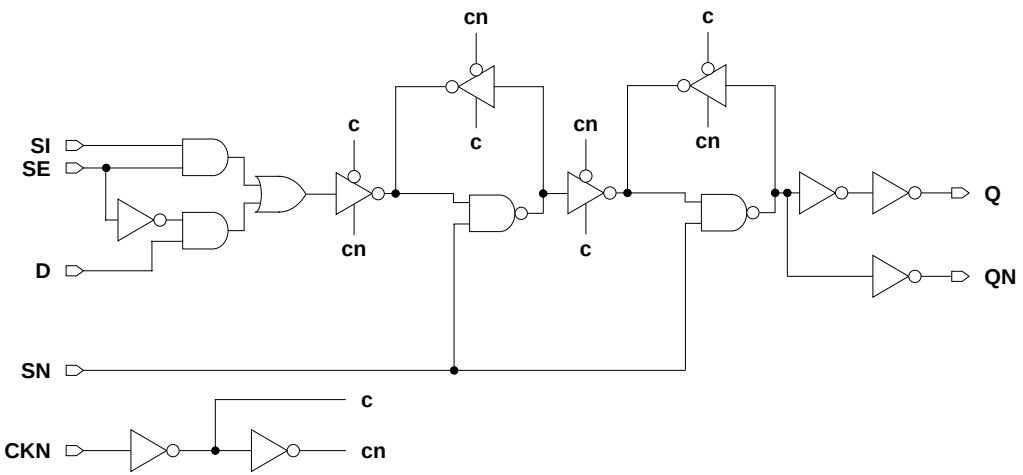
Function

SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	x	0	↓	1	0
1	0	x	0	↓	0	1
1	x	x	x	↑	Q[n]	QN[n]
1	x	1	1	↓	1	0
1	x	0	1	↓	0	1
0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNSXL	5.0	15.8
SDFFNSX1	5.0	15.8
SDFFNSX2	5.0	16.5
SDFFNSX4	5.0	21.8

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0417	0.0355	0.0389	0.0472
SE	0.0476	0.0401	0.0436	0.0518
D	0.0355	0.0307	0.0342	0.0415
CKN	0.0351	0.0339	0.0368	0.0480
SN	0.0050	0.0059	0.0092	0.0166
Q	0.0424	0.0501	0.0772	0.1334

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0019	0.0019	0.0019
SE	0.0045	0.0039	0.0039	0.0042
D	0.0025	0.0017	0.0016	0.0018
CKN	0.0020	0.0026	0.0026	0.0034
SN	0.0047	0.0052	0.0069	0.0117

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.292	0.267	0.271	0.255	6.241	4.518	2.276	1.137
CKN → Q↓	0.398	0.392	0.379	0.362	3.299	2.431	1.211	0.606
SN → Q↑	0.156	0.147	0.151	0.142	6.239	4.515	2.276	1.137
CKN → QN↑	0.350	0.330	0.311	0.294	6.253	4.522	2.279	1.139
CKN → QN↓	0.262	0.230	0.220	0.206	3.362	2.441	1.214	0.608
SN → QN↓	0.126	0.109	0.101	0.093	3.342	2.439	1.216	0.610

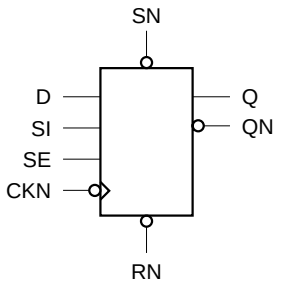
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.09	0.11	0.11	0.12
	setup↓ → CKN	0.32	0.34	0.35	0.36
	hold↑ → CKN	0.03	0.01	0.02	0.00
	hold↓ → CKN	-0.28	-0.30	-0.30	-0.31
SE	setup↑ → CKN	0.33	0.35	0.37	0.38
	setup↓ → CKN	0.19	0.33	0.35	0.30
	hold↑ → CKN	0.04	0.02	0.02	0.02
	hold↓ → CKN	0.00	-0.04	-0.04	-0.05
D	setup↑ → CKN	0.06	0.10	0.10	0.12
	setup↓ → CKN	0.20	0.34	0.35	0.30
	hold↑ → CKN	0.05	0.02	0.02	0.01
	hold↓ → CKN	-0.17	-0.30	-0.30	-0.27
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.08	-0.05	-0.05	-0.04

Cell Description

The SDFFNSR cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



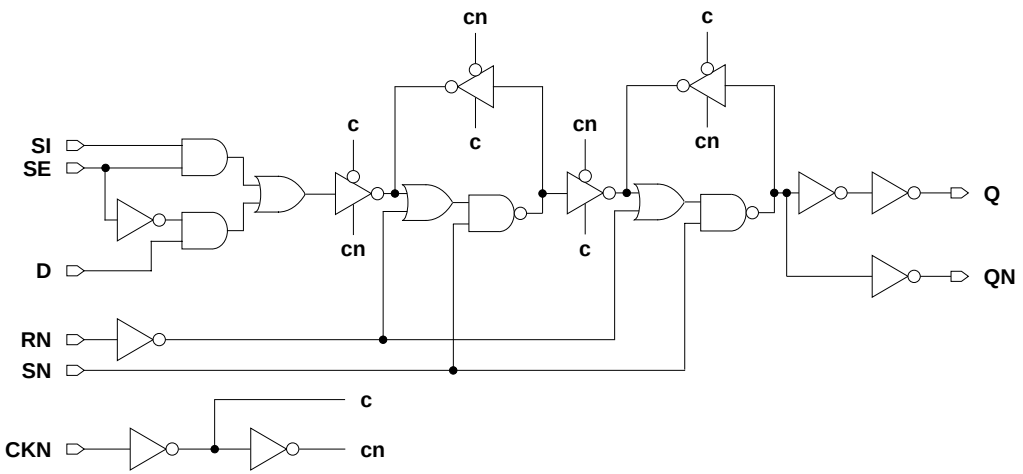
Functions

RN	SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	1	x	0	↓	1	0
1	1	0	x	0	↓	0	1
1	1	x	x	x	↑	Q[n]	QN[n]
1	1	x	1	1	↓	1	0
1	1	x	0	1	↓	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFNSRXL	5.0	19.1
SDFFNSRX1	5.0	19.1
SDFFNSRX2	5.0	19.1
SDFFNSRX4	5.0	25.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0441	0.0390	0.0443	0.0567
SE	0.0508	0.0454	0.0503	0.0627
D	0.0384	0.0337	0.0388	0.0504
CKN	0.0348	0.0346	0.0385	0.0542
SN	0.0051	0.0056	0.0092	0.0170
RN	0.0176	0.0196	0.0234	0.0402
Q	0.0450	0.0535	0.0828	0.1441

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0019	0.0018	0.0018	0.0018
SE	0.0042	0.0039	0.0040	0.0044
D	0.0021	0.0015	0.0016	0.0023
CKN	0.0022	0.0027	0.0027	0.0040
SN	0.0061	0.0066	0.0088	0.0148
RN	0.0021	0.0024	0.0035	0.0060

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CKN → Q↑	0.361	0.327	0.319	0.291	6.235	4.516	2.276	1.137
CKN → Q↓	0.425	0.421	0.389	0.366	3.311	2.437	1.211	0.610
SN → Q↑	0.182	0.171	0.166	0.156	6.237	4.517	2.276	1.137
SN → Q↓	0.186	0.179	0.160	0.155	3.312	2.437	1.211	0.610
RN → Q↓	0.277	0.266	0.229	0.223	3.312	2.437	1.211	0.610
CKN → QN↑	0.366	0.350	0.321	0.298	6.259	4.522	2.279	1.139
CKN → QN↓	0.327	0.289	0.265	0.243	3.580	2.501	1.239	0.624
SN → QN↑	0.127	0.109	0.092	0.088	6.278	4.533	2.284	1.142
SN → QN↓	0.145	0.130	0.113	0.109	3.386	2.455	1.221	0.618
RN → QN↑	0.218	0.195	0.161	0.155	6.278	4.532	2.285	1.142

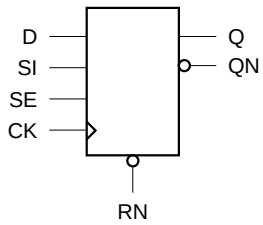
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CKN	0.16	0.19	0.18	0.19
	setup↓ → CKN	0.33	0.37	0.38	0.38
	hold↑ → CKN	0.01	-0.02	-0.02	-0.02
	hold↓ → CKN	-0.28	-0.31	-0.32	-0.31
SE	setup↑ → CKN	0.35	0.38	0.40	0.40
	setup↓ → CKN	0.26	0.38	0.36	0.27
	hold↑ → CKN	0.02	-0.01	-0.01	-0.02
	hold↓ → CKN	-0.03	-0.08	-0.07	-0.05
D	setup↑ → CKN	0.12	0.17	0.16	0.15
	setup↓ → CKN	0.26	0.38	0.36	0.27
	hold↑ → CKN	0.02	-0.02	-0.01	0.00
	hold↓ → CKN	-0.21	-0.31	-0.30	-0.22
CKN	minpwl	0.18	0.18	0.18	0.18
	minpwh	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.06	-0.03	-0.03	-0.04
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.08	0.12	0.10	0.09

Cell Description

The SDFFR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol



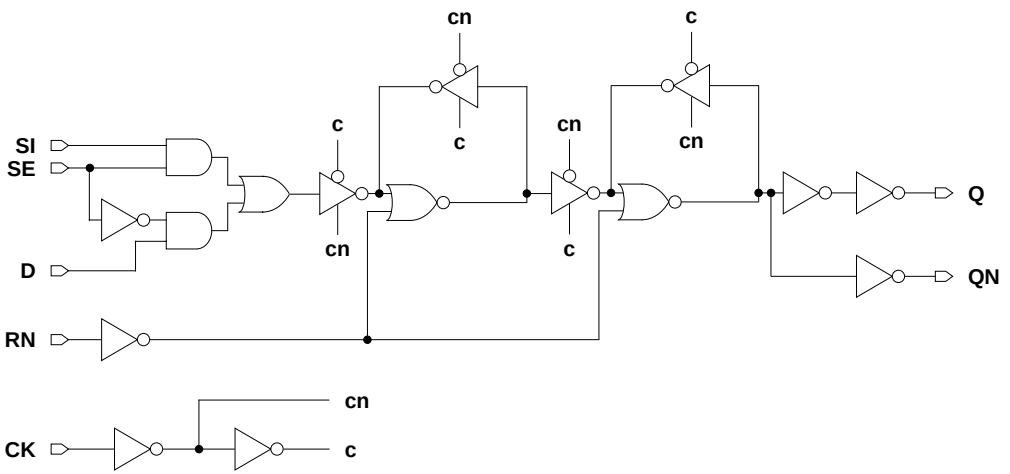
Functions

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	↑	1	0
1	0	x	0	↑	0	1
1	x	x	x	↓	Q[n]	QN[n]
1	x	1	1	↑	1	0
1	x	0	1	↑	0	1
0	x	x	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFRXL	5.0	18.5
SDFFRX1	5.0	18.5
SDFFRX2	5.04	19.80
SDFFRX4	5.0	23.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0420	0.0391	0.0443	0.0535
SE	0.0484	0.0442	0.0525	0.0590
D	0.0361	0.0334	0.0395	0.0464
CK	0.0436	0.0420	0.0481	0.0498
RN	0.0165	0.0185	0.0213	0.0313
Q	0.0282	0.0343	0.0817	0.1210

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0022	0.0023	0.0022
SE	0.0047	0.0041	0.0045	0.0047
D	0.0028	0.0020	0.0020	0.0025
CK	0.0022	0.0027	0.0032	0.0037
RN	0.0020	0.0025	0.0033	0.0054

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.412	0.382	0.388	0.335	6.239	4.516	2.077	1.137
CK → Q↓	0.291	0.315	0.307	0.272	3.300	2.434	1.344	0.615
RN → Q↓	0.238	0.243	0.238	0.211	3.301	2.434	1.345	0.615
CK → QN↑	0.240	0.250	0.228	0.203	6.237	4.516	2.078	1.138
CK → QN↓	0.384	0.347	0.340	0.283	3.517	2.490	1.471	0.625
RN → QN↑	0.187	0.179	0.161	0.143	6.241	4.519	2.079	1.138

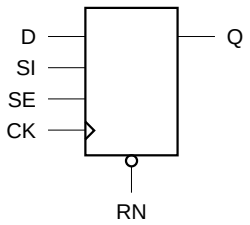
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.14	0.13	0.17	0.16
	setup↓ → CK	0.33	0.34	0.41	0.39
	hold↑ → CK	-0.12	-0.11	-0.13	-0.12
	hold↓ → CK	-0.20	-0.23	-0.28	-0.27
SE	setup↑ → CK	0.34	0.37	0.42	0.41
	setup↓ → CK	0.21	0.34	0.41	0.30
	hold↑ → CK	-0.11	-0.09	-0.12	-0.12
	hold↓ → CK	-0.09	-0.16	-0.18	-0.16
D	setup↑ → CK	0.09	0.12	0.15	0.13
	setup↓ → CK	0.21	0.34	0.41	0.30
	hold↑ → CK	-0.08	-0.09	-0.11	-0.10
	hold↓ → CK	-0.09	-0.23	-0.28	-0.19
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.03	0.05	0.08	0.05

Cell Description

The SDFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



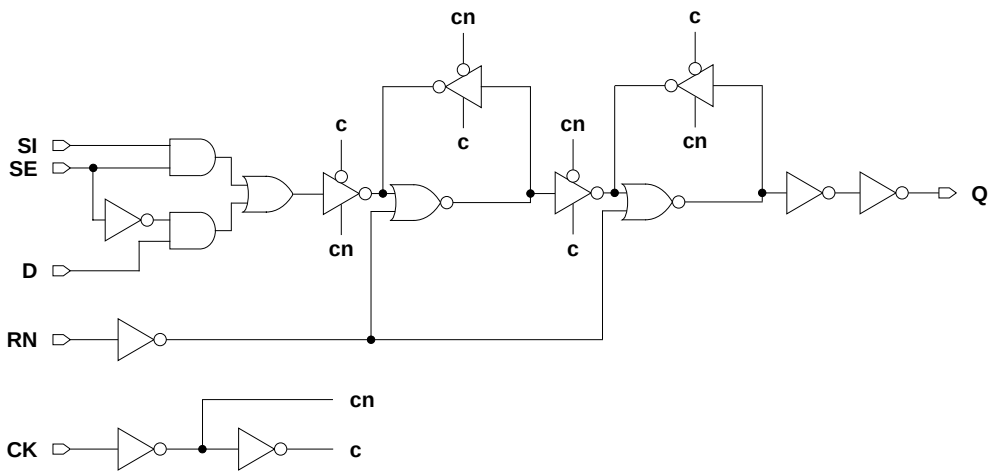
Functions

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	↑	1
1	0	x	0	↑	0
1	x	x	x	↓	Q[n]
1	x	1	1	↑	1
1	x	0	1	↑	0
0	x	x	x	x	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFRHQXL	5.0	16.5
SDFFRHQX1	5.0	16.5
SDFFRHQX2	5.0	19.8
SDFFRHQX4	5.0	24.4

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0434	0.0523	0.0756	0.1129
SE	0.0520	0.0598	0.0828	0.1146
D	0.0369	0.0465	0.0673	0.0975
CK	0.0416	0.0419	0.0496	0.0664
RN	0.0212	0.0253	0.0351	0.0543
Q	0.0136	0.0183	0.0318	0.0535

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0021	0.0021	0.0021
SE	0.0048	0.0041	0.0045	0.0052
D	0.0027	0.0019	0.0022	0.0036
CK	0.0020	0.0029	0.0039	0.0060
RN	0.0023	0.0039	0.0053	0.0093

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.236	0.196	0.172	0.158	9.483	6.726	3.364	1.832
CK → Q↓	0.251	0.175	0.151	0.139	3.620	2.467	1.225	0.676
RN → Q↓	0.171	0.137	0.117	0.096	2.885	1.941	1.081	0.646

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.16	0.18	0.21	0.23
	setup↓ → CK	0.38	0.43	0.48	0.52
	hold↑ → CK	-0.11	-0.12	-0.13	-0.14
	hold↓ → CK	-0.20	-0.25	-0.28	-0.32
SE	setup↑ → CK	0.39	0.44	0.48	0.55
	setup↓ → CK	0.27	0.41	0.38	0.31
	hold↑ → CK	-0.10	-0.10	-0.12	-0.14
	hold↓ → CK	-0.09	-0.16	-0.16	-0.14
D	setup↑ → CK	0.12	0.16	0.19	0.16
	setup↓ → CK	0.27	0.41	0.38	0.32
	hold↑ → CK	-0.07	-0.09	-0.11	-0.08
	hold↓ → CK	-0.09	-0.23	-0.20	-0.15
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.09	0.10	0.12	0.10

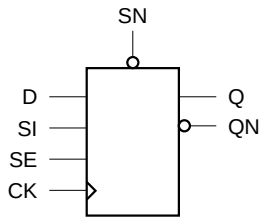
Cell Description

The SDFFS cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Functions

SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	↑	1	0
1	0	x	0	↑	0	1
1	x	x	x	↓	Q[n]	QN[n]
1	x	1	1	↑	1	0
1	x	0	1	↑	0	1
0	x	x	x	x	1	0

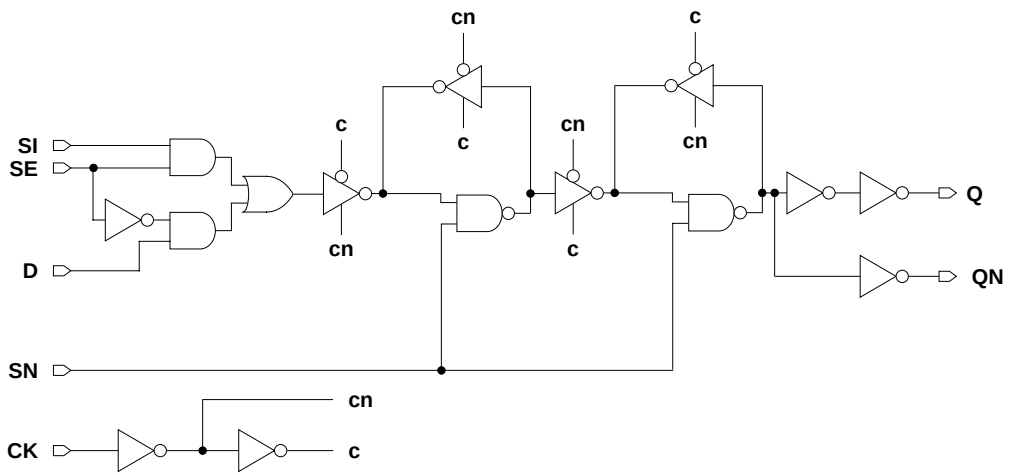
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSXL	5.0	15.8
SDFFSX1	5.0	15.8
SDFFSX2	5.0	16.5
SDFFSX4	5.0	21.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0405	0.0354	0.0390	0.0458
SE	0.0466	0.0398	0.0437	0.0501
D	0.0339	0.0298	0.0340	0.0396
CK	0.0377	0.0397	0.0430	0.0451
SN	0.0050	0.0060	0.0102	0.0169
Q	0.0283	0.0288	0.0596	0.1160

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0020	0.0020	0.0021
SE	0.0047	0.0042	0.0042	0.0044
D	0.0027	0.0017	0.0017	0.0019
CK	0.0020	0.0028	0.0028	0.0035
SN	0.0050	0.0054	0.0073	0.0125

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.329	0.311	0.329	0.306	6.239	4.516	2.248	1.109
CK → Q↓	0.274	0.292	0.293	0.268	3.299	2.432	1.210	0.609
SN → Q↑	0.156	0.142	0.152	0.141	6.239	4.517	2.248	1.109
CK → QN↑	0.226	0.234	0.223	0.200	6.254	4.721	2.251	1.111
CK → QN↓	0.299	0.278	0.279	0.258	3.361	2.696	1.215	0.611
SN → QN↓	0.126	0.108	0.102	0.094	3.341	2.695	1.217	0.614

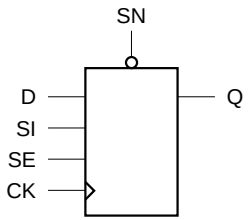
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.12	0.12	0.12	0.12
	setup↓ → CK	0.33	0.35	0.38	0.37
	hold↑ → CK	-0.10	-0.09	-0.09	-0.10
	hold↓ → CK	-0.23	-0.27	-0.27	-0.27
SE	setup↑ → CK	0.35	0.37	0.39	0.38
	setup↓ → CK	0.22	0.36	0.38	0.32
	hold↑ → CK	-0.09	-0.08	-0.08	-0.09
	hold↓ → CK	-0.11	-0.13	-0.13	-0.14
D	setup↑ → CK	0.09	0.10	0.10	0.11
	setup↓ → CK	0.22	0.36	0.38	0.32
	hold↑ → CK	-0.07	-0.08	-0.08	-0.08
	hold↓ → CK	-0.12	-0.27	-0.28	-0.22
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.02	-0.01	-0.01	0.00

Cell Description

The SDFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



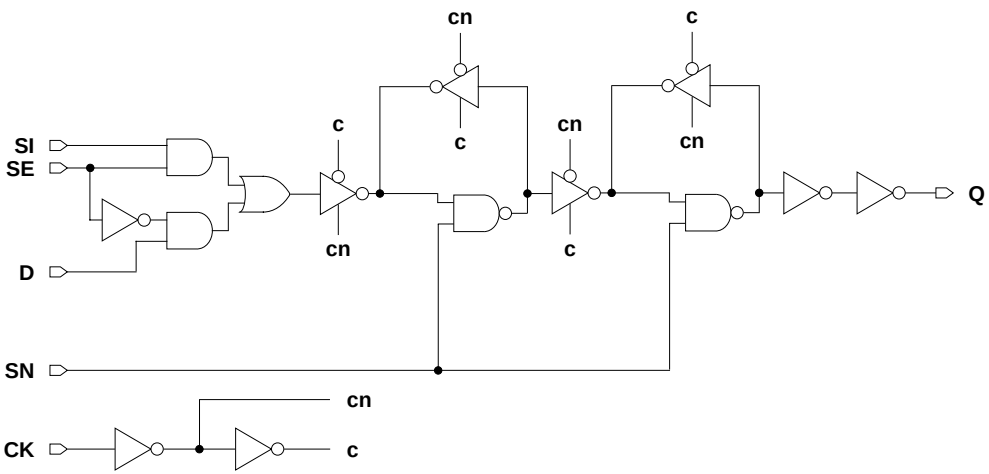
Functions

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	↑	1
1	0	x	0	↑	0
1	x	x	x	↓	Q[n]
1	x	1	1	↑	1
1	x	0	1	↑	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSHQXL	5.0	15.8
SDFFSHQX1	5.0	15.8
SDFFSHQX2	5.0	18.5
SDFFSHQX4	5.0	21.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0457	0.0507	0.0682	0.1048
SE	0.0527	0.0559	0.0739	0.1061
D	0.0392	0.0462	0.0605	0.0871
CK	0.0387	0.0394	0.0467	0.0649
SN	0.0091	0.0102	0.0173	0.0317
Q	0.0152	0.0177	0.0261	0.0513

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0023	0.0021	0.0022
SE	0.0048	0.0043	0.0044	0.0050
D	0.0027	0.0018	0.0021	0.0030
CK	0.0021	0.0028	0.0036	0.0056
SN	0.0079	0.0085	0.0135	0.0215

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.231	0.193	0.174	0.155	6.272	4.523	2.250	1.125
CK → Q↓	0.268	0.173	0.151	0.136	4.293	2.772	1.382	0.690
SN → Q↑	0.071	0.081	0.082	0.087	3.443	2.424	1.251	0.665

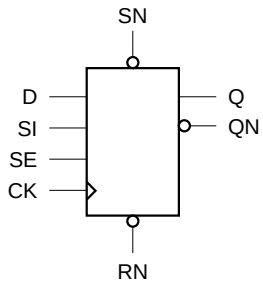
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.14	0.15	0.16	0.20
	setup↓ → CK	0.34	0.45	0.46	0.50
	hold↑ → CK	-0.11	-0.10	-0.11	-0.13
	hold↓ → CK	-0.23	-0.27	-0.28	-0.33
SE	setup↑ → CK	0.35	0.46	0.48	0.52
	setup↓ → CK	0.21	0.46	0.40	0.34
	hold↑ → CK	-0.10	-0.09	-0.10	-0.12
	hold↓ → CK	-0.12	-0.14	-0.15	-0.14
D	setup↑ → CK	0.10	0.13	0.14	0.14
	setup↓ → CK	0.22	0.46	0.40	0.34
	hold↑ → CK	-0.07	-0.08	-0.09	-0.09
	hold↓ → CK	-0.12	-0.29	-0.22	-0.17
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.02	0.05	0.06	0.06

Cell Description

The SDFFSR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



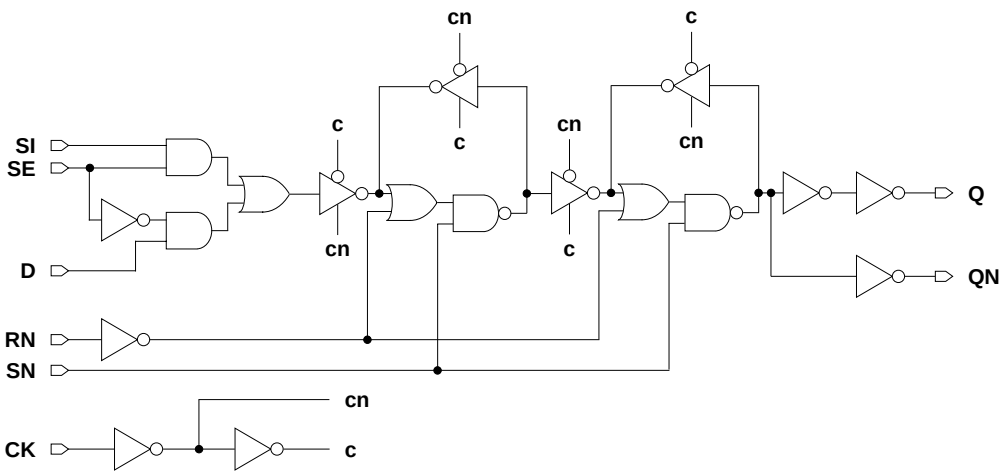
Functions

RN	SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	1	x	0	↑	1	0
1	1	0	x	0	↑	0	1
1	1	x	x	x	↓	Q[n]	QN[n]
1	1	x	1	1	↑	1	0
1	1	x	0	1	↑	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSRXL	5.0	19.1
SDFFSRX1	5.0	19.8
SDFFSRX2	5.0	19.1
SDFFSRX4	5.0	25.7

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0438	0.0376	0.0425	0.0557
SE	0.0504	0.0448	0.0495	0.0619
D	0.0380	0.0331	0.0379	0.0495
CK	0.0382	0.0375	0.0377	0.0477
SN	0.0058	0.0062	0.0098	0.0177
RN	0.0173	0.0191	0.0229	0.0400
Q	0.0312	0.0382	0.0718	0.1354

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0020	0.0019	0.0019	0.0020
SE	0.0044	0.0041	0.0042	0.0046
D	0.0023	0.0017	0.0018	0.0025
CK	0.0024	0.0029	0.0029	0.0040
SN	0.0060	0.0064	0.0087	0.0148
RN	0.0022	0.0024	0.0035	0.0060

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.402	0.368	0.366	0.341	6.237	4.514	2.276	1.137
CK → Q↓	0.307	0.319	0.285	0.275	3.310	2.437	1.211	0.610
SN → Q↑	0.181	0.171	0.166	0.156	6.233	4.514	2.276	1.137
SN → Q↓	0.185	0.178	0.160	0.155	3.311	2.437	1.211	0.610
RN → Q↓	0.276	0.264	0.228	0.223	3.311	2.437	1.211	0.610
CK → QN↑	0.248	0.248	0.216	0.207	6.260	4.524	2.279	1.139
CK → QN↓	0.369	0.330	0.312	0.293	3.577	2.501	1.239	0.624
SN → QN↑	0.127	0.109	0.091	0.088	6.276	4.531	2.283	1.142
SN → QN↓	0.144	0.130	0.112	0.109	3.386	2.455	1.220	0.618
RN → QN↑	0.218	0.194	0.159	0.155	6.275	4.531	2.283	1.142

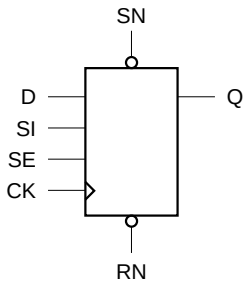
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.16	0.18	0.17	0.17
	setup↓ → CK	0.34	0.37	0.38	0.39
	hold↑ → CK	-0.12	-0.12	-0.12	-0.12
	hold↓ → CK	-0.21	-0.25	-0.25	-0.26
SE	setup↑ → CK	0.36	0.38	0.40	0.41
	setup↓ → CK	0.27	0.38	0.37	0.29
	hold↑ → CK	-0.11	-0.12	-0.11	-0.12
	hold↓ → CK	-0.15	-0.17	-0.17	-0.15
D	setup↑ → CK	0.12	0.16	0.15	0.13
	setup↓ → CK	0.27	0.38	0.36	0.29
	hold↑ → CK	-0.09	-0.11	-0.11	-0.09
	hold↓ → CK	-0.15	-0.25	-0.23	-0.16
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	-0.01	0.01	0.01	0.02
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.06	0.11	0.09	0.07

Cell Description

The SDFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol



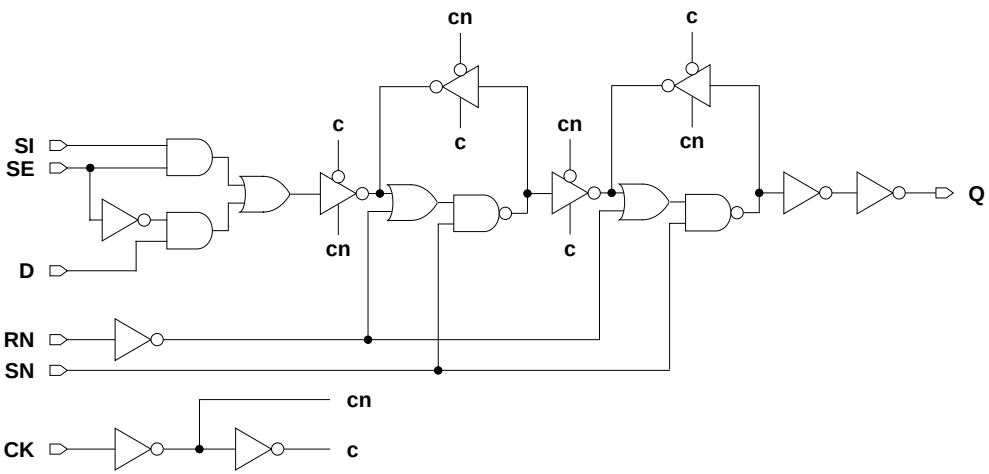
Functions

RN	SN	D	SI	SE	CK	Q[n+1]
1	1	1	x	0	↑	1
1	1	0	x	0	↑	0
1	1	x	x	x	↓	Q[n]
1	1	x	1	1	↑	1
1	1	x	0	1	↑	0
0	1	x	x	x	x	0
1	0	x	x	x	x	1
0	0	x	x	x	x	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFSRHQXL	5.0	19.8
SDFFSRHQX1	5.0	19.8
SDFFSRHQX2	5.0	25.1
SDFFSRHQX4	5.0	33.7

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0480	0.0534	0.0752	0.1225
SE	0.0537	0.0599	0.0888	0.1352
D	0.0408	0.0475	0.0711	0.1124
CK	0.0429	0.0410	0.0524	0.0735
SN	0.0092	0.0103	0.0173	0.0310
RN	0.0240	0.0267	0.0418	0.0671
Q	0.0160	0.0192	0.0365	0.0653

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0020	0.0020	0.0020	0.0021
SE	0.0054	0.0049	0.0051	0.0058
D	0.0027	0.0018	0.0026	0.0043
CK	0.0022	0.0028	0.0043	0.0064
SN	0.0105	0.0112	0.0166	0.0272
RN	0.0022	0.0035	0.0057	0.0100

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.245	0.204	0.188	0.174	9.492	6.731	3.365	1.683
CK → Q↓	0.247	0.170	0.158	0.143	4.196	2.761	1.432	0.717
SN → Q↑	0.077	0.084	0.088	0.090	4.006	2.838	1.451	0.771
SN → Q↓	0.049	0.051	0.048	0.038	3.736	2.484	1.362	0.712
RN → Q↓	0.177	0.128	0.114	0.099	3.773	2.484	1.361	0.712

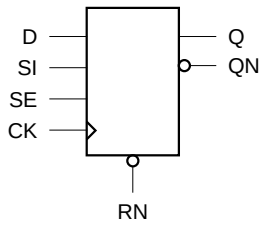
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		X1	X2	X4	X8
SI	setup↑ → CK	0.18	0.19	0.22	0.27
	setup↓ → CK	0.42	0.43	0.48	0.58
	hold↑ → CK	-0.12	-0.12	-0.13	-0.16
	hold↓ → CK	-0.22	-0.24	-0.28	-0.37
SE	setup↑ → CK	0.45	0.45	0.50	0.61
	setup↓ → CK	0.29	0.38	0.36	0.33
	hold↑ → CK	-0.10	-0.10	-0.12	-0.16
	hold↓ → CK	-0.09	-0.16	-0.16	-0.14
D	setup↑ → CK	0.13	0.17	0.18	0.17
	setup↓ → CK	0.30	0.39	0.36	0.33
	hold↑ → CK	-0.07	-0.09	-0.09	-0.08
	hold↓ → CK	-0.09	-0.21	-0.17	-0.15
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.05	0.06	0.08	0.08
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.11	0.12	0.12	0.12

Cell Description

The SDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-low reset (RN). Scan enable (SE) dominates reset (RN).

Logic Symbol



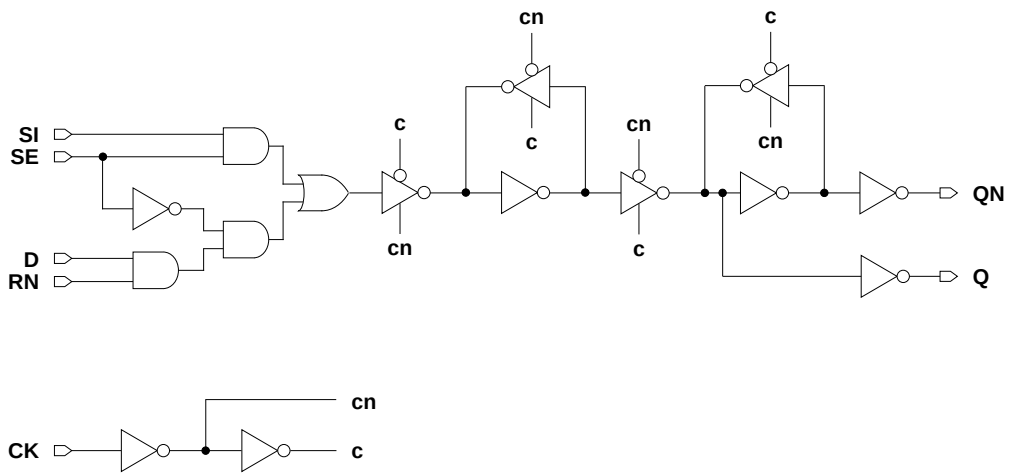
Functions

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
0	x	x	0	↑	0	1
1	0	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	x	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SDFFTRXL	5.0	14.5
SDFFTRX1	5.0	14.5
SDFFTRX2	5.0	17.2
SDFFTRX4	5.0	19.8

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0418	0.0398	0.0487	0.0753
SE	0.0495	0.0453	0.0541	0.0781
D	0.0353	0.0344	0.0427	0.0620
CK	0.0431	0.0415	0.0500	0.0664
RN	0.0392	0.0378	0.0469	0.0673
Q	0.0142	0.0220	0.0522	0.0944

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0022	0.0022	0.0021	0.0023
SE	0.0048	0.0041	0.0044	0.0052
D	0.0024	0.0017	0.0019	0.0025
CK	0.0020	0.0028	0.0039	0.0064
RN	0.0027	0.0018	0.0020	0.0038

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.218	0.192	0.193	0.157	6.246	4.520	2.250	1.110
CK → Q↓	0.179	0.160	0.150	0.137	3.185	2.631	1.225	0.617
CK → QN↑	0.225	0.207	0.206	0.186	6.242	4.518	2.249	1.109
CK → QN↓	0.286	0.265	0.267	0.227	3.328	2.441	1.213	0.610

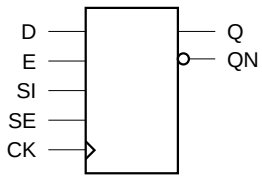
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.14	0.12	0.15	0.17
	setup↓ → CK	0.38	0.40	0.39	0.48
	hold↑ → CK	-0.12	-0.09	-0.12	-0.13
	hold↓ → CK	-0.27	-0.29	-0.27	-0.35
SE	setup↑ → CK	0.39	0.41	0.39	0.48
	setup↓ → CK	0.27	0.41	0.35	0.29
	hold↑ → CK	-0.10	-0.09	-0.10	-0.12
	hold↓ → CK	-0.15	-0.17	-0.18	-0.16
D	setup↑ → CK	0.12	0.14	0.16	0.13
	setup↓ → CK	0.24	0.40	0.34	0.27
	hold↑ → CK	-0.09	-0.11	-0.12	-0.09
	hold↓ → CK	-0.14	-0.28	-0.21	-0.16
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
RN	setup↑ → CK	0.12	0.15	0.17	0.14
	setup↓ → CK	0.29	0.45	0.38	0.31
	hold↑ → CK	-0.10	-0.12	-0.13	-0.11
	hold↓ → CK	-0.16	-0.33	-0.24	-0.20

Cell Description

The SEDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E).

Logic Symbol



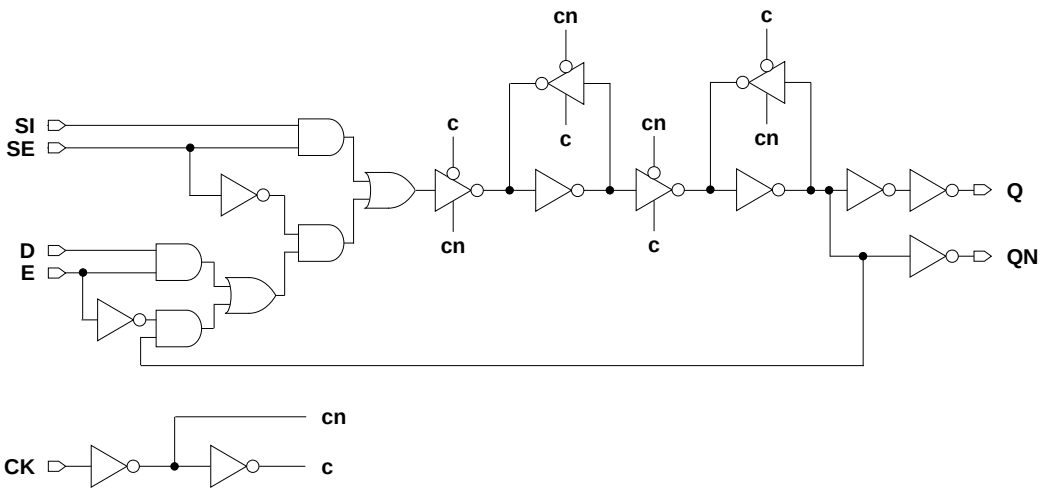
Functions

D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	1	1	↑	1	0
x	x	0	1	↑	0	1
x	0	x	0	↑	Q[n]	QN[n]
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	x	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SEDFFXL	5.0	17.8
SEDFFX1	5.0	17.8
SEDFFX2	5.0	19.8
SEDFFX4	5.0	23.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0460	0.0483	0.0619	0.0884
SE	0.0546	0.0566	0.0701	0.0981
D	0.0386	0.0421	0.0532	0.0748
CK	0.0621	0.0676	0.0849	0.1243
E	0.0528	0.0561	0.0675	0.0949
Q	0.0026	0.0061	0.0249	0.0498

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0020	0.0017	0.0021	0.0033
SE	0.0039	0.0038	0.0043	0.0050
D	0.0019	0.0017	0.0021	0.0032
CK	0.0020	0.0029	0.0039	0.0066
E	0.0047	0.0044	0.0048	0.0057

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.223	0.203	0.175	0.157	6.240	4.936	2.250	1.110
CK → Q↓	0.180	0.160	0.144	0.135	3.408	2.636	1.263	0.598
CK → QN↑	0.254	0.221	0.204	0.192	6.246	4.519	2.249	1.109
CK → QN↓	0.326	0.291	0.258	0.233	3.410	2.455	1.255	0.592

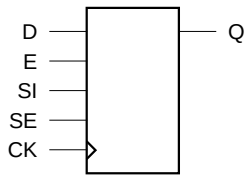
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.16	0.15	0.16	0.14
	setup↓ → CK	0.33	0.47	0.39	0.32
	hold↑ → CK	-0.14	-0.12	-0.14	-0.12
	hold↓ → CK	-0.30	-0.46	-0.37	-0.29
SE	setup↑ → CK	0.44	0.59	0.50	0.42
	setup↓ → CK	0.47	0.62	0.52	0.45
	hold↑ → CK	-0.11	-0.10	-0.12	-0.10
	hold↓ → CK	-0.22	-0.21	-0.22	-0.21
D	setup↑ → CK	0.16	0.16	0.18	0.16
	setup↓ → CK	0.42	0.56	0.47	0.41
	hold↑ → CK	-0.13	-0.12	-0.13	-0.12
	hold↓ → CK	-0.30	-0.42	-0.34	-0.29
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
E	setup↑ → CK	0.46	0.60	0.51	0.45
	setup↓ → CK	0.35	0.50	0.41	0.34
	hold↑ → CK	-0.14	-0.14	-0.15	-0.12
	hold↓ → CK	-0.20	-0.20	-0.21	-0.20

Cell Description

The SEDFFHQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q) and fast clock-to-output path.

Logic Symbol



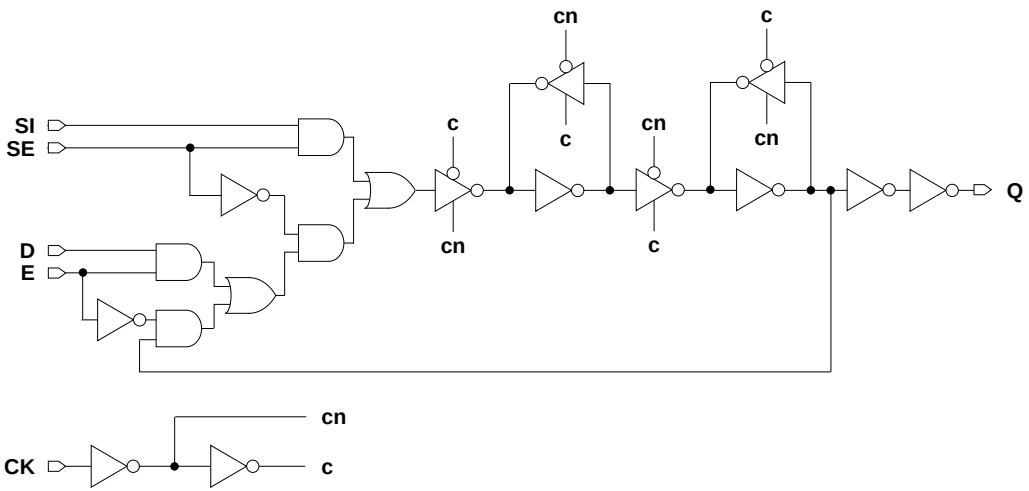
Functions

D	E	SI	SE	CK	Q[n+1]
x	x	1	1	↑	1
x	x	0	1	↑	0
x	0	x	0	↑	Q[n]
0	1	x	0	↑	0
1	1	x	0	↑	1
x	x	x	x	↓	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SEDFFHQXL	5.0	20.5
SEDFFHQX1	5.0	20.5
SEDFFHQX2	5.0	22.4
SEDFFHQX4	5.0	25.1

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0529	0.0641	0.0822	0.1202
SE	0.0742	0.0837	0.1010	0.1399
D	0.0726	0.0830	0.0999	0.1385
CK	0.0581	0.0756	0.1019	0.1488
E	0.0937	0.0984	0.1171	0.1510
Q	-0.0046	-0.0054	-0.0107	-0.0158

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0021	0.0021	0.0021	0.0021
SE	0.0020	0.0020	0.0020	0.0020
D	0.0026	0.0029	0.0029	0.0029
CK	0.0020	0.0034	0.0045	0.0064
E	0.0020	0.0021	0.0021	0.0021

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.260	0.173	0.165	0.139	6.247	4.517	2.218	1.109
CK → Q↓	0.306	0.215	0.202	0.182	3.443	2.433	1.223	0.612

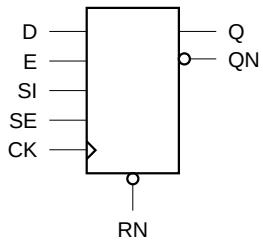
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.10	0.13	0.16	0.20
	setup↓ → CK	0.18	0.18	0.19	0.21
	hold↑ → CK	-0.09	-0.12	-0.14	-0.18
	hold↓ → CK	-0.17	-0.17	-0.18	-0.20
SE	setup↑ → CK	0.27	0.30	0.32	0.36
	setup↓ → CK	0.24	0.26	0.27	0.29
	hold↑ → CK	-0.16	-0.18	-0.20	-0.23
	hold↓ → CK	-0.13	-0.16	-0.19	-0.23
D	setup↑ → CK	0.30	0.28	0.31	0.35
	setup↓ → CK	0.30	0.26	0.27	0.30
	hold↑ → CK	-0.16	-0.16	-0.19	-0.23
	hold↓ → CK	-0.27	-0.22	-0.23	-0.25
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
E	setup↑ → CK	0.36	0.35	0.38	0.42
	setup↓ → CK	0.31	0.27	0.28	0.30
	hold↑ → CK	-0.23	-0.24	-0.27	-0.30
	hold↓ → CK	-0.12	-0.12	-0.16	-0.27

Cell Description

The SEDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), synchronous active-high enable (E) and synchronous active low reset (RN). Scan enable (SE) dominates reset (RN) and enable (E).

Logic Symbol



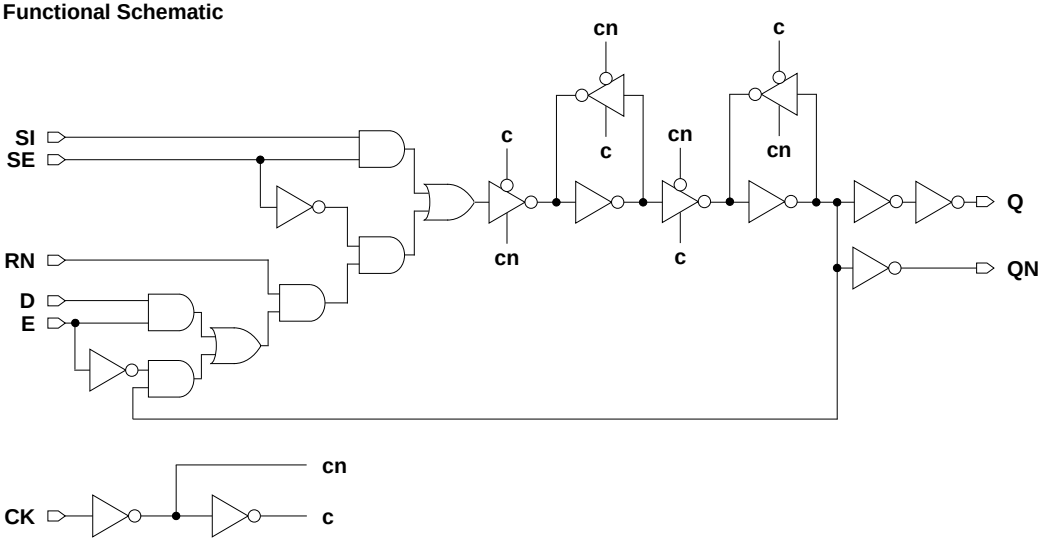
Functions

RN	D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	x	0	1	↑	0	1
x	x	x	1	1	↑	1	0
1	x	0	x	0	↑	Q[n]	QN[n]
0	x	x	x	0	↑	0	1
1	1	1	x	0	↑	1	0
1	0	1	x	0	↑	0	1
x	x	x	x	x	↓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
SEDFFTRXL	5.0	25.1
SEDFFTRX1	5.0	25.7
SEDFFTRX2	5.0	26.4
SEDFFTRX4	5.0	27.7

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
SI	0.0557	0.0692	0.0692	0.0692
SE	0.0801	0.0918	0.0918	0.0919
D	0.0727	0.0915	0.0914	0.0918
CK	0.0624	0.0865	0.0866	0.0869
E	0.0932	0.1116	0.1119	0.1107
RN	0.0510	0.0669	0.0669	0.0669
Q	0.0037	0.0017	0.0234	0.0733

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0022	0.0022	0.0022	0.0022
SE	0.0039	0.0039	0.0039	0.0039
D	0.0020	0.0030	0.0030	0.0030
CK	0.0019	0.0035	0.0035	0.0035
E	0.0020	0.0021	0.0021	0.0021
RN	0.0026	0.0026	0.0026	0.0026

Delays at 25^{o}C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	0.316	0.197	0.217	0.257	6.253	4.516	2.281	1.109
CK → Q↓	0.342	0.227	0.234	0.253	3.478	2.435	1.261	0.605
CK → QN↑	0.203	0.161	0.169	0.186	6.260	4.519	2.284	1.113
CK → QN↓	0.217	0.150	0.171	0.212	3.611	2.466	1.288	0.633

Timing Constraints at 25°C, 1.8V, Typical Process

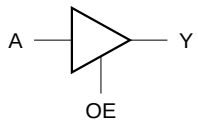
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
SI	setup↑ → CK	0.27	0.31	0.31	0.27
	setup↓ → CK	0.20	0.23	0.23	0.23
	hold↑ → CK	-0.14	-0.19	-0.18	-0.18
	hold↓ → CK	-0.19	-0.20	-0.20	-0.20
SE	setup↑ → CK	0.34	0.38	0.38	0.34
	setup↓ → CK	0.37	0.38	0.37	0.34
	hold↑ → CK	-0.20	-0.23	-0.23	-0.23
	hold↓ → CK	-0.17	-0.23	-0.23	-0.23
D	setup↑ → CK	0.37	0.35	0.35	0.31
	setup↓ → CK	0.31	0.27	0.27	0.27
	hold↑ → CK	-0.21	-0.22	-0.22	-0.22
	hold↓ → CK	-0.29	-0.23	-0.23	-0.23
CK	minpwh	0.18	0.18	0.18	0.18
	minpwl	0.25	0.25	0.25	0.25
E	setup↑ → CK	0.43	0.43	0.42	0.39
	setup↓ → CK	0.33	0.31	0.31	0.30
	hold↑ → CK	-0.30	-0.29	-0.29	-0.29
	hold↓ → CK	-0.10	-0.12	-0.14	-0.25
RN	setup↑ → CK	0.26	0.29	0.29	0.25
	setup↓ → CK	0.20	0.22	0.22	0.22
	hold↑ → CK	-0.12	-0.16	-0.16	-0.15
	hold↓ → CK	-0.18	-0.19	-0.19	-0.19

Cell Description

The TBUF cell provides the logical buffer of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



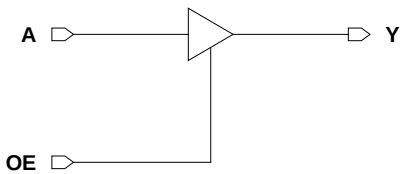
Functions

OE	A	Y
0	x	Z
1	0	0
1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TBUFXL	5.0	4.6
TBUFX1	5.0	4.6
TBUFX2	5.0	4.6
TBUFX3	5.0	5.3
TBUFX4	5.0	5.9
TBUFX8	5.0	7.9
TBUFX12	5.0	9.9
TBUFX16	5.0	11.2
TBUFX20	5.0	15.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0229	0.0251	0.0338	0.0398	0.0506	0.0922	0.1332	0.1679	0.2168
OE	0.0161	0.0168	0.0224	0.0278	0.0350	0.0690	0.0970	0.1281	0.1596

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0022	0.0022	0.0031	0.0043	0.0057	0.0115	0.0167	0.0201	0.0264
OE	0.0039	0.0041	0.0040	0.0041	0.0045	0.0066	0.0095	0.0120	0.0151
Y	0.0019	0.0024	0.0039	0.0036	0.0047	0.0093	0.0137	0.0179	0.0222

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.092	0.099	0.101	0.098	0.092	0.088	0.080	0.080	0.080
A → Y↓	0.148	0.162	0.143	0.135	0.129	0.118	0.113	0.114	0.110
OE → Y↑	0.063	0.068	0.075	0.078	0.073	0.070	0.066	0.064	0.065
OE → Y↓	0.103	0.108	0.103	0.098	0.100	0.095	0.095	0.093	0.091

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6.248	4.527	2.342	1.549	1.142	0.571	0.371	0.278	0.229
A → Y↓	4.376	2.532	1.282	0.811	0.626	0.330	0.226	0.169	0.131
OE → Y↑	6.242	4.522	2.340	1.548	1.142	0.571	0.370	0.278	0.229
OE → Y↓	4.365	2.522	1.276	0.806	0.623	0.330	0.225	0.169	0.130

Cell Description

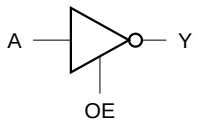
The TBUFI cell provides the logical inversion of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$$Y = \overline{A}$$

Function

OE	A	Y
0	x	Z
1	0	1
1	1	0

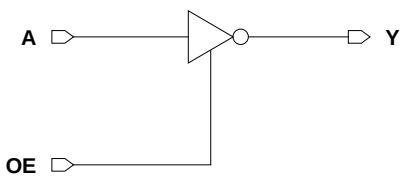
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
TBUFIXL	5.0	2.6
TBUFIX1	5.0	2.6
TBUFIX2	5.0	4.0
TBUFIX3	5.0	6.6
TBUFIX4	5.0	6.6
TBUFIX8	5.0	8.6
TBUFIX12	5.0	11.2
TBUFIX16	5.0	12.5
TBUFIX20	5.0	16.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0215	0.0217	0.0410	0.0484	0.0594	0.1079	0.1576	0.1978	0.2582
OE	0.0136	0.0137	0.0227	0.0296	0.0360	0.0675	0.1014	0.1300	0.1732

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0046	0.0046	0.0092	0.0020	0.0026	0.0046	0.0066	0.0086	0.0105
OE	0.0037	0.0037	0.0056	0.0035	0.0036	0.0049	0.0070	0.0086	0.0110
Y	0.0031	0.0031	0.0037	0.0037	0.0043	0.0090	0.0137	0.0184	0.0226

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.062	0.062	0.055	0.179	0.170	0.154	0.149	0.142	0.143
A → Y↓	0.029	0.030	0.026	0.176	0.165	0.155	0.153	0.149	0.146
OE → Y↑	0.060	0.060	0.059	0.079	0.078	0.067	0.067	0.065	0.066
OE → Y↓	0.019	0.019	0.015	0.101	0.097	0.096	0.096	0.094	0.092

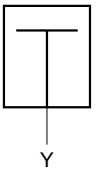
Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6.724	6.719	3.361	1.525	1.178	0.600	0.371	0.278	0.229
A → Y↓	2.665	2.722	1.362	0.813	0.634	0.299	0.214	0.159	0.123
OE → Y↑	6.750	6.731	3.366	1.523	1.177	0.600	0.370	0.278	0.229
OE → Y↓	2.661	2.723	1.363	0.809	0.631	0.298	0.213	0.159	0.122

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$Y = 1$

Logic Symbol



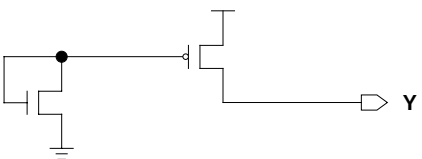
Function

Y
1

Cell Size

Drive Strength	Height (μm)	Width (μm)
TIEHI	5.0	1.3

Functional Schematic



Cell Description

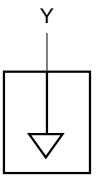
The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 0$$

Function

Y
0

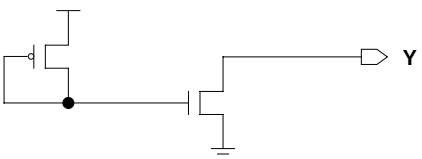
Logic Symbol



Cell Size

Drive Strength	Height (μm)	Width (μm)
TIELO	5.0	1.3

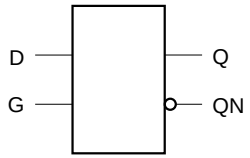
Functional Schematic



Cell Description

The TLAT cell is an active-high D-type transparent latch. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



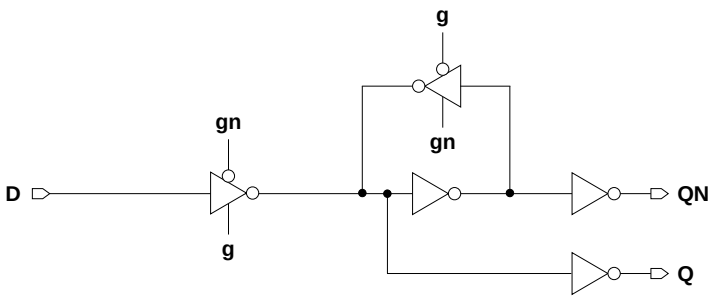
Functions

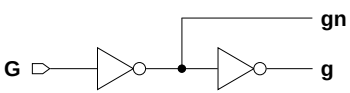
G	D	Q[n+1]	QN[n+1]
1	0	0	1
1	1	1	0
0	x	Q[n]	QN[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATXL	5.0	7.3
TLATX1	5.0	7.3
TLATX2	5.0	7.9
TLATX4	5.0	11.2

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0050	0.0061	0.0100	0.0215
G	0.0204	0.0223	0.0260	0.0414
Q	0.0311	0.0362	0.0642	0.1057

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0033	0.0041	0.0060	0.0136
G	0.0020	0.0026	0.0027	0.0045

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.089	0.086	0.079	0.070	6.248	4.522	2.278	1.153
D → Q↓	0.146	0.149	0.134	0.124	3.398	2.471	1.227	0.617
G → Q↑	0.182	0.173	0.179	0.152	6.245	4.519	2.279	1.152
G → Q↓	0.157	0.156	0.150	0.137	3.394	2.469	1.226	0.617
D → QN↑	0.193	0.201	0.200	0.193	6.244	4.520	2.277	1.152
D → QN↓	0.160	0.165	0.168	0.162	3.336	2.444	1.219	0.614
G → QN↑	0.205	0.209	0.216	0.206	6.246	4.518	2.277	1.152
G → QN↓	0.254	0.252	0.270	0.245	3.336	2.444	1.219	0.614

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	-0.02	-0.01	-0.02	-0.02
	setup↓ → G	0.09	0.10	0.08	0.08
	hold↑ → G	0.03	0.02	0.04	0.04
	hold↓ → G	-0.09	-0.09	-0.07	-0.06
G	minpwh	0.18	0.18	0.18	0.18

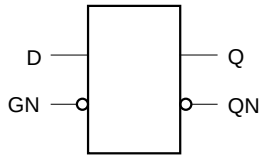
Cell Description

The TLATN cell is an active-low D-type transparent latch. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Functions

GN	D	Q[n+1]	QN[n+1]
0	0	0	1
0	1	1	0
1	x	Q[n]	QN[n]

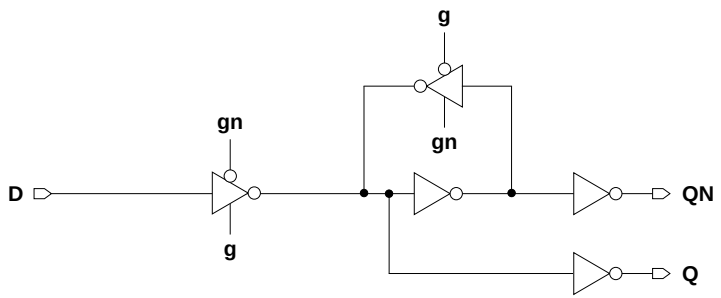
Logic Symbol

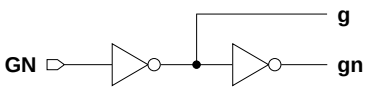


Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNXL	5.0	7.3
TLATNX1	5.0	7.3
TLATNX2	5.0	7.9
TLATNX4	5.0	11.2

Functional Schematic





AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0051	0.0063	0.0100	0.0216
GN	0.0232	0.0259	0.0316	0.0552
Q	0.0342	0.0408	0.0697	0.1133

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0034	0.0040	0.0061	0.0136
GN	0.0020	0.0025	0.0027	0.0045

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.088	0.083	0.078	0.069	6.251	4.519	2.251	1.152
D → Q↓	0.145	0.144	0.136	0.125	3.397	2.465	1.228	0.617
GN → Q↑	0.156	0.135	0.136	0.113	6.250	4.522	2.251	1.153
GN → Q↓	0.235	0.223	0.225	0.210	3.395	2.465	1.228	0.617
D → QN↑	0.193	0.197	0.202	0.195	6.247	4.518	2.249	1.152
D → QN↓	0.160	0.162	0.169	0.161	3.336	2.444	1.219	0.615
GN → QN↑	0.284	0.276	0.292	0.279	6.245	4.518	2.249	1.152
GN → QN↓	0.229	0.215	0.228	0.206	3.335	2.445	1.219	0.614

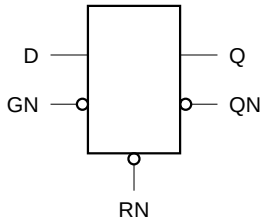
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.05	0.05	0.05	0.05
	setup↓ → GN	0.06	0.07	0.05	0.04
	hold↑ → GN	-0.04	-0.04	-0.04	-0.03
	hold↓ → GN	-0.05	-0.05	-0.03	-0.03
GN	minpwl	0.18	0.18	0.18	0.18

Cell Description

The TLATNR cell is an active-low D-type transparent latch with asynchronous active-low reset (RN). When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



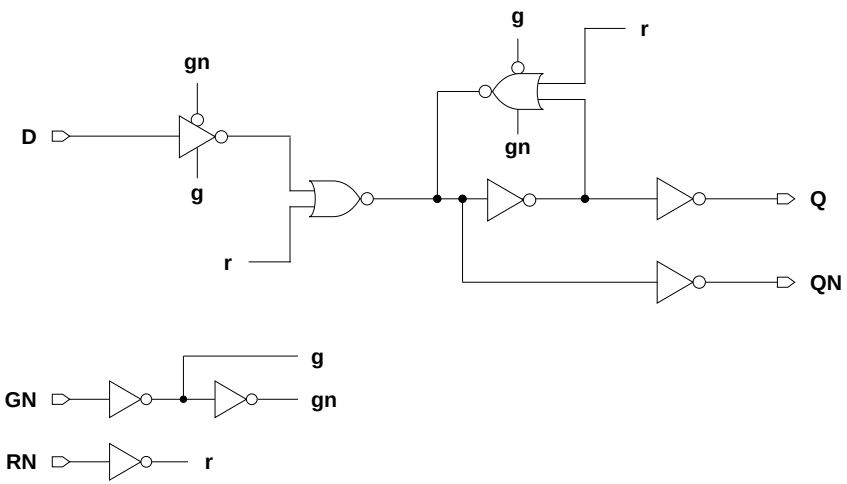
Function

RN	GN	D	Q[n+1]	QN[n+1]
1	0	0	0	1
1	0	1	1	0
1	1	x	Q[n]	QN[n]
0	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNRXL	5.0	8.6
TLATNRX1	5.0	8.6
TLATNRX2	5.0	9.2
TLATNRX4	5.0	11.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0035	0.0042	0.0075	0.0144
GN	0.0259	0.0275	0.0351	0.0585
RN	0.0039	0.0042	0.0053	0.0071
Q	0.0373	0.0455	0.0745	0.1233

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0026	0.0031	0.0052	0.0098
GN	0.0020	0.0020	0.0024	0.0036
RN	0.0038	0.0040	0.0051	0.0068

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.129	0.124	0.107	0.099	6.272	4.532	2.255	1.113
D → Q↓	0.214	0.211	0.190	0.175	3.545	2.524	1.249	0.627
GN → Q↑	0.200	0.197	0.170	0.153	6.273	4.530	2.256	1.114
GN → Q↓	0.309	0.309	0.283	0.271	3.544	2.524	1.249	0.627
RN → Q↑	0.126	0.120	0.102	0.092	6.272	4.532	2.255	1.113
RN → Q↓	0.139	0.160	0.232	0.370	3.431	2.511	1.306	0.721
D → QN↑	0.265	0.266	0.259	0.247	6.248	4.521	2.249	1.110
D → QN↓	0.208	0.210	0.202	0.199	3.353	2.452	1.220	0.615
GN → QN↑	0.361	0.365	0.352	0.343	6.248	4.521	2.249	1.110
GN → QN↓	0.280	0.284	0.265	0.253	3.354	2.453	1.220	0.615
RN → QN↑	0.193	0.214	0.303	0.458	6.247	4.519	2.248	1.110
RN → QN↓	0.206	0.207	0.196	0.192	3.354	2.452	1.220	0.615

Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.09	0.09	0.08	0.07
	setup↓ → GN	0.12	0.12	0.09	0.07
	hold↑ → GN	-0.09	-0.08	-0.06	-0.05
	hold↓ → GN	-0.11	-0.10	-0.08	-0.06
GN	minpwl	0.18	0.18	0.18	0.18
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.09	0.09	0.07	0.06

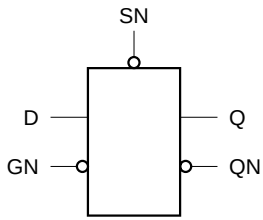
Cell Description

The TLATNS cell is an active-low D-type transparent latch with asynchronous active-low set (SN). When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Function

SN	GN	D	Q[n+1]	QN[n+1]
1	0	0	0	1
1	0	1	1	0
1	1	x	Q[n]	QN[n]
0	x	x	1	0

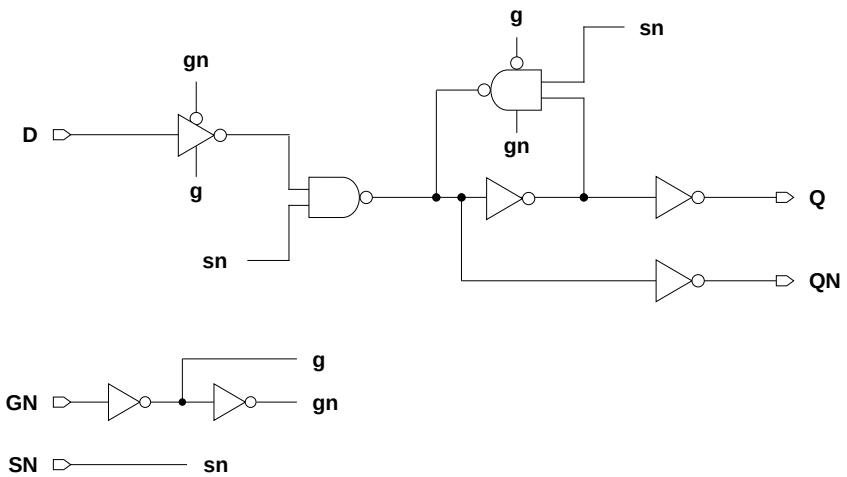
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNSXL	5.0	10.6
TLATNSX1	5.0	10.6
TLATNSX2	5.0	11.2
TLATNSX4	5.0	13.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0040	0.0049	0.0083	0.0152
GN	0.0247	0.0264	0.0310	0.0449
SN	0.0142	0.0146	0.0158	0.0220
Q	0.0468	0.0538	0.0854	0.1365

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0026	0.0031	0.0049	0.0091
GN	0.0021	0.0026	0.0027	0.0039
SN	0.0019	0.0019	0.0025	0.0037

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.134	0.125	0.108	0.102	6.279	4.533	2.255	1.113
D → Q↓	0.289	0.283	0.251	0.235	3.632	2.716	1.289	0.646
GN → Q↑	0.218	0.185	0.171	0.151	6.276	4.536	2.256	1.114
GN → Q↓	0.378	0.353	0.330	0.300	3.633	2.715	1.289	0.646
SN → Q↑	0.193	0.205	0.233	0.311	6.247	4.522	2.256	1.119
SN → Q↓	0.322	0.315	0.277	0.259	3.633	2.716	1.290	0.646
D → QN↑	0.361	0.345	0.325	0.309	6.242	4.520	2.249	1.110
D → QN↓	0.229	0.233	0.210	0.201	3.155	2.464	1.223	0.615
GN → QN↑	0.450	0.417	0.405	0.374	6.244	4.521	2.249	1.109
GN → QN↓	0.314	0.295	0.274	0.251	3.154	2.463	1.223	0.615
SN → QN↑	0.393	0.377	0.351	0.333	6.244	4.523	2.250	1.109
SN → QN↓	0.287	0.312	0.338	0.422	3.150	2.461	1.223	0.616

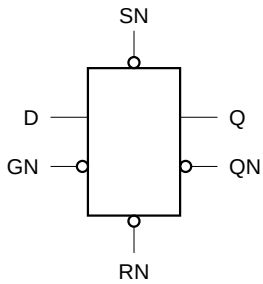
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.11	0.10	0.09	0.08
	setup↓ → GN	0.20	0.19	0.16	0.14
	hold↑ → GN	-0.10	-0.09	-0.07	-0.07
	hold↓ → GN	-0.16	-0.15	-0.12	-0.12
GN	minpwl	0.18	0.18	0.18	0.18
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.23	0.22	0.18	0.16

Cell Description

The TLATNSR cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



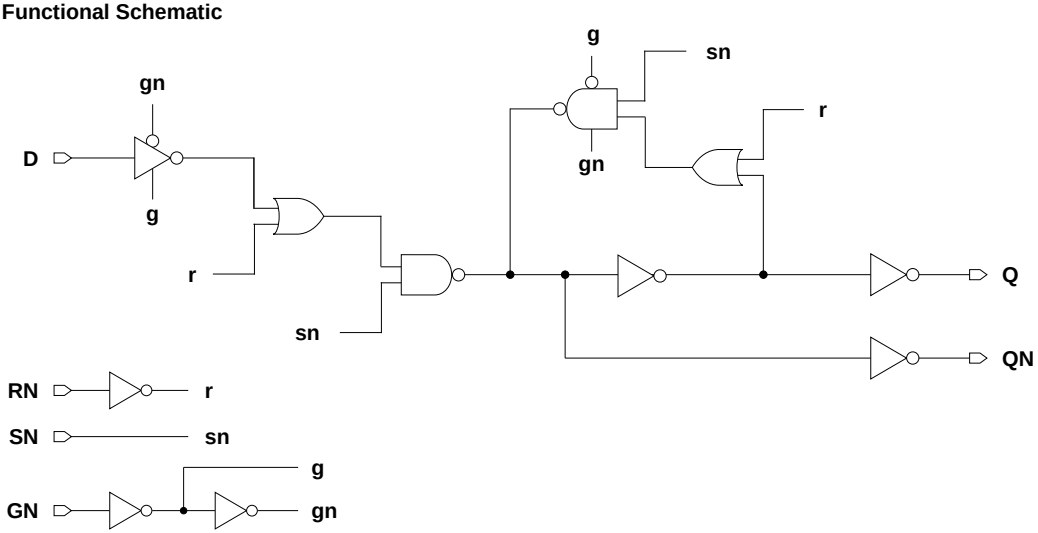
Functions

RN	SN	GN	D	Q[n+1]	QN[n+1]
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATNSRXL	5.0	11.2
TLATNSRX1	5.0	11.2
TLATNSRX2	5.0	11.9
TLATNSRX4	5.0	16.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0039	0.0048	0.0081	0.0164
GN	0.0254	0.0266	0.0341	0.0611
SN	0.0161	0.0177	0.0236	0.0445
RN	0.0048	0.0056	0.0096	0.0186
Q	0.0504	0.0596	0.0967	0.1593

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0028	0.0033	0.0051	0.0109
GN	0.0020	0.0026	0.0028	0.0041
SN	0.0020	0.0025	0.0039	0.0066
RN	0.0038	0.0042	0.0060	0.0108

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.172	0.161	0.154	0.139	6.310	4.548	2.262	1.116
D → Q↓	0.329	0.323	0.293	0.272	4.023	2.801	1.339	0.667
GN → Q↑	0.243	0.210	0.203	0.180	6.312	4.546	2.262	1.116
GN → Q↓	0.400	0.380	0.361	0.341	4.027	2.802	1.338	0.668
SN → Q↑	0.222	0.205	0.180	0.173	6.259	4.527	2.253	1.111
SN → Q↓	0.360	0.352	0.319	0.298	4.006	2.794	1.335	0.666
RN → Q↑	0.168	0.158	0.150	0.135	6.314	4.548	2.261	1.115
RN → Q↓	0.242	0.235	0.211	0.192	3.901	2.763	1.318	0.659
D → QN↑	0.400	0.387	0.368	0.346	6.246	4.520	2.249	1.110
D → QN↓	0.272	0.275	0.256	0.241	3.375	2.466	1.222	0.616
GN → QN↑	0.473	0.445	0.437	0.416	6.246	4.521	2.249	1.110
GN → QN↓	0.345	0.325	0.306	0.284	3.377	2.466	1.222	0.615
SN → QN↑	0.432	0.416	0.394	0.372	6.248	4.520	2.249	1.110
SN → QN↓	0.321	0.315	0.280	0.273	3.367	2.463	1.221	0.615
RN → QN↑	0.312	0.297	0.281	0.261	6.244	4.520	2.250	1.110
RN → QN↓	0.269	0.271	0.253	0.238	3.376	2.467	1.222	0.615

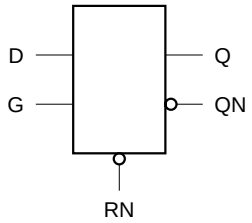
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → GN	0.15	0.14	0.12	0.12
	setup↓ → GN	0.25	0.23	0.20	0.16
	hold↑ → GN	-0.13	-0.12	-0.11	-0.10
	hold↓ → GN	-0.20	-0.20	-0.17	-0.14
GN	minpwl	0.18	0.18	0.18	0.18
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.30	0.27	0.21	0.20
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.14	0.14	0.12	0.11

Cell Description

The TLATR cell is an active-high D-type transparent latch with asynchronous active-low reset (RN). When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



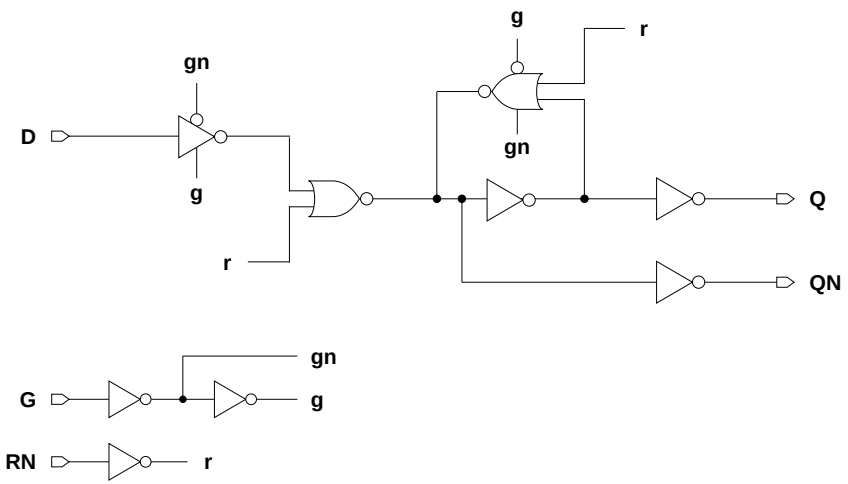
Function

RN	G	D	Q[n+1]	QN[n+1]
1	1	0	0	1
1	1	1	1	0
1	0	x	Q[n]	QN[n]
0	x	x	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATRXL	5.0	8.6
TLATRX1	5.0	8.6
TLATRX2	5.0	9.2
TLATRX4	5.0	11.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0033	0.0039	0.0074	0.0145
G	0.0250	0.0255	0.0292	0.0505
RN	0.0040	0.0040	0.0052	0.0073
Q	0.0289	0.0377	0.0693	0.1238

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0025	0.0031	0.0052	0.0099
G	0.0020	0.0021	0.0024	0.0038
RN	0.0038	0.0039	0.0051	0.0069

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.131	0.125	0.108	0.101	6.268	4.531	2.255	1.113
D → Q↓	0.215	0.212	0.190	0.174	3.552	2.527	1.249	0.627
G → Q↑	0.229	0.221	0.215	0.210	6.269	4.531	2.254	1.113
G → Q↓	0.220	0.218	0.201	0.184	3.550	2.526	1.249	0.627
RN → Q↑	0.127	0.121	0.102	0.094	6.270	4.530	2.255	1.113
RN → Q↓	0.141	0.160	0.232	0.370	3.434	2.513	1.307	0.721
D → QN↑	0.267	0.267	0.259	0.246	6.245	4.520	2.248	1.110
D → QN↓	0.210	0.211	0.203	0.201	3.353	2.451	1.220	0.615
G → QN↑	0.273	0.274	0.271	0.257	6.247	4.522	2.248	1.110
G → QN↓	0.310	0.309	0.310	0.310	3.356	2.452	1.220	0.615
RN → QN↑	0.194	0.215	0.304	0.457	6.246	4.521	2.249	1.109
RN → QN↓	0.207	0.207	0.197	0.194	3.354	2.452	1.220	0.615

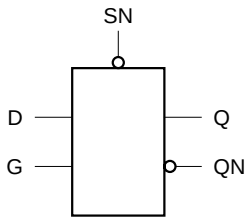
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.03	0.03	0.00	-0.01
	setup↓ → G	0.16	0.16	0.14	0.12
	hold↑ → G	0.00	0.00	0.02	0.03
	hold↓ → G	-0.16	-0.15	-0.13	-0.12
G	minpwh	0.18	0.18	0.18	0.18
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.02	0.02	-0.02	-0.02

Cell Description

The TLATS cell is an active-high D-type transparent latch with asynchronous active-low set (SN). When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



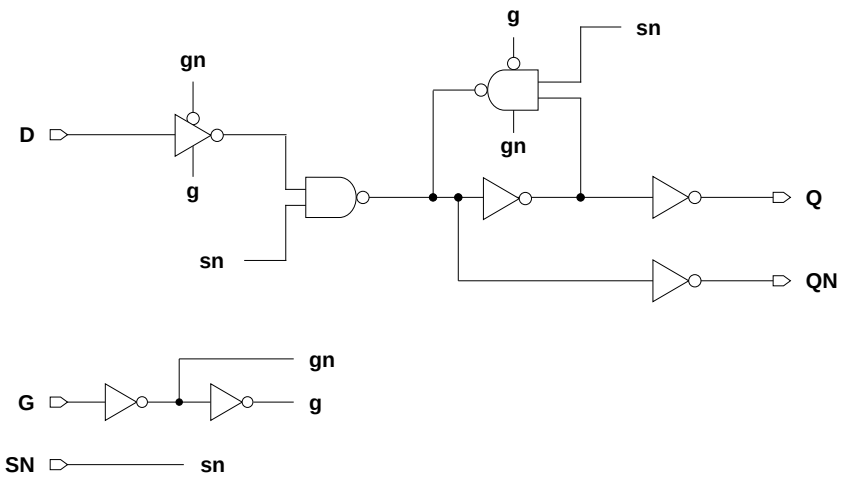
Function

SN	G	D	Q[n+1]	QN[n+1]
1	1	0	0	1
1	1	1	1	0
1	0	x	Q[n]	QN[n]
0	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATSXL	5.0	10.6
TLATSX1	5.0	10.6
TLATSX2	5.0	11.2
TLATSX4	5.0	13.9

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0040	0.0049	0.0084	0.0152
G	0.0257	0.0268	0.0292	0.0374
SN	0.0143	0.0146	0.0158	0.0221
Q	0.0386	0.0427	0.0759	0.1316

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0026	0.0031	0.0050	0.0091
G	0.0021	0.0027	0.0027	0.0040
SN	0.0020	0.0019	0.0025	0.0037

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.134	0.126	0.110	0.104	6.279	4.534	2.255	1.113
D → Q↓	0.287	0.282	0.250	0.233	3.627	2.798	1.290	0.646
G → Q↑	0.246	0.236	0.222	0.202	6.278	4.532	2.254	1.113
G → Q↓	0.266	0.257	0.237	0.219	3.628	2.798	1.289	0.646
SN → Q↑	0.192	0.203	0.233	0.311	6.244	4.523	2.256	1.119
SN → Q↓	0.320	0.314	0.276	0.257	3.629	2.798	1.290	0.646
D → QN↑	0.359	0.343	0.325	0.307	6.244	4.520	2.250	1.110
D → QN↓	0.229	0.234	0.212	0.203	3.156	2.464	1.223	0.615
G → QN↑	0.339	0.319	0.312	0.294	6.246	4.520	2.250	1.110
G → QN↓	0.343	0.346	0.325	0.301	3.155	2.464	1.223	0.615
SN → QN↑	0.392	0.375	0.352	0.332	6.245	4.520	2.250	1.110
SN → QN↓	0.287	0.311	0.339	0.422	3.151	2.464	1.224	0.616

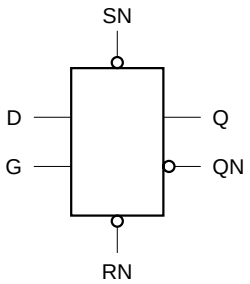
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.01	0.02	-0.01	-0.01
	setup↓ → G	0.23	0.22	0.20	0.18
	hold↑ → G	0.00	-0.01	0.02	0.02
	hold↓ → G	-0.22	-0.21	-0.18	-0.16
G	minpwh	0.18	0.18	0.18	0.18
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.27	0.26	0.22	0.20

Cell Description

The TLATSR cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



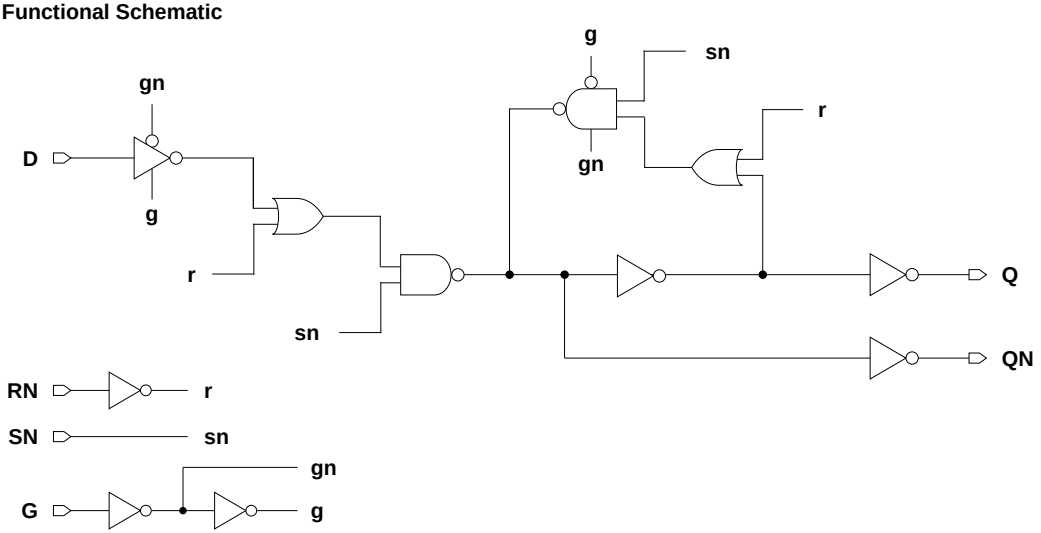
Functions

RN	SN	G	D	Q[n+1]	QN[n+1]
1	1	1	0	0	1
1	1	1	1	1	0
1	1	0	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
TLATSRXL	5.0	11.2
TLATSRX1	5.0	11.2
TLATSRX2	5.0	11.9
TLATSRX4	5.0	16.5

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0039	0.0048	0.0081	0.0164
G	0.0278	0.0278	0.0296	0.0520
SN	0.0161	0.0178	0.0239	0.0447
RN	0.0047	0.0056	0.0095	0.0185
Q	0.0426	0.0510	0.0904	0.1524

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0028	0.0033	0.0051	0.0109
G	0.0020	0.0025	0.0028	0.0041
SN	0.0020	0.0025	0.0039	0.0067
RN	0.0038	0.0042	0.0060	0.0109

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.173	0.164	0.155	0.140	6.311	4.548	2.262	1.116
D → Q↓	0.330	0.326	0.293	0.271	4.029	2.808	1.338	0.667
G → Q↑	0.273	0.258	0.251	0.228	6.312	4.546	2.261	1.115
G → Q↓	0.321	0.313	0.281	0.260	4.030	2.808	1.339	0.668
SN → Q↑	0.222	0.206	0.180	0.172	6.260	4.529	2.253	1.112
SN → Q↓	0.362	0.355	0.318	0.296	4.012	2.801	1.335	0.666
RN → Q↑	0.169	0.160	0.151	0.137	6.311	4.547	2.263	1.116
RN → Q↓	0.243	0.238	0.211	0.192	3.906	2.765	1.319	0.659
D → QN↑	0.402	0.389	0.370	0.345	6.242	4.519	2.249	1.110
D → QN↓	0.273	0.276	0.259	0.242	3.375	2.466	1.222	0.615
G → QN↑	0.394	0.377	0.360	0.334	6.247	4.520	2.250	1.110
G → QN↓	0.375	0.372	0.357	0.331	3.377	2.467	1.222	0.615
SN → QN↑	0.433	0.418	0.396	0.371	6.245	4.521	2.250	1.110
SN → QN↓	0.322	0.316	0.282	0.272	3.367	2.463	1.222	0.615
RN → QN↑	0.313	0.299	0.283	0.261	6.243	4.521	2.250	1.110
RN → QN↓	0.269	0.273	0.256	0.239	3.376	2.467	1.223	0.615

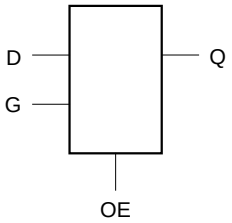
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	0.06	0.08	0.05	0.02
	setup↓ → G	0.27	0.27	0.24	0.21
	hold↑ → G	-0.03	-0.05	-0.02	0.00
	hold↓ → G	-0.26	-0.25	-0.22	-0.20
G	minpwh	0.18	0.18	0.18	0.18
SN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.32	0.30	0.26	0.24
RN	minpwl	0.50	0.50	0.50	0.50
	recovery	0.05	0.06	0.03	0.01

Cell Description

The TTLAT cell is an active-high D-type transparent latch with active-high output enable (OE). When the enable (G) is high and the output enable (OE) is high, data is transferred to the output (Q).

Logic Symbol



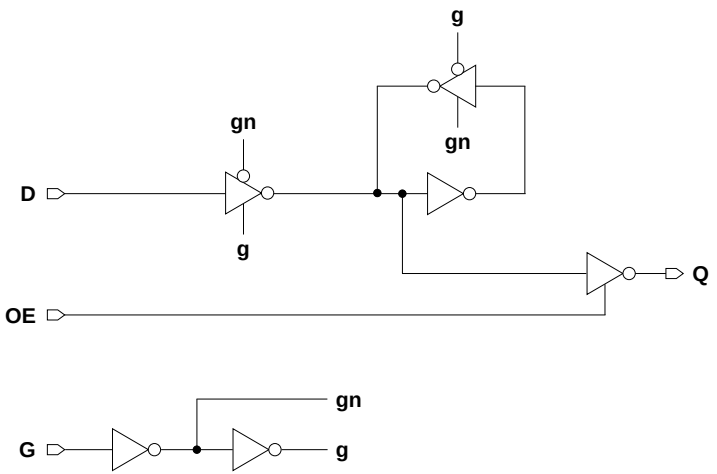
Function

OE	G	D	Q[n+1]
0	x	x	Z
1	1	0	0
1	1	1	1
1	0	x	Q[n]

Cell Size

Drive Strength	Height (µm)	Width (µm)
TTLATXL	5.0	8.6
TTLATX1	5.0	8.6
TTLATX2	5.0	12.5
TTLATX4	5.0	15.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
D	0.0049	0.0099	0.0186	0.0187
G	0.0238	0.0245	0.0372	0.0525
OE	0.0340	0.0571	0.1055	0.1668
Q	0.0261	0.0571	0.1060	0.1575

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0034	0.0061	0.0113	0.0113
G	0.0020	0.0026	0.0041	0.0067
OE	0.0025	0.0032	0.0055	0.0097
Q	0.0020	0.0043	0.0047	0.0089

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
D → Q↑	0.118	0.101	0.103	0.113	8.134	2.678	1.394	0.718
D → Q↓	0.175	0.147	0.146	0.179	5.085	1.629	0.808	0.460
G → Q↑	0.216	0.198	0.198	0.180	8.139	2.679	1.394	0.719
G → Q↓	0.191	0.163	0.162	0.185	5.081	1.627	0.807	0.460
OE → Q↑	0.028	0.023	0.017	0.021	8.065	2.637	1.372	0.708
OE → Q↓	0.016	0.016	0.012	0.014	4.994	1.586	0.786	0.445

Timing Constraints at 25°C, 1.8V, Typical Process

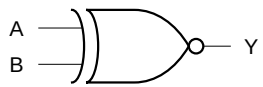
Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → G	-0.02	-0.02	-0.03	0.01
	setup↓ → G	0.10	0.08	0.08	0.12
	hold↑ → G	0.04	0.04	0.05	0.01
	hold↓ → G	-0.08	-0.06	-0.06	-0.09
G	minpwh	0.18	0.18	0.18	0.18

Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet B) + (\bar{A} \bullet \bar{B})$$

Logic Symbol



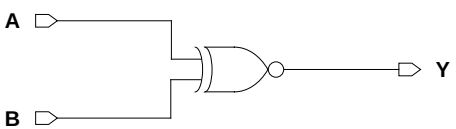
Functions

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
XNOR2XL	5.0	5.3
XNOR2X1	5.0	5.3
XNOR2X2	5.0	7.3
XNOR2X4	5.0	11.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0349	0.0378	0.0641	0.1150
B	0.0357	0.0512	0.0995	0.1814

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0058	0.0054	0.0085	0.0152
B	0.0021	0.0064	0.0141	0.0266

Delays at 25°C, 1.8V, Typical Process

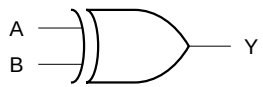
Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.131	0.126	0.131	0.118	6.246	4.522	2.249	1.214
A → Y↓	0.124	0.111	0.101	0.103	3.500	2.466	1.221	0.576
B → Y↑	0.183	0.124	0.107	0.105	6.252	4.520	2.249	1.214
B → Y↓	0.192	0.139	0.123	0.122	3.493	2.474	1.226	0.578

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet \bar{B}) + (\bar{A} \bullet B)$$

Logic Symbol



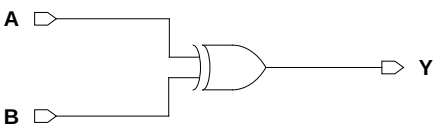
Functions

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
XOR2XL	5.0	5.3
XOR2X1	5.0	5.3
XOR2X2	5.0	6.6
XOR2X4	5.0	11.2

Functional Schematic



AC Power

Pin	Power (µW/MHz)			
	XL	X1	X2	X4
A	0.0345	0.0355	0.0612	0.1054
B	0.0344	0.0487	0.0987	0.1681

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0058	0.0054	0.0084	0.0162
B	0.0022	0.0064	0.0141	0.0266

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
A → Y↑	0.130	0.117	0.122	0.105	6.251	4.516	2.248	1.213
A → Y↓	0.125	0.114	0.113	0.107	3.255	2.474	1.226	0.578
B → Y↑	0.177	0.121	0.106	0.101	6.248	4.518	2.250	1.214
B → Y↓	0.183	0.140	0.127	0.124	3.256	2.474	1.226	0.578

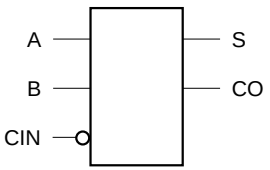
Cell Description

The AFHCIN cell is a full adder that provides the arithmetic sum (S) and carry-out (CO) of two operands (A, B) with active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus \overline{CIN}$$

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol



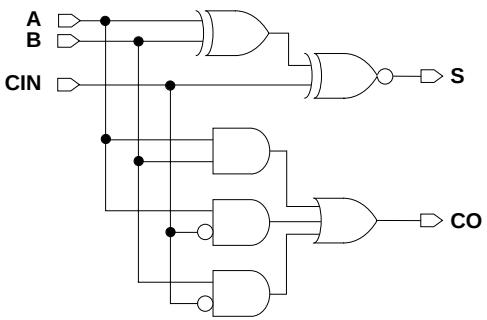
Functions

A	B	CIN	S	CO
0	0	0	1	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
AFHCINX2	5.04	16.50
AFHCINX4	5.04	18.48

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1714	0.1933
B	0.1796	0.1990
CIN	0.1234	0.1799

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0072	0.0072
B	0.0176	0.0155
CIN	0.0135	0.0265

Delays at 25°C, 3.3V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.245	0.261	2.876	2.261
A → S↓	0.292	0.314	1.406	1.281
B → S↑	0.220	0.236	2.877	2.262
B → S↓	0.220	0.241	1.405	1.281
CIN → S↑	0.140	0.124	2.876	2.261
CIN → S↓	0.156	0.157	1.410	1.282
A → CO↑	0.174	0.200	3.030	3.021
A → CO↓	0.214	0.250	1.902	1.876
B → CO↑	0.132	0.153	3.009	3.014
B → CO↓	0.181	0.214	1.882	1.868
CIN → CO↑	0.052	0.046	2.785	1.400
CIN → CO↓	0.042	0.041	1.662	0.837

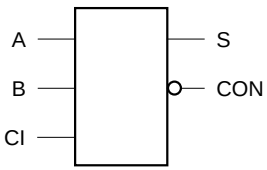
Cell Description

The AFHCON cell is a full adder that provides the arithmetic sum (S) and active-low carry-out (CON) of two operands (A, B) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus B \oplus CI$$

$$CON = \overline{(A \bullet B) + (A \bullet CI) + (B \bullet CI)}$$

Logic Symbol



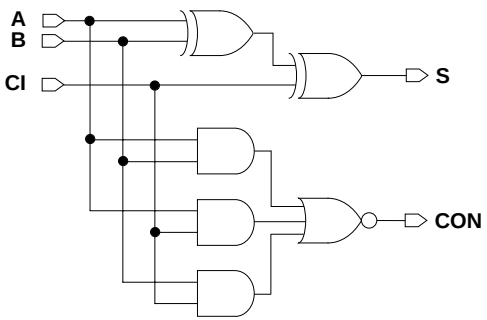
Functions

A	B	CI	S	CON
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AFHCONX2	5.04	15.84
AFHCONX4	5.04	17.16

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1822	0.2036
B	0.1658	0.1854
CI	0.1194	0.1721

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0071	0.0072
B	0.0213	0.0224
CI	0.0135	0.0270

Delays at 25°C, 3.3V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.237	0.253	2.876	2.873
A → S↓	0.275	0.290	1.611	1.599
B → S↑	0.168	0.175	2.877	2.872
B → S↓	0.191	0.208	1.611	1.599
CI → S↑	0.135	0.122	2.874	2.873
CI → S↓	0.151	0.157	1.612	1.600
A → CON↑	0.225	0.249	3.128	2.990
A → CON↓	0.187	0.219	1.935	1.857
B → CON↑	0.150	0.172	3.169	3.010
B → CON↓	0.118	0.147	1.952	1.866
CI → CON↑	0.067	0.052	2.778	1.366
CI → CON↓	0.046	0.039	1.657	0.830

Cell Description

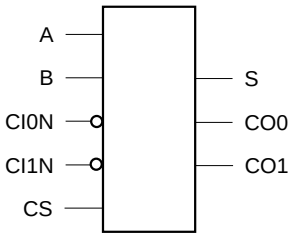
The AFCSHCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carry-outs (CO0, CO1) of the operands (A,B) with active-low carry-ins (CI0N, CI1N).The three outputs (S, CO0, CO1) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus \overline{CI1N}) + \overline{CS} \bullet (A \oplus B \oplus \overline{CI0N})$$

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol



Cell Size

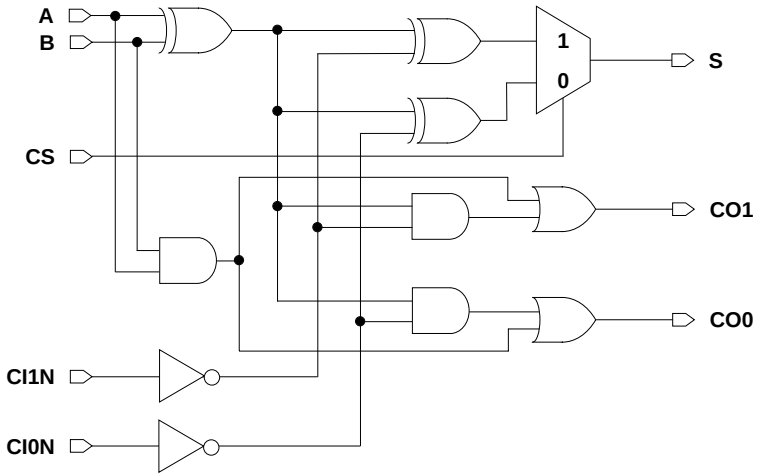
Drive Strength	Height (µm)	Width (µm)
AFCSHCINX2	5.04	33.00
AFCSHCINX4	5.04	38.28

Functions

A	B	CI0N	CI1N	CS	S	CO0	CO1
0	0	0	0	0	1	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0

A	B	CI0N	CI1N	CS	S	CO0	CO1
1	0	0	0	0	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	0	1	1
1	1	1	1	1	0	1	1

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
CS	0.0666	0.0666
A	0.3490	0.3860
B	0.3126	0.3444
CI0N	0.1311	0.1644
CI1N	0.1322	0.1636

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0056	0.0056
A	0.0075	0.0075
B	0.0170	0.0170
CI0N	0.0085	0.0146
CI1N	0.0085	0.0144

Delays at 25°C, 3.3V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
CS → S↑	0.147	0.148	2.265	2.261
CS → S↓	0.131	0.135	1.303	1.281
A → S↑	0.454	0.485	2.266	2.261
A → S↓	0.423	0.447	1.306	1.282
B → S↑	0.372	0.397	2.266	2.261
B → S↓	0.364	0.391	1.306	1.283
CI0N → S↑	0.284	0.291	2.266	2.261
CI0N → S↓	0.301	0.307	1.306	1.283
CI1N → S↑	0.255	0.251	2.266	2.261
CI1N → S↓	0.284	0.279	1.303	1.282
A → CO0↑	0.218	0.253	3.130	3.069
A → CO0↓	0.270	0.325	1.630	1.597
B → CO0↑	0.177	0.208	3.048	3.062
B → CO0↓	0.205	0.250	1.608	1.589
CI0N → CO0↑	0.090	0.069	3.159	1.590
CI0N → CO0↓	0.049	0.041	1.571	0.817
A → CO1↑	0.214	0.264	3.030	2.756
A → CO1↓	0.285	0.337	1.692	1.665
B → CO1↑	0.150	0.192	3.047	2.747
B → CO1↓	0.205	0.254	1.680	1.657
CI1N → CO1↑	0.086	0.065	3.092	1.543
CI1N → CO1↓	0.051	0.041	1.636	0.817

Cell Description

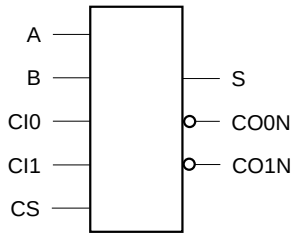
The AFCSHCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carry-outs (CO0N, CO1N) of two operands (A,B) with carry-ins (CI0, CI1). The three outputs (S, CO0N, CO1N) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus CI1) + \overline{CS} \bullet (A \oplus B \oplus CI0)$$

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol



Cell Size

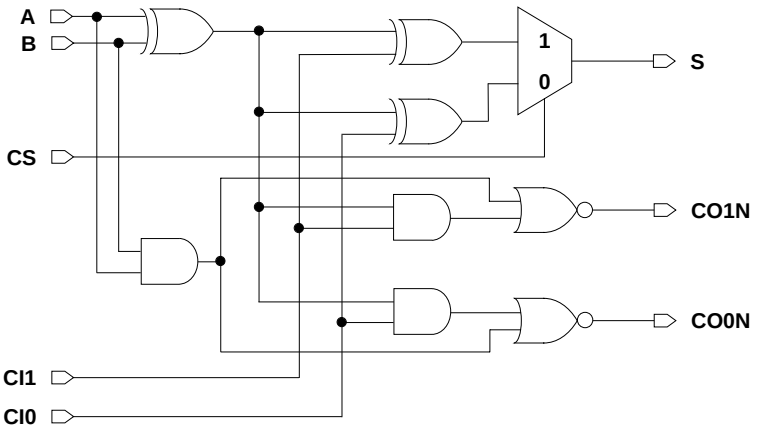
Drive Strength	Height (µm)	Width (µm)
AFCSHCONX2	5.04	33.66
AFCSHCONX4	5.04	38.94

Functions

A	B	CI0	CI1	CS	S	CO0N	CO1N
0	0	0	0	0	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	0	0	1	1
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0

A	B	CI0	CI1	CS	S	CO0N	CO1N
1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	1	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
CS	0.0663	0.0664
A	0.3524	0.3942
B	0.3292	0.3722
CI0	0.1636	0.2092
CI1	0.1379	0.1822

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0092	0.0092
A	0.0136	0.0137
B	0.0156	0.0156
CI0	0.0128	0.0255
CI1	0.0125	0.0253

Delays at 25°C, 3.3V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
CS → S↑	0.148	0.149	2.265	2.261
CS → S↓	0.131	0.135	1.303	1.281
A → S↑	0.481	0.526	2.266	2.262
A → S↓	0.431	0.471	1.307	1.284
B → S↑	0.430	0.472	2.266	2.261
B → S↓	0.396	0.421	1.306	1.284
CI0 → S↑	0.278	0.272	2.266	2.262
CI0 → S↓	0.278	0.264	1.305	1.283
CI1 → S↑	0.234	0.224	2.265	2.261
CI1 → S↓	0.247	0.233	1.304	1.282
A → CO0N↑	0.279	0.333	2.718	2.711
A → CO0N↓	0.276	0.338	1.702	1.667
B → CO0N↑	0.235	0.298	2.985	2.710
B → CO0N↓	0.222	0.281	1.701	1.667
CI0 → CO0N↑	0.078	0.066	3.068	1.636
CI0 → CO0N↓	0.053	0.043	1.771	0.915
A → CO1N↑	0.289	0.339	3.042	3.108
A → CO1N↓	0.271	0.338	1.658	1.635
B → CO1N↑	0.255	0.304	3.043	3.108
B → CO1N↓	0.219	0.281	1.649	1.635
CI1 → CO1N↑	0.072	0.058	3.062	1.556
CI1 → CO1N↓	0.049	0.037	1.772	0.829

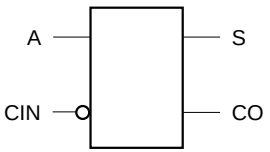
Cell Description

The AHHCIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN). The outputs (S, CO) are represented by the logic equations:

$$S = A \oplus \overline{CIN}$$

$$CO = A \bullet \overline{CIN}$$

Logic Symbol



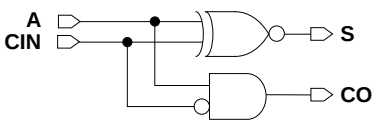
Functions

A	CIN	S	CO
0	0	1	0
0	1	0	0
1	0	0	1
1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AHHCINX2	5.04	7.92
AHHCINX4	5.04	9.24

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.0909	0.1114
CIN	0.0762	0.1024

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0081	0.0102
CIN	0.0157	0.0211

Delays at 25°C, 3.3V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.094	0.093	3.322	3.327
A → S↓	0.101	0.092	1.868	1.912
CIN → S↑	0.056	0.055	3.320	3.326
CIN → S↓	0.073	0.070	1.909	1.930
A → CO↑	0.080	0.073	4.917	2.458
A → CO↓	0.101	0.095	1.665	0.832
CIN → CO↑	0.054	0.051	4.915	2.458
CIN → CO↓	0.025	0.024	1.655	0.827

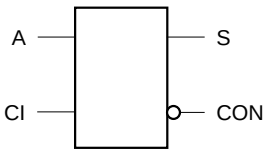
Cell Description

The AHHCON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI). The outputs (S, CON) are represented by the logic equations:

$$S = A \oplus CI$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol



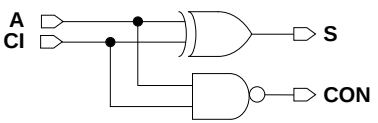
Functions

A	CI	S	CON
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
AHHCONX2	5.04	7.26
AHHCONX4	5.04	8.58

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.0995	0.1255
CI	0.0606	0.0786

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0119	0.0181
CI	0.0172	0.0231

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → S↑	0.103	0.104	3.240	3.235
A → S↓	0.111	0.110	1.858	1.854
CI → S↑	0.058	0.056	3.223	3.230
CI → S↓	0.074	0.069	1.814	1.835
A → CON↑	0.039	0.039	2.988	1.494
A → CON↓	0.026	0.024	2.002	0.924
CI → CON↑	0.032	0.030	2.990	1.495
CI → CON↓	0.023	0.020	2.002	0.924

Cell Description

The booth encoder block (BENC) cell performs a 2-bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (M0, M1, M2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction. The outputs (S, A, X2) are represented by the logic equations:

$$S = \overline{M2} \bullet (M1 + M0)$$

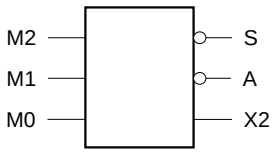
$$A = M2 \bullet (\overline{M1} + \overline{M0})$$

$$X2 = \overline{M1 \oplus M0}$$

Functions

M2	M1	M0	X2	A	S
0	0	0	x	1	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	x	1	1

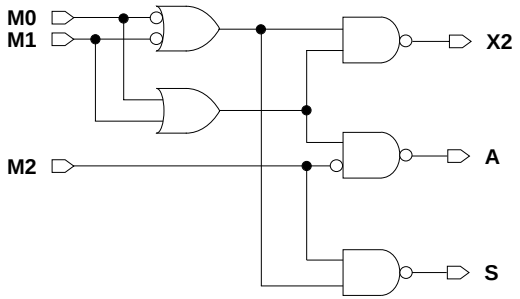
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
BENCX1	5.04	20.46
BENCX2	5.04	27.06
BENCX4	5.04	40.26

Functional Schematic



AC Power

Pin	Power (µW/MHz)		
	X1	X2	X4
M2	0.0793	0.1390	0.2528
M1	0.1639	0.2840	0.5764
M0	0.1885	0.3208	0.5996

Pin Capacitance

Pin	Capacitance (pF)		
	X1	X2	X4
M2	0.0079	0.0099	0.0160
M1	0.0104	0.0173	0.0302
M0	0.0095	0.0155	0.0245

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1	X2	X4	X1	X2	X4
M2 → A↑	0.228	0.229	0.214	1.117	0.562	0.281
M2 → A↓	0.208	0.215	0.221	0.664	0.326	0.163
M1 → A↑	0.254	0.233	0.206	1.116	0.562	0.281
M1 → A↓	0.179	0.169	0.183	0.665	0.327	0.163
M0 → A↑	0.245	0.220	0.192	1.116	0.562	0.281
M0 → A↓	0.172	0.159	0.170	0.665	0.327	0.163
M2 → S↑	0.177	0.176	0.168	1.174	0.562	0.279
M2 → S↓	0.138	0.128	0.137	0.656	0.325	0.156
M1 → S↑	0.312	0.277	0.254	1.174	0.562	0.279
M1 → S↓	0.305	0.269	0.280	0.657	0.326	0.157
M0 → S↑	0.285	0.245	0.234	1.174	0.562	0.279
M0 → S↓	0.247	0.236	0.236	0.657	0.326	0.156
M1 → X2↑	0.211	0.180	0.186	1.104	0.552	0.253
M1 → X2↓	0.259	0.228	0.216	0.709	0.455	0.174
M0 → X2↑	0.266	0.216	0.225	1.104	0.551	0.253
M0 → X2↓	0.276	0.258	0.253	0.710	0.455	0.174

Cell Description

The BMX cell performs the shifting and 2's complement inversion of the multiplicand bits (M1 and M0) based on the recode control signals (X2, A, and S) from the BENC cell. The partial product output (PP) is represented by the logic equation:

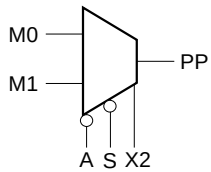
$$PP = X2 \bullet ((M0 \bullet \overline{A}) + (\overline{M0} \bullet \overline{S})) + \overline{X2} \bullet ((M1 \bullet \overline{A}) + (\overline{M1} \bullet \overline{S}))$$

Functions[1]

X2	A	S	M0	M1	PP
0	0	0	x	x	x
0	0	1	x	0	0
0	0	1	x	1	1
0	1	0	x	0	1
0	1	0	x	1	0
0	1	1	x	x	0
1	0	0	x	x	x
1	0	1	0	x	0
1	0	1	1	x	1
1	1	0	0	x	1
1	1	0	1	x	0
1	1	1	x	x	0

[1] Shaded areas represent illegal conditions.

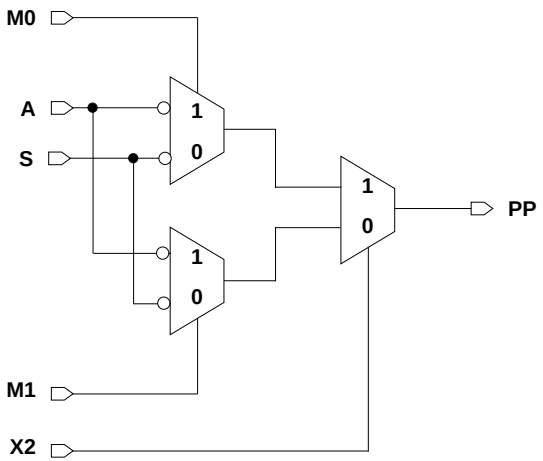
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
BMXX1	5.04	12.54

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
X2	0.0404
M0	0.0596
A	0.0623
S	0.0816
M1	0.0517

Pin Capacitance

Pin	Capacitance (pF)
	X1
X2	0.0034
M0	0.0057
A	0.0046
S	0.0044
M1	0.0053

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
X2 → PP↑	0.146	4.516
X2 → PP↓	0.130	2.495
M0 → PP↑	0.210	4.521
M0 → PP↓	0.257	2.500
A → PP↑	0.232	4.520
A → PP↓	0.226	2.499
S → PP↑	0.253	4.521
S → PP↓	0.241	2.499
M1 → PP↑	0.193	4.521
M1 → PP↓	0.231	2.489

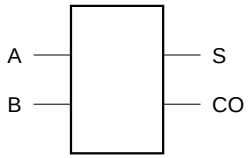
Cell Description

The CMPR22 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$S = (\bar{A} \bullet B) + (A \bullet \bar{B})$

$CO = A \bullet B$

Logic Symbol



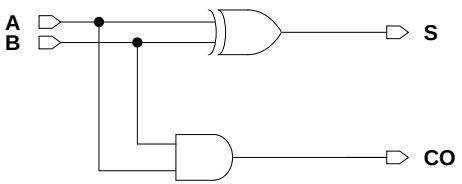
Functions

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
CMPR22X1	5.04	7.92

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
A	0.1120
B	0.0621

Pin Capacitance

Pin	Capacitance (pF)
	X1
A	0.0108
B	0.0089

Delays (25°C, 1.8V, Typical Process)

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → S↑	0.090	2.756
A → S↓	0.095	1.627
B → S↑	0.060	2.735
B → S↓	0.080	1.551
A → CO↑	0.089	4.522
A → CO↓	0.127	2.620
B → CO↑	0.089	4.520
B → CO↓	0.122	2.617

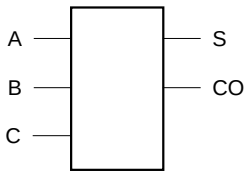
Cell Description

The CMPR32 cell takes in 3 bits of the partial product (A, B, C) and compresses them into 2-bits of partial product (S, CO). The two outputs (S, CO) are represented by the logic equations:

$$S = A \oplus B \oplus C$$

$$CO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

Logic Symbol



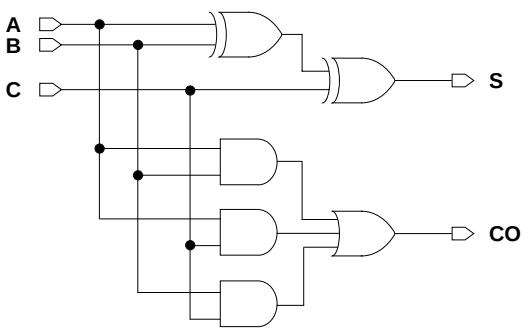
Functions

A	B	C	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
CMPR32X1	5.04	13.86

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X1
A	0.1196
B	0.1533
C	0.0630

Pin Capacitance

Pin	Capacitance (pF)
	X1X2
A	0.0072
B	0.0070
C	0.0066

Delays at 25°C, 1.8V, Typical Process

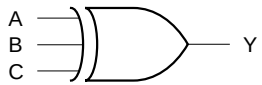
Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X1	X1
A → S↑	0.231	4.532
A → S↓	0.311	2.614
B → S↑	0.271	4.538
B → S↓	0.354	2.613
C → S↑	0.182	4.533
C → S↓	0.158	2.614
A → CO↑	0.285	4.512
A → CO↓	0.279	2.514
B → CO↑	0.327	4.512
B → CO↓	0.302	2.465
C → CO↑	0.143	4.527
C → CO↓	0.190	2.537

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A,B,C). The output (Y) is represented by the following equation:

$$Y = A \oplus B \oplus C$$

Logic Symbol



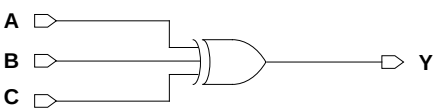
Functions

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

Drive Strength	Height (µm)	Width (µm)
XOR3X2	5.04	11.88
XOR3X4	5.04	19.80

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1477	0.2802
B	0.1283	0.2402
C	0.0601	0.1099

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0069	0.0137
B	0.0151	0.0285
C	0.0088	0.0163

Delays at 25°C, 1.8V, Typical Process

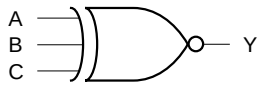
Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X2	X4	X2	X4
A → Y↑	0.276	0.260	2.226	1.113
A → Y↓	0.301	0.280	1.319	0.655
B → Y↑	0.180	0.168	2.225	1.113
B → Y↓	0.221	0.210	1.308	0.653
C → Y↑	0.147	0.139	2.224	1.113
C → Y↓	0.144	0.139	1.301	0.650

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE NOR of three inputs (A,B,C). The output (Y) is represented by the following equation:

$$Y = \overline{A \oplus B \oplus C}$$

Logic Symbol



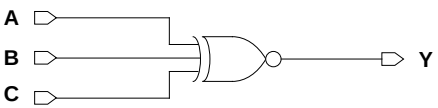
Functions

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

Drive Strength	Height (µm)	Width (µm)
XNOR3X2	5.04	11.88
XNOR3X4	5.04	19.80

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X2	X4
A	0.1475	0.2786
B	0.1252	0.2308
C	0.0606	0.1100

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0069	0.0137
B	0.0151	0.0284
C	0.0052	0.0093

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF	
	X2	X4	X2	X4
A → Y↑	0.275	0.260	2.225	1.113
A → Y↓	0.303	0.283	1.318	0.655
B → Y↑	0.181	0.169	2.225	1.113
B → Y↓	0.219	0.207	1.309	0.653
C → Y↑	0.148	0.139	2.224	1.113
C → Y↓	0.143	0.139	1.303	0.650

Cell Description

The CMPR42 cell takes in 4 bits of the partial product (A, B, C, D) and compresses them into 2-bits of partial product (S, CO). The cell requires an intermediate carry-in input (ICI) from the n-1 compressor and an intermediate carry-out output (CO) to the n+1 compressor. The CMPR42 cell also contains an internal sum (IS). The internal sum (IS), carry-in output (ICO), and the two outputs (S, CO) are represented by the logic equations:

$$IS = A \oplus B \oplus C$$

$$ICO = (A \bullet B) + (A \bullet C) + (B \bullet C)$$

$$S = IS \oplus D \oplus ICI$$

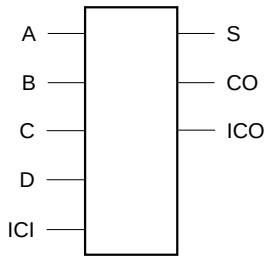
$$CO = (IS \bullet D) + (IS \bullet ICI) + (D \bullet ICI)$$

Functions

A	B	C	IS	ICO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IS	D	ICI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

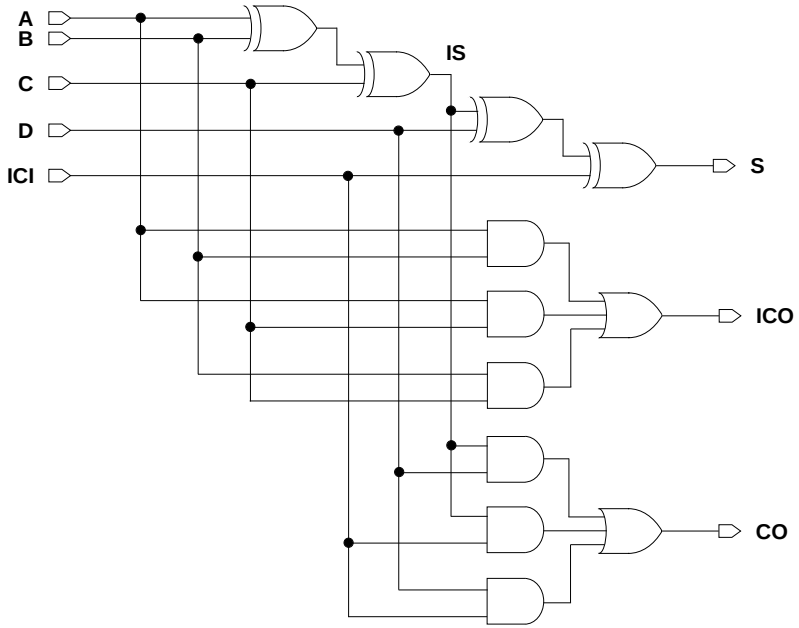
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
CMPR42X1	5.04	22.44
CMPR42X2	5.04	26.40

Functional Schematic



AC Power

Pin	Power (µW/MHz)	
	X1	X2
A	0.1702	0.2942
B	0.1642	0.2798
C	0.1542	0.2668
D	0.1267	0.2124
ICI	0.0677	0.1189

Pin Capacitance

Pin	Capacitance (pF)	
	X1	X2
A	0.0086	0.0162
B	0.0086	0.0164
C	0.0082	0.0136
D	0.0047	0.0095
ICI	0.0029	0.0061

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	X2	X1	X2
A → S↑	0.549	0.542	4.532	2.238
A → S↓	0.647	0.648	2.493	1.291
B → S↑	0.479	0.445	4.528	2.238
B → S↓	0.569	0.551	2.493	1.291
C → S↑	0.425	0.402	4.530	2.238
C → S↓	0.523	0.512	2.493	1.291
D → S↑	0.438	0.339	4.525	2.235
D → S↓	0.452	0.410	2.491	1.291
ICI → S↑	0.251	0.191	4.528	2.237
ICI → S↓	0.270	0.210	2.495	1.291
A → ICO↑	0.123	0.091	4.531	2.238
A → ICO↓	0.197	0.166	2.496	1.230
B → ICO↑	0.123	0.092	4.530	2.239
B → ICO↓	0.185	0.159	2.514	1.234
C → ICO↑	0.107	0.082	4.526	2.236
C → ICO↓	0.160	0.139	2.520	1.236
A → CO↑	0.533	0.526	4.532	2.237
A → CO↓	0.614	0.618	2.511	1.230
B → CO↑	0.473	0.462	4.522	2.238
B → CO↓	0.544	0.554	2.510	1.229
C → CO↑	0.420	0.389	4.531	2.237
C → CO↓	0.456	0.432	2.511	1.230
D → CO↑	0.387	0.315	4.525	2.235
D → CO↓	0.401	0.321	2.508	1.223
ICI → CO↑	0.154	0.101	4.534	2.238
ICI → CO↓	0.198	0.158	2.556	1.246

Cell Description

The RF1R1W register file cell is an active-high D-type transparent latch with an active-high tri-state output. The output (RB) is inverted.

Functions for Write Operations

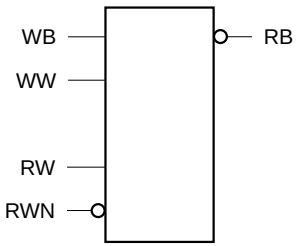
WW	WB	Q[n+1]
0	0	0
0	1	Q[n]
0	0	Q[n]
0	1	Q[n]
1	0	0
1	1	1
1	0	Q[n]
1	1	1

Functions for Read Operations[1]

RW	RWN	Q	RB
0	0	0	1
0	0	1	Hi-Z
0	1	0	Hi-Z
0	1	1	Hi-Z
1	0	0	1
1	0	1	0
1	1	0	Hi-Z
1	1	1	0

[1] Shaded areas represent operations that are legal only during RW/RWN transitions.

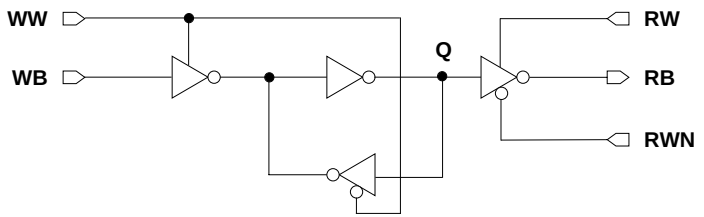
Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
RF1R1WX2	5.04	6.60

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X2
WW	0.0375
WB	0.0379
RW	0.0119
RB	0.0226

Pin Capacitance

Pin	Capacitance (pF)
	X2
WW	0.0054
WB	0.0023
RW	0.0030
RWN	0.0020
RB	0.0091

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	X2
WW → RB↑	0.291	4.358
WW → RB↓	0.175	1.810
WB → RB↑	0.273	4.358
WB → RB↓	0.190	1.810
RW → RB↑	0.033	4.354
RW → RB↓	0.014	1.804

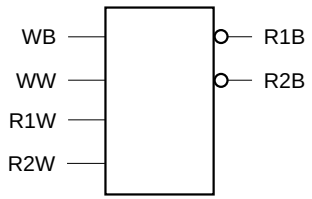
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)
		X2
WW	minpwh	0.18
WB	setup↑ → WW	0.10
	setup↓ → WW	0.15
	hold↑ → WW	-0.09
	hold↓ → WW	-0.14

Cell Description

The RF2R1W register file cell is an active-high D-type transparent latch with two independently controlled, active-high tri-state outputs. The cell has two read ports and one write port. The outputs (R1B, R2B) are inverted.

Logic Symbol



Functions for Write Operations

WW	WB	Q[n+1]
0	0	Q[n]
0	1	Q[n]
1	0	0
1	1	1

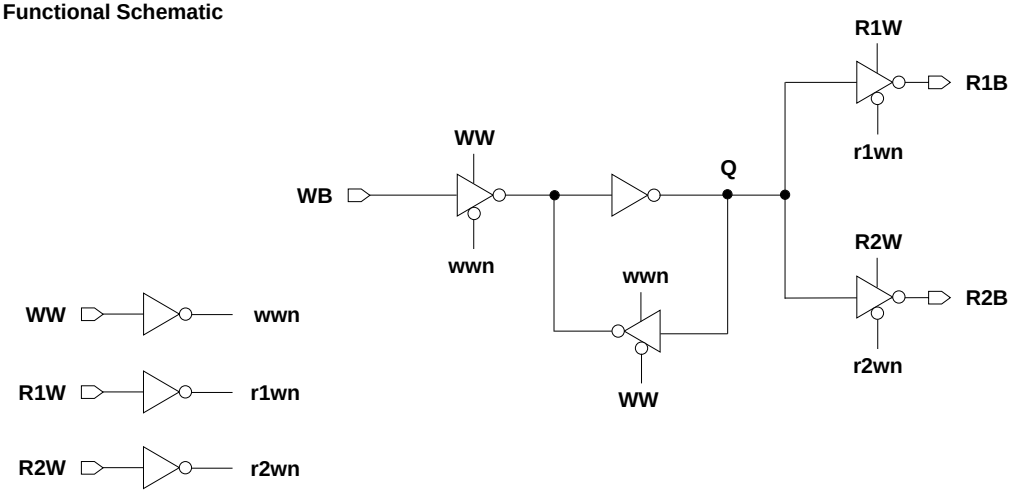
Cell Size

Drive Strength	Height (µm)	Width (µm)
RF2R1WX2	5.04	10.56

Functions for Read Operations

R1W/ R2W	Q	R1B/ R2B
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0

Functional Schematic



AC Power

Pin	Power (µW/MHz)
	X2
WB	0.0519
WW	0.0141
R1W	0.0131
R2W	0.0129
R1B	0.0973

Pin Capacitance

Pin	Capacitance (pF)
	X2
WB	0.0024
WW	0.0045
R1W	0.0034
R2W	0.0045
R1B	0.0051
R2B	0.0050

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	X2
WB → R1B↑	0.313	4.359
WB → R1B↓	0.228	1.818
WW → R1B↑	0.328	4.360
WW → R1B↓	0.214	1.818
R1W → R1B↑	0.071	4.354
R1W → R1B↓	0.016	1.803
WB → R2B↑	0.312	4.360
WB → R2B↓	0.228	1.818
WW → R2B↑	0.327	4.359
WW → R2B↓	0.214	1.817
R2W → R2B↑	0.070	4.354
R2W → R2B↓	0.016	1.803

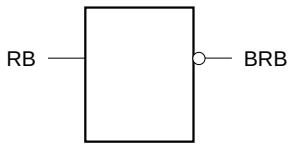
Timing Constraints at 25°C, 1.8V, Typical Process

Pin	Requirement	Interval (ns)
		X2
WB	setup↑ → WW	0.12
	setup↓ → WW	0.17
	hold↑ → WW	-0.10
	hold↓ → WW	-0.15
WW	minpwh	0.18

Cell Description

The RFRD output buffer has a “keeper” function that holds the input and output ports at the present level when the input (RB) is in a state of high-impedance.

Logic Symbol



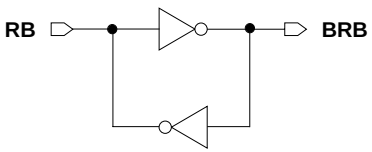
Functions

RB	BRB
0	1
1	0
Hi-Z	Keep

Cell Size

Drive Strength	Height (µm)	Width (µm)
RFRDX1	5.04	3.30
RFRDX2	5.04	3.30
RFRDX4	5.04	3.96

Functional Schematic



AC Power

Pin	Power (µW/MHz)		
	X1	X2	X4
RB	0.0303	0.0385	0.0555

Pin Capacitance

Pin	Capacitance (pF)		
	X1	X2	X4
RB	0.0251	0.0260	0.0329

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1	X2	X4	X1	X2	X4
RB → BRB↑	0.051	0.035	0.026	4.519	2.234	1.117
RB → BRB↓	0.031	0.021	0.015	2.401	1.194	0.597