Power Dissipation

There are 3 main source of power dissipation in CMOS logic:

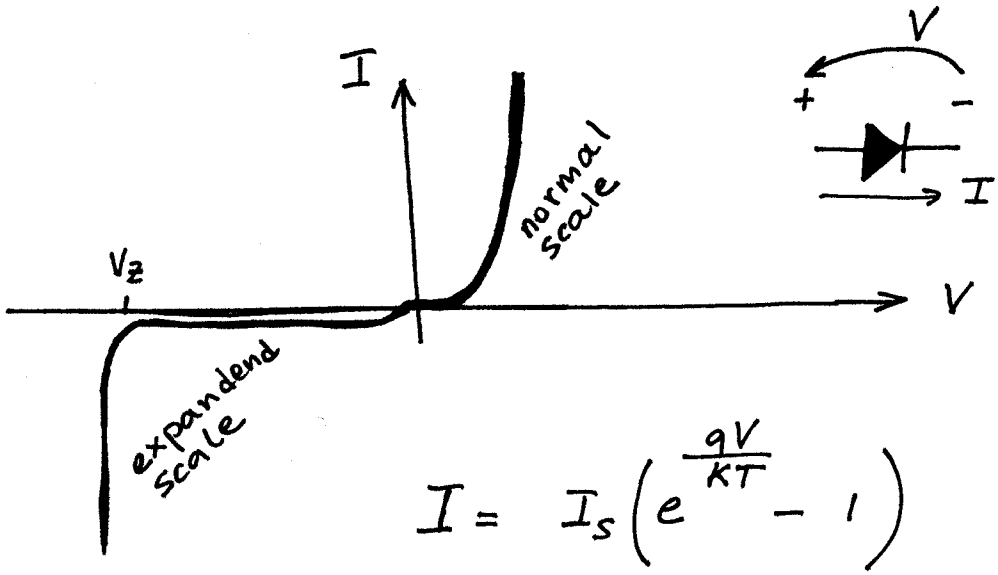
1. static power dissipation due mainly to leakage current
2. dynamic power dissipation due to the charging and discharging of the load capacitance.
3. dynamic power dissipation due to the transient current during switching time (when both nMOS and pMOS are conducting)

1. Static power dissipation

A cmos transistor is never completely OFF.

"The source and drain (diffusion regions) of every transistor, as well as the junction between the wells and substrate form parasitic diodes". [Textbook]

Transistor leakage current is due to the fact that a reversed diode conduct a very small leakage current.



PN junction

$$I = I_S\left(e^{\frac{qV}{KT}} - 1\right)$$

where

q = electron charge $= 1.602 \times 10^{-19}$ C

k = Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K

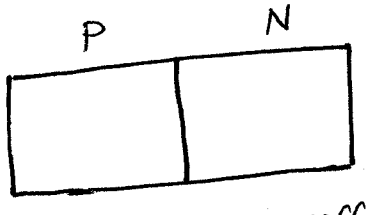
T = temperature

V = voltage applied to the diode

I_S = reverse saturation current (e.g. order $10^{-14} \div 10^{-15}$ A)

$$I_S = q \cdot AREA \cdot \left(\frac{D_p P_n}{L_p} + \frac{D_n n_p}{L_n}\right)$$

(n_p: electron density in region P)



D_p = hole diffusion constant

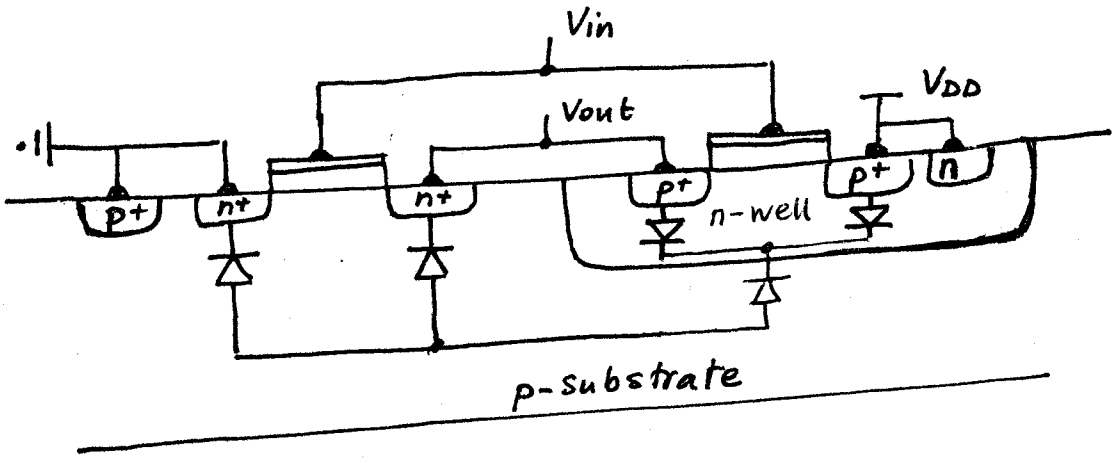
D_n = electron diffusion constant

τ_n = electron minority carrier lifetime

τ_p = hole minority carrier lifetime

$L_n = \sqrt{\tau_n D_n}$ ← electron diffusion length

$L_p = \sqrt{\tau_p D_p}$ ← hole diffusion length



The picture shows the parasitic diodes in a CMOS inverter

$$P_{static} = \sum_{1}^{n/2} \text{leakage current} \times V_{DD}$$

where n is the number of transistors
(In practice we assume that only half of the transistors are off at any time)

Example

* $I_{leakage} \approx 560 \times 10^{-15}$ A (per transistor)
We assume that the leakages for the n-diffusion/p-substrate and p-diffusion/n-well are the same and we neglect the effect of the n-well/p-substrate leakage (we have the effect of the n-well/p-substrate diode only when the nMOS is OFF, so in average we can reasonably neglect it)

* power supply 3.3 V

* ASIC size 100 000 transistor

$$P_{static} = 10^5 \cdot \frac{1}{2} \cdot 560 \cdot 10^{-15} \cdot 3.3 \simeq 1.85 \times 10^{-12} \text{ W}$$

As you can see the static power dissipation is really small, so it is usually neglected.

The total leakage current measured when the power supply is applied, but there is no signal activity (each input is set to a steady value and kept at this value) can be used as a quick method to test if the ASIC is "broken".

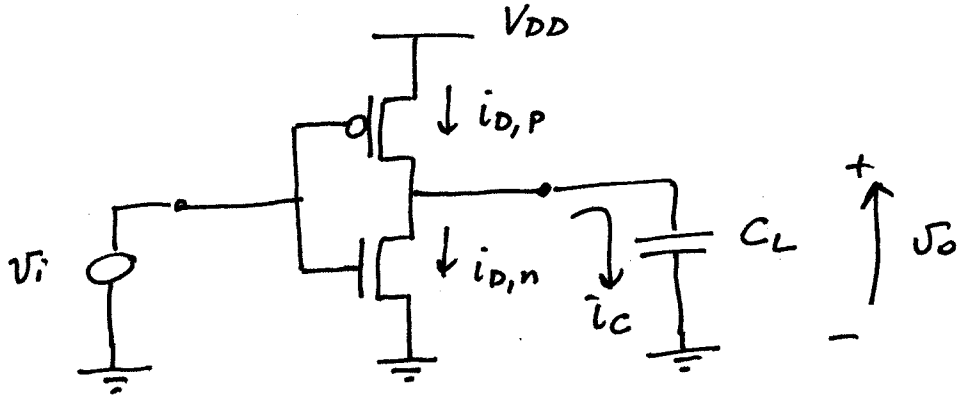
The leakage current measured under this conditions (I_{DDQ} = quiescent leakage current) is expected to be very small.

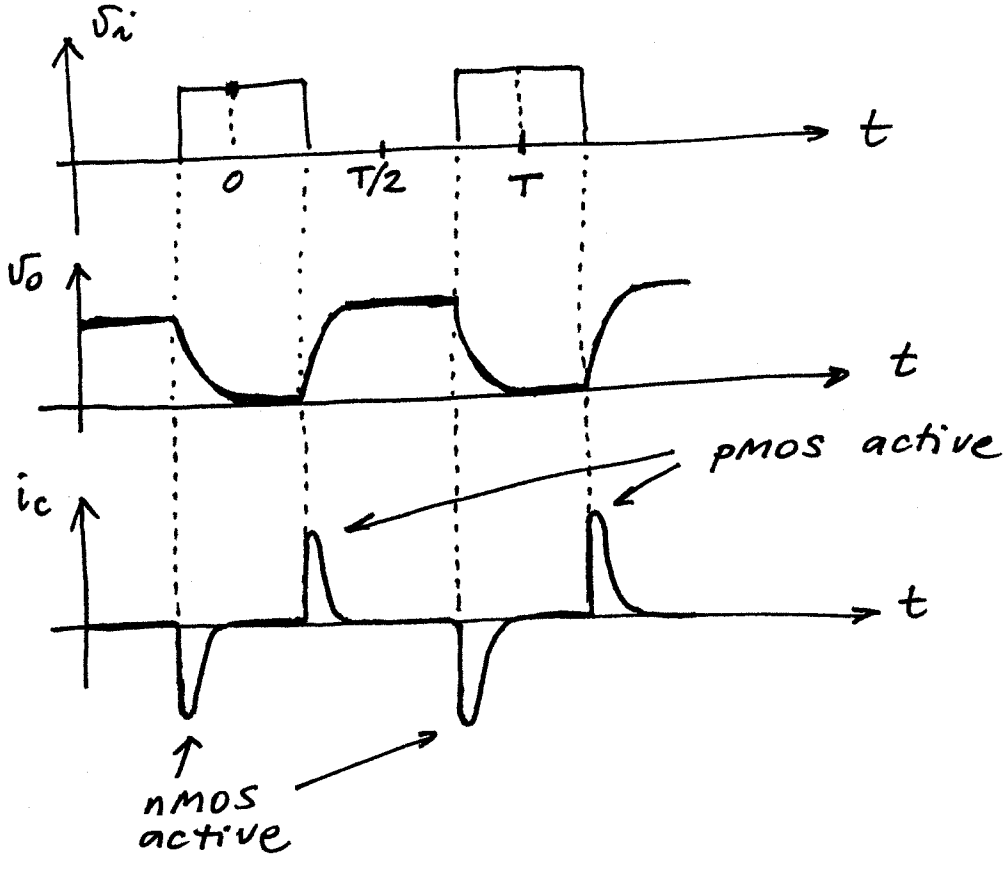
All the parts with an I_{DDQ} bigger than a certain threshold are discarded.

2. Dynamic Power dissipation - switching current

This is the biggest contribute to the power dissipation, so often in practice is used to estimate the total power dissipation.

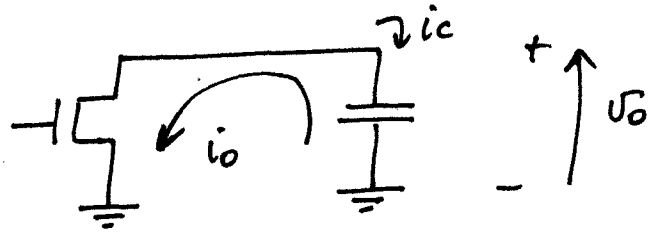
It's due to the charging and discharging of the load capacitance.





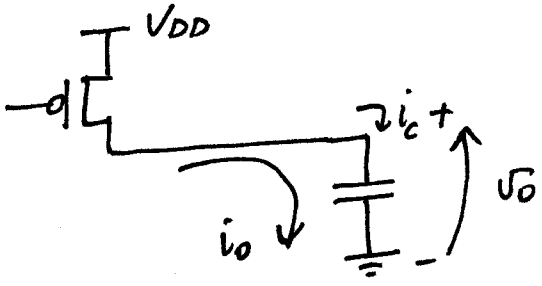
$$P_d = \text{average power} = \frac{1}{T}\int_0^T v_o(t)\cdot i_o(t)\,dt$$

nMOS active



at the beginning the capacitance is charged

pMOS active



at the beginning the capacitance is uncharged

pMOS active $\rightarrow$ $\displaystyle\int_0^{T/2} v_o(t)\cdot i_o(t)\,dt = P_{d_{PMOS}}$

nMOS active $\rightarrow$ $\displaystyle\int_{T/2}^{T} v_o(t)\cdot i_o(t)\,dt = P_{d_{NMOS}}$

$$i_o = |i_c|$$

$$i_o = i_{D,p} \quad \text{or} \quad i_{D,n}$$

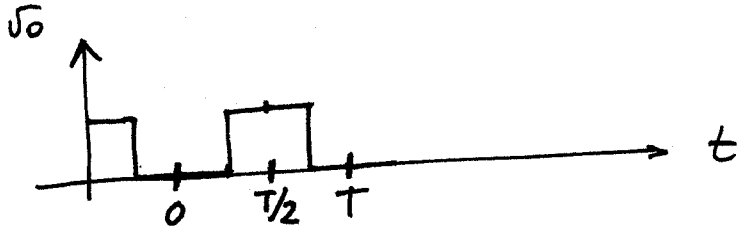
pMOS active

$$\int_0^{T/2} v_o(t)\, i_o(t)\, dt = \int_0^{T/2} v_o(t) \cdot i_c(t)\, dt =$$

$$= \int_0^{T/2} v_o(t) \cdot C_L \frac{dv_c}{dt} dt = C_L \int_0^{T/2} v_o \frac{dv_o}{dt} dt$$

$$= C_L \int_{v_o(0)}^{v_o(T/2)} v_o\, dv_o = C_L \left[\frac{v_o^2}{2} \right]_{v_o(0)}^{v_o(T/2)} =$$

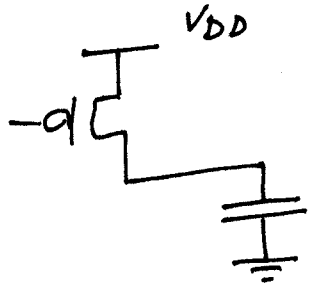
$$= C_L \left[\frac{V_{DD}^2}{2} - 0 \right] = C_L \cdot \frac{V_{DD}^2}{2}$$



$v_o(0) = 0$

$v_o(T/2) = V_{DD}$

$v_o(T) = 0$



C_L is initially uncharged

nMOS active

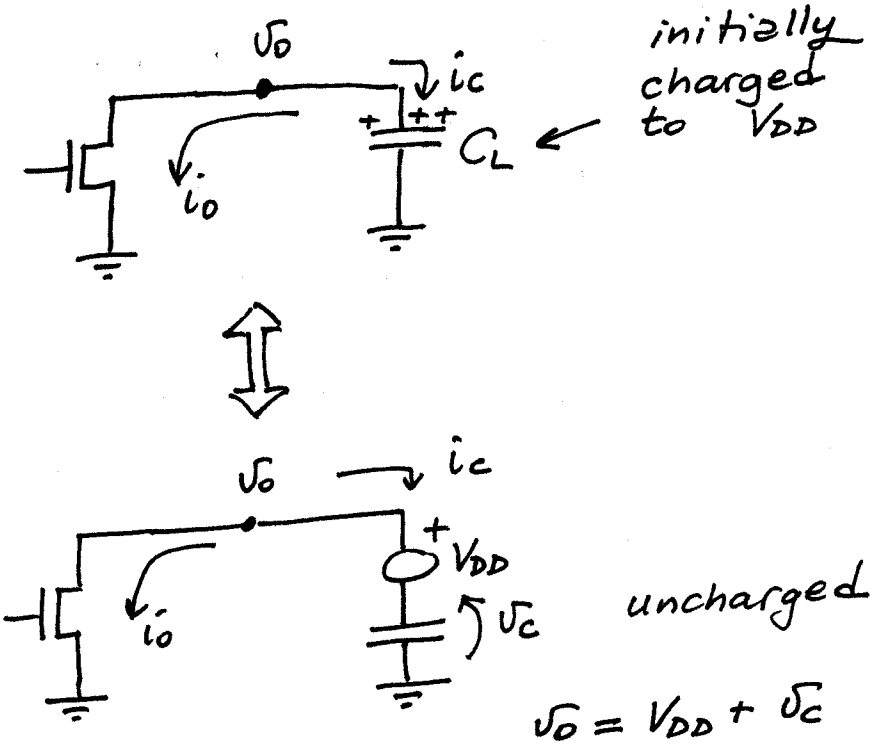
$$\int_{T/2}^{T} v_o(t)\, i_o(t)\, dt = \int_{T/2}^{T} v_o(t)\cdot\left(-i_c(t)\right) dt =$$

$$= -\int_{T/2}^{T} v_o(t)\cdot i_c(t)\, dt = -\int_{T/2}^{T} v_o(t)\cdot C_L \frac{dv_c(t)}{dt} dt =$$

$$= -C_L \int_{T/2}^{T} v_o(t)\cdot \frac{dv_c(t)}{dt}\, dt =$$

$$= -C_L \int_{T/2}^{T} v_o(t)\cdot \frac{d(v_o - V_{DD})}{dt}\, dt =$$

$v_c = v_o - V_{DD}$



$v_o = V_{DD} + v_c$

$$= -C_L \int_{v_o(T/2)-V_{DD}}^{v_o(T)-V_{DD}} v_o\, d(v_o - V_{DD}) =$$

$$= - C_L \int_{u(T/2)}^{u(T)} (u + V_{DD})\, du =$$

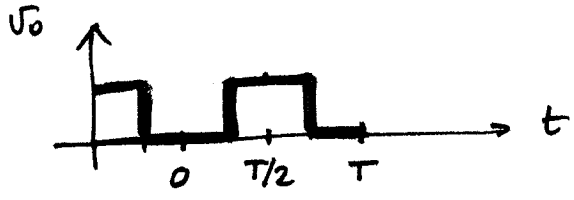
$\uparrow$ $u = v_o - V_{DD}$

$$= -\left(C_L \int_{u(T/2)}^{u(T)} u\, du + C_L \int_{u(T/2)}^{u(T)} V_{DD}\, du \right) =$$

$$= - C_L \left\{ \left[\frac{u^2}{2} \right]_{u(T/2)}^{u(T)} + V_{DD} \cdot \left[u \right]_{u(T/2)}^{u(T)} \right\} =$$

$$= - C_L \cdot \left[\frac{(v_o(T) - V_{DD})^2}{2} - \frac{(v_o(T/2) - V_{DD})^2}{2} \right]$$

$$- C_L \cdot V_{DD} \left[(v_o(T) - V_{DD}) - (v_o(T/2) - V_{DD}) \right] =$$



$$= - C_L \left[\frac{(-V_{DD})^2}{2} - 0 \right] - C_L V_{DD} \left[-V_{DD} - 0 \right] =$$

$$= C_L \frac{V_{DD}^2}{2}$$

So globally

$$P_d = P_{average} = \frac{1}{T}\left[\underbrace{\int_0^{T/2} v_o(t)\cdot i_o(t)\,dt}_{P_{d_{PMOS}}} + \underbrace{\int_{T/2}^{T} v_o(t)\cdot i_o(t)\,dt}_{P_{d_{NMOS}}} \right] =$$

$$= \frac{1}{T} C_L \cdot V_{DD}^2$$

The interesting thing to notice is that the power is proportional to the switching frequency and the load but does not depend at all on the transistor parameters

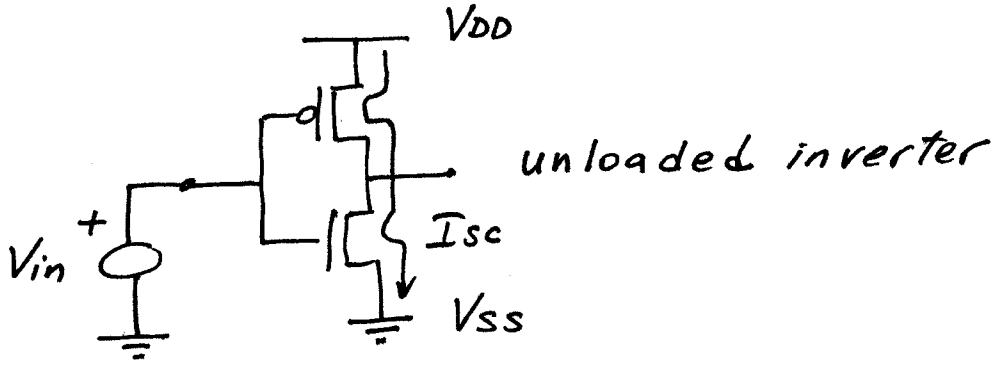
Since V_{DD} appears squared in the power dissipation equation, the best way to reduce power is to reduce V_{DD} ($5V \rightarrow 3.3V \rightarrow \ldots$)

f = switching frequency = $\frac{1}{T}$

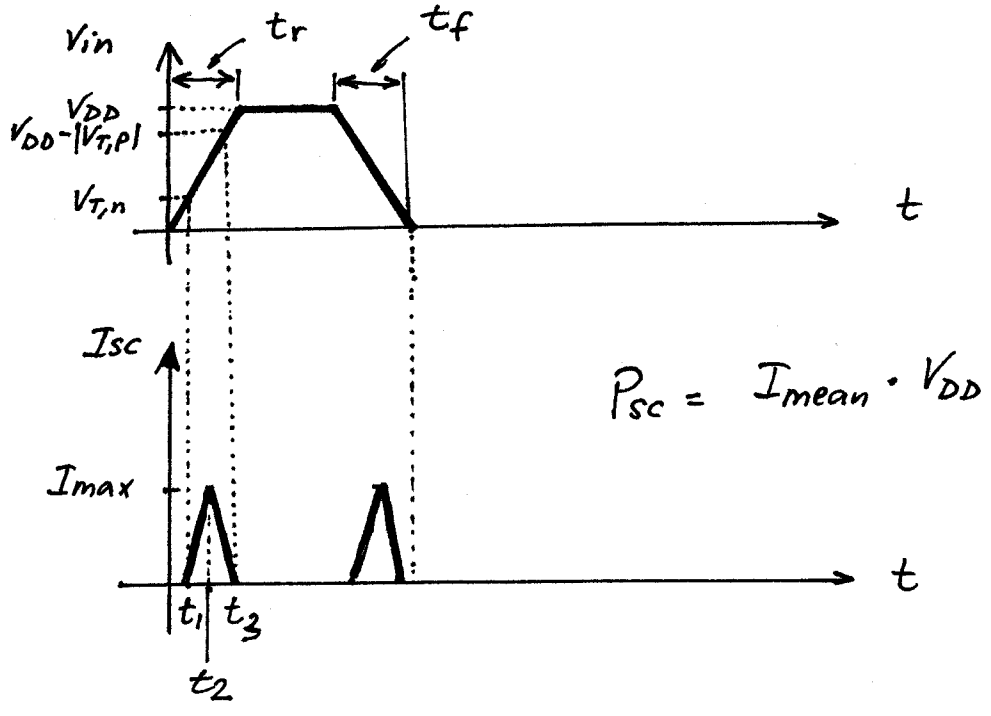
↙ also called toggle frequency

3. Dynamic power dissipation – Short circuit current

When both nMOS and pMOS are "on" there is a current path between V_{DD} and V_{SS} (short circuit current). This results in dissipation



The amount of time that both transistors remain active depends on the way we have designed the inverter (β_n, β_p), how often the input signal toggle and the slope of the input waveform



$$P_{sc} = I_{mean} \cdot V_{DD}$$

In order To make things a little bit easier we can assume that the inverter is symmetrical: $\beta_n = \beta_p \triangleq \beta$, $V_{T,n} = -V_{T,p} \triangleq V_T$ and that the input waveform has the same rise and fall time $t_r = t_f \triangleq t_{r,f}$

$$I_{mean} = \frac{4}{T} \int_{t_1}^{t_2} I(t)\,dt$$

Since for $V_{T,n} \le V_{in} \le V_{DD} - |V_{T,p}|$ at least one of the two transistor is in saturation we know that:

$$I(t) = \frac{\beta}{2} \left(V_{in}(t) - V_T \right)^2$$

Recalling some geometry we can write that:

$$V_{in}(t) = \frac{V_{DD}}{t_{r,f}} \cdot t \qquad \text{for} \quad t_1 \le t \le t_2$$

$$t_1 = V_T \cdot \frac{t_{r,f}}{V_{DD}}$$

$$V_{in}(t_1) = V_T$$

$$t_2 = \frac{t_{r,f}}{2}$$

$$I_{mean} = \frac{4}{T} \int_{\frac{t_{r,f}}{2}}^{\frac{V_T}{V_{DD}} t_{r,f}} \frac{\beta}{2} \left(\frac{V_{DD}}{t_{r,f}} t - V_T \right)^2 dt =$$

$$= \frac{2\beta}{T} \int_{\frac{t_{r,f}}{2}}^{\frac{V_T}{V_{DD}} \cdot t_{r,f}} \left(\frac{V_{DD}}{t_{r,f}} t - V_T \right)^2 dt =$$

.... and so on

It is possible to find out that the power dissipated because of the short-circuit current is:

$$P_{SC} = I_{mean} \cdot V_{DD} = \frac{\beta}{12} (V_{DD} - 2V_T)^3 \cdot \frac{t_{r,f}}{T}$$

Usually the P_{sc} is negligible, however if β is particularly big (high drive strength output buffer or large clock buffers) it can play a non negligible role.

$$P_{total} = P_{static} + \underbrace{P_d + P_{sc}}_{P_{dynamic}} \approx P_d$$

P_{total}: total power dissipation

$\approx$: often