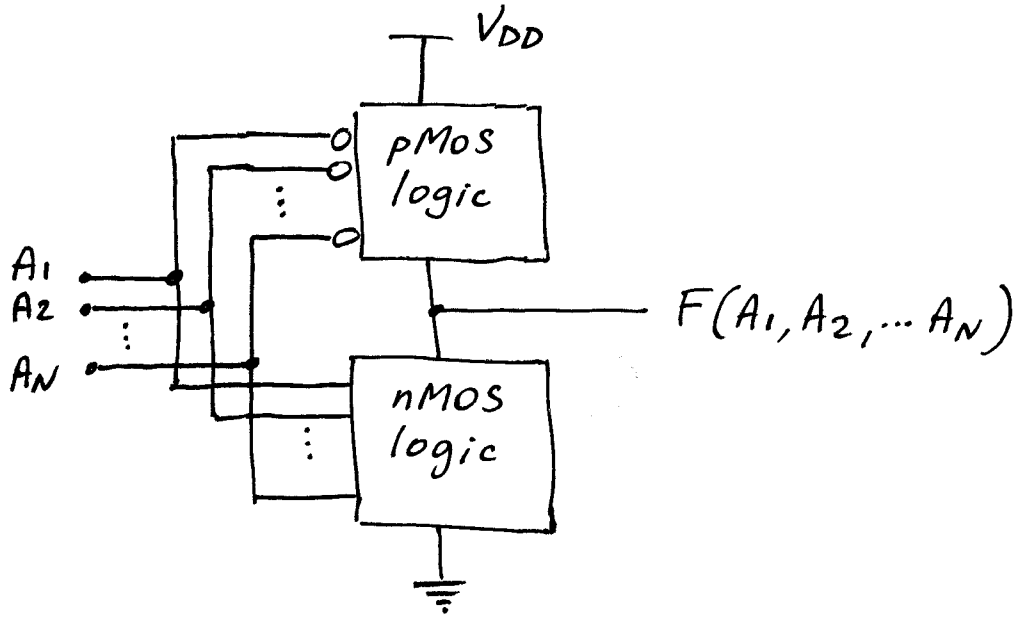
CMOS combinational logic

CMOS logic gates are built from symmetric ("complementary") nMOS and pMOS transistors structures



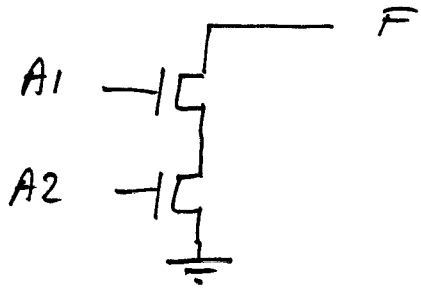
Generic CMOS gate

Example : 2 inputs NAND gate

A1	A2	F
0	0	1
0	1	1
1	0	1
1	1	0

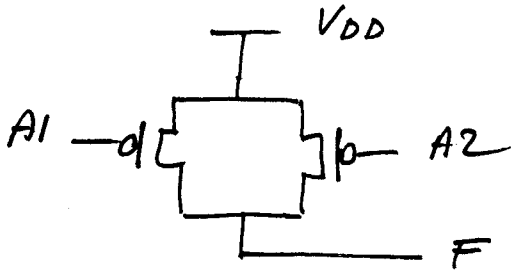
For F=0 I need to create a path between F and ground (this is done through the nMOS transistors)

In order to put F=1 I need to create a path between F and VDD (this is done through the pMOS transistors)



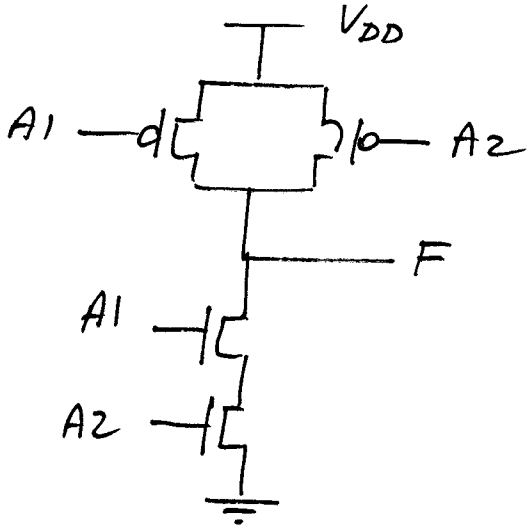
nMOS logic section

Once one of the 2 sections is built we can infer the other by symmetry (no need of too much thinking)



pMOS logic section

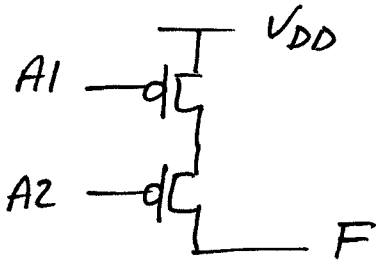
The "complementary" logic is built simply putting together the pMOS and nMOS sections.



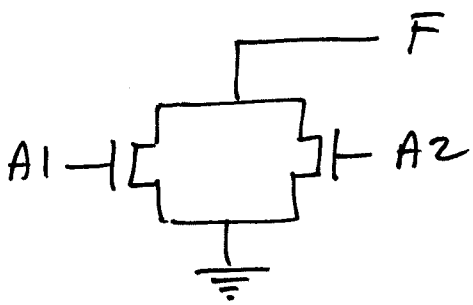
Example : 2 inputs NOR gate

A_1	A_2	F
0	0	1
0	1	0
1	0	0
1	1	0

This time I start building the pMOS logic (I have less ones than zeros on the F column) and later I build the nMOS logic by symmetry



The switches connected serially on one section become connected in parallel in the other section, and viceversa.



Example

$$F = \overline{ABC + AD}$$

A	B	C	D	F
1	1	1	–	0
1	–	–	1	0
0	–	–	–	1
–	0	–	0	1
–	–	0	0	1