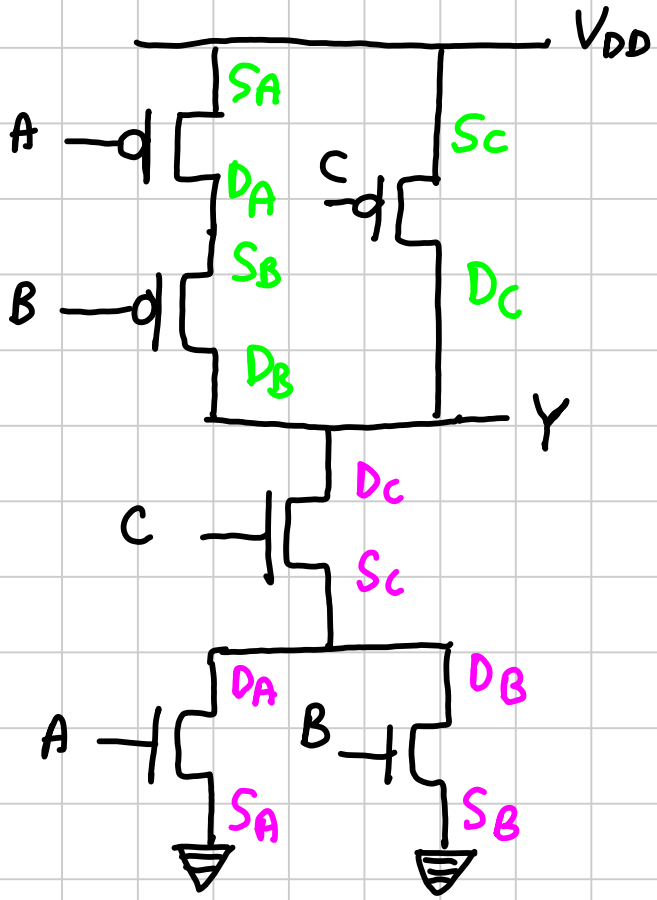
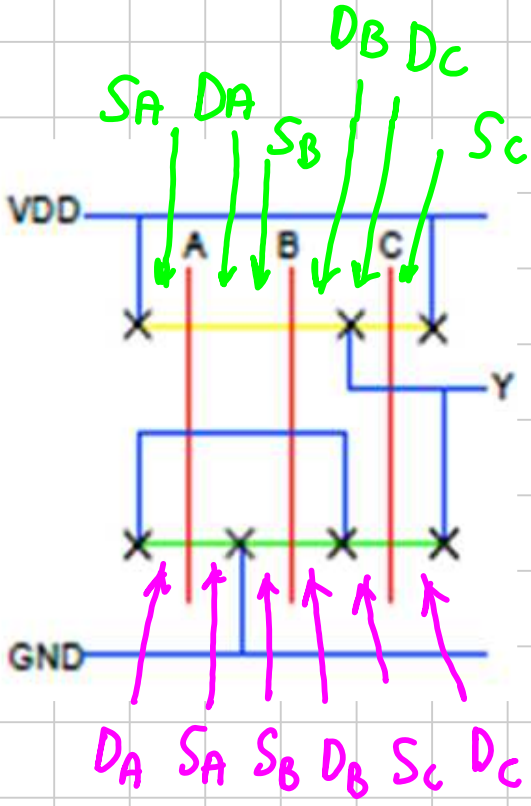
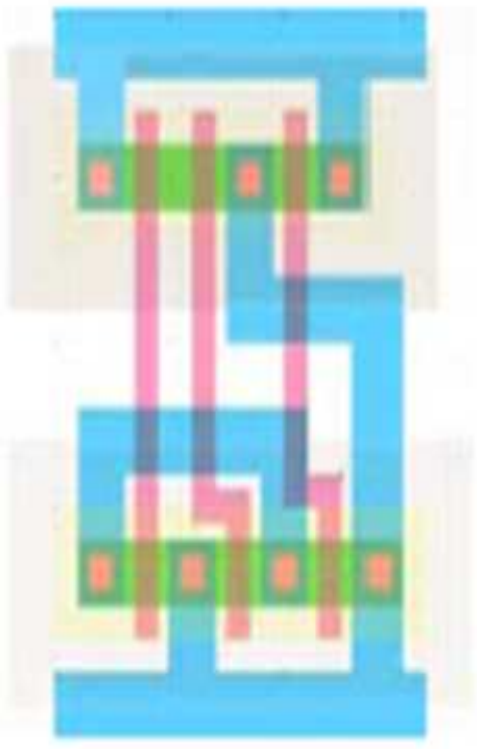
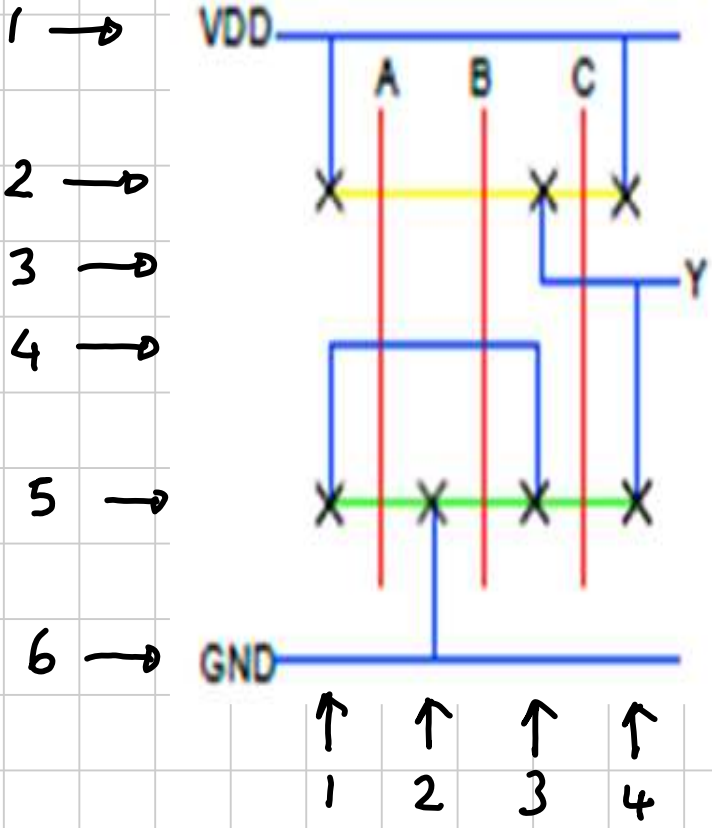
Problem #1

$$Y = \overline{(A+B)\cdot C}$$



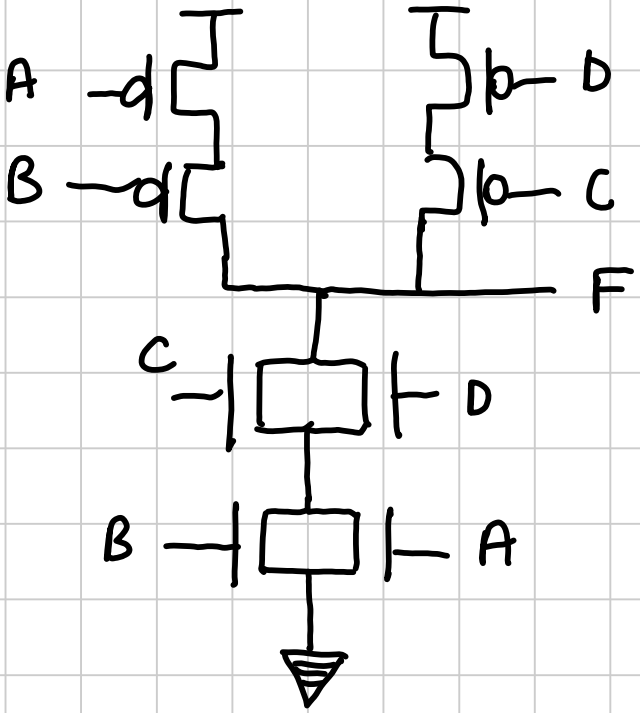


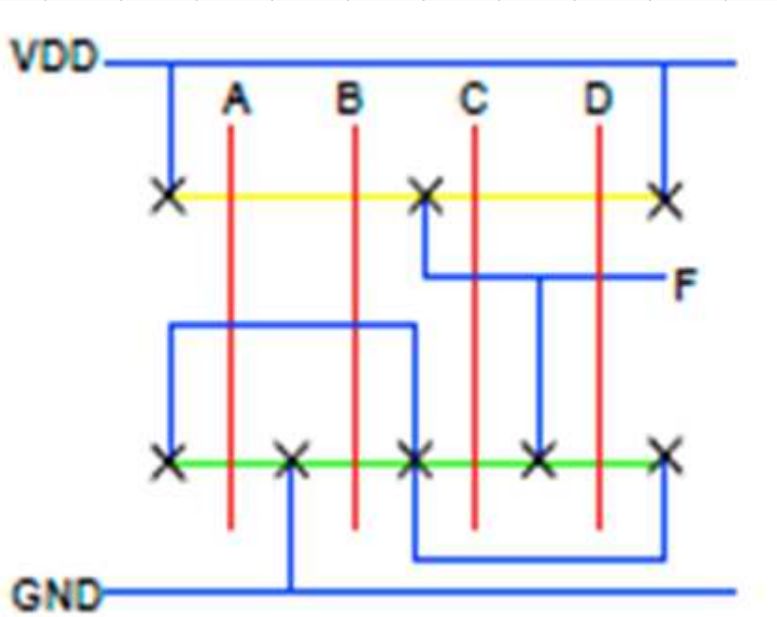




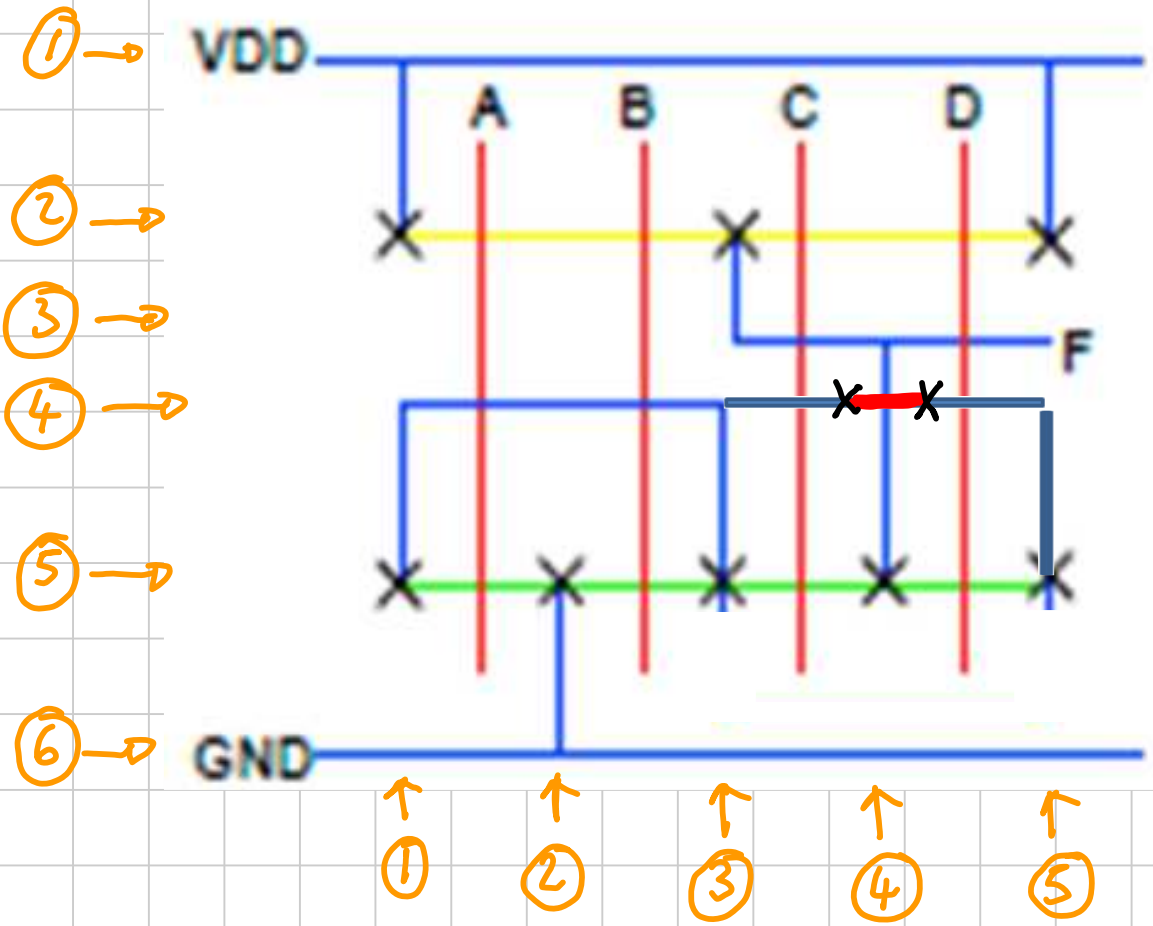
Problem #2

$$F = \overline{(A+B)\cdot(C+D)}$$





with little improvement



Level Sensitive Latch

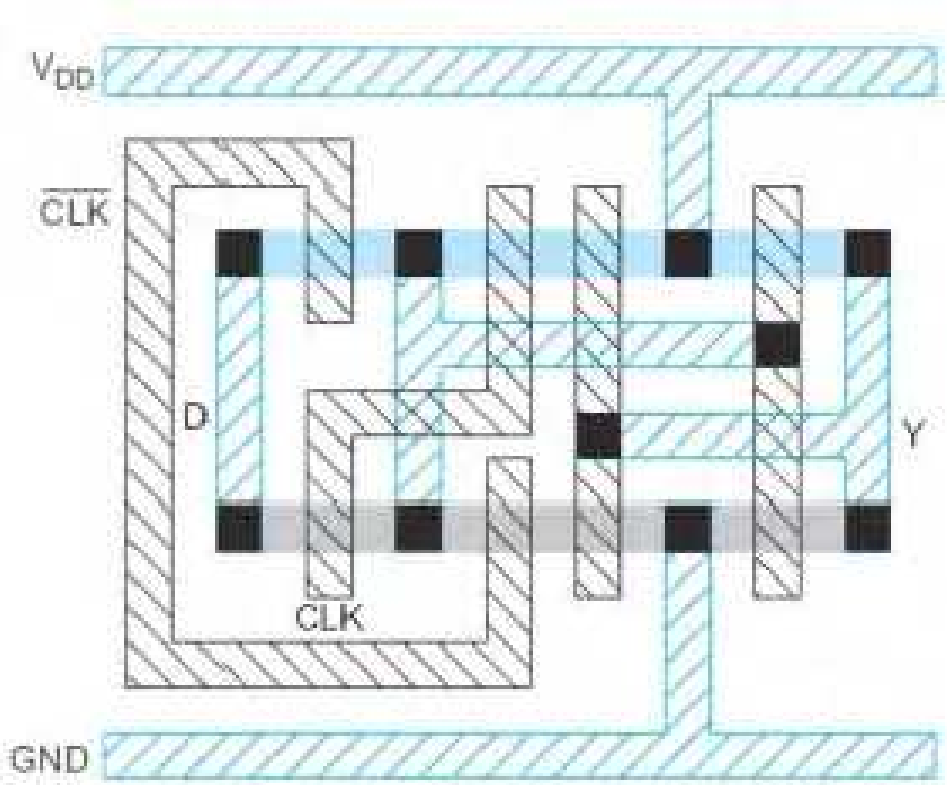
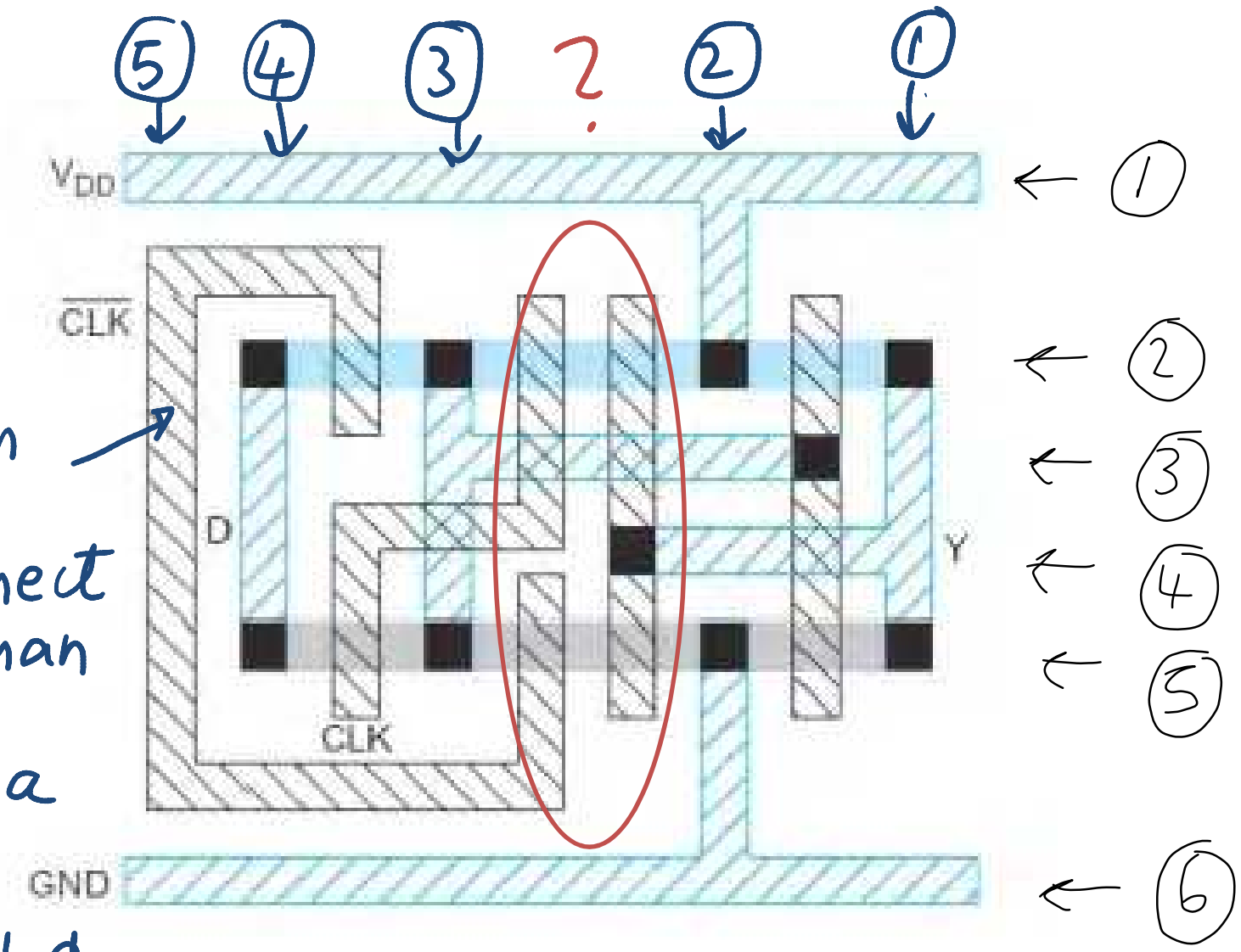


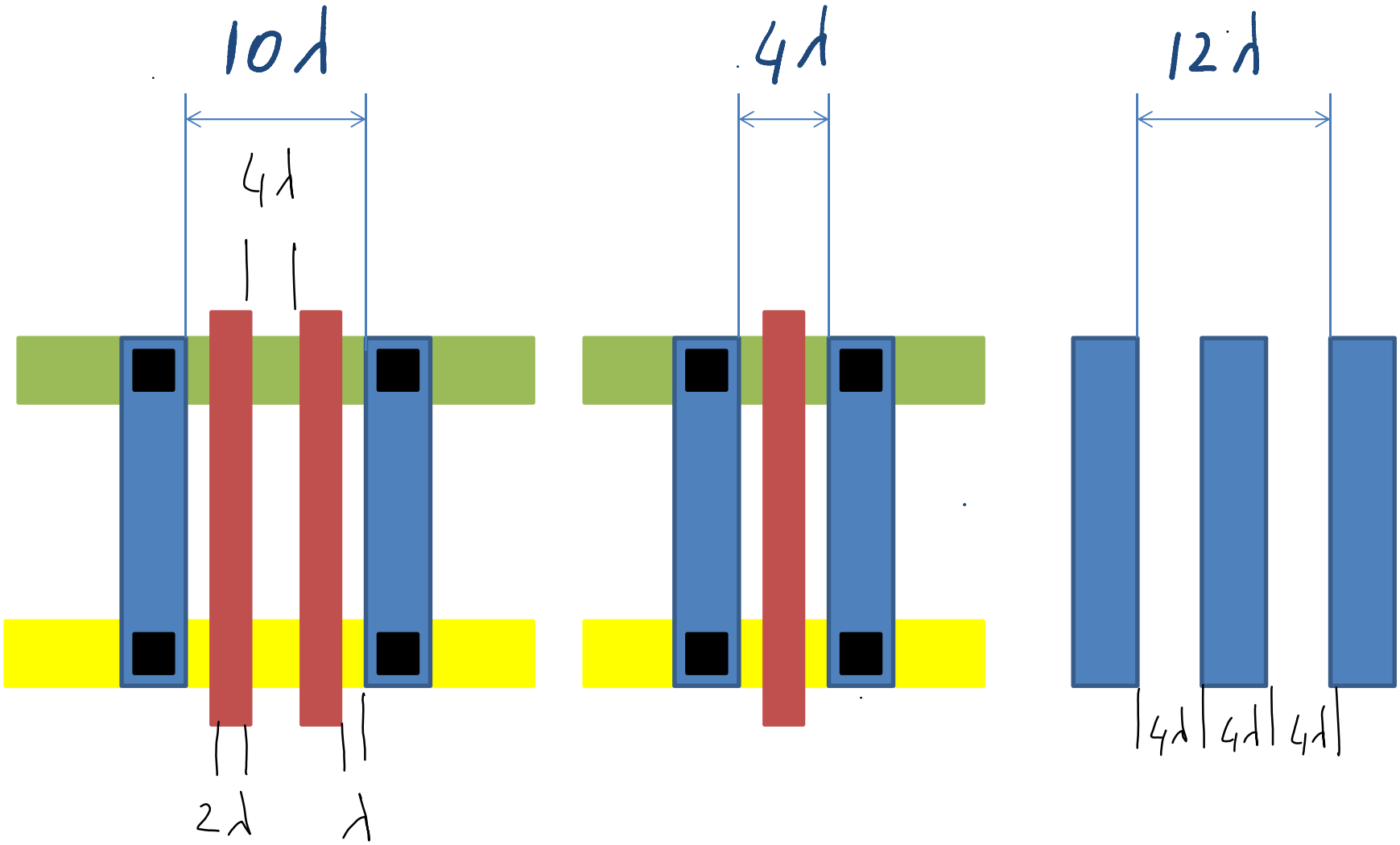
Fig.1.75 Level-sensitive latch stick diagram

Area Estimation



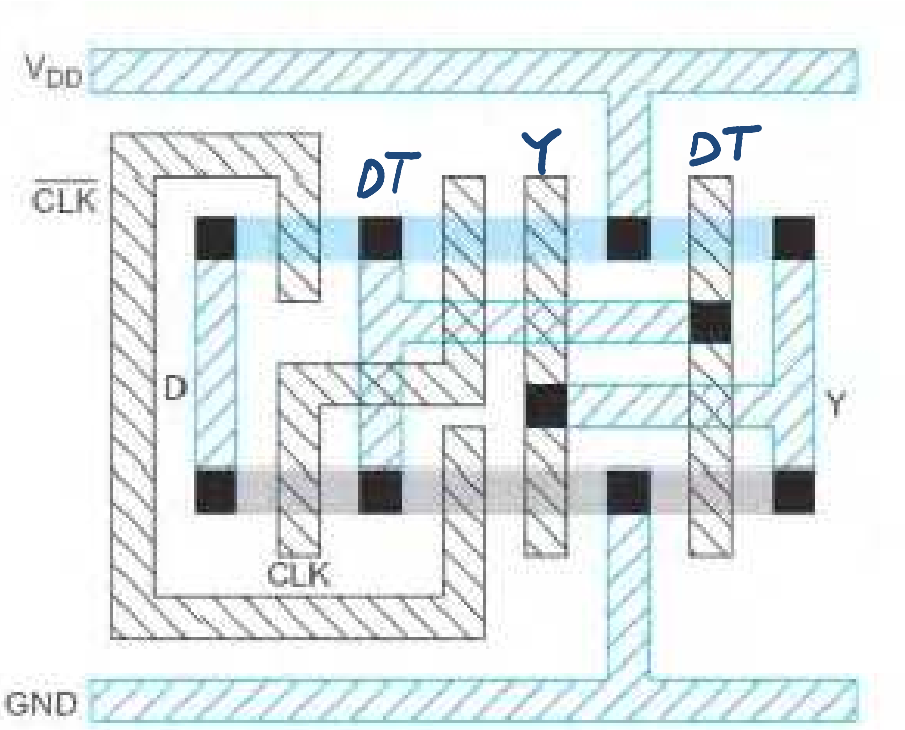
polysicon used as interconnect rather than for the gate of a MOSFET

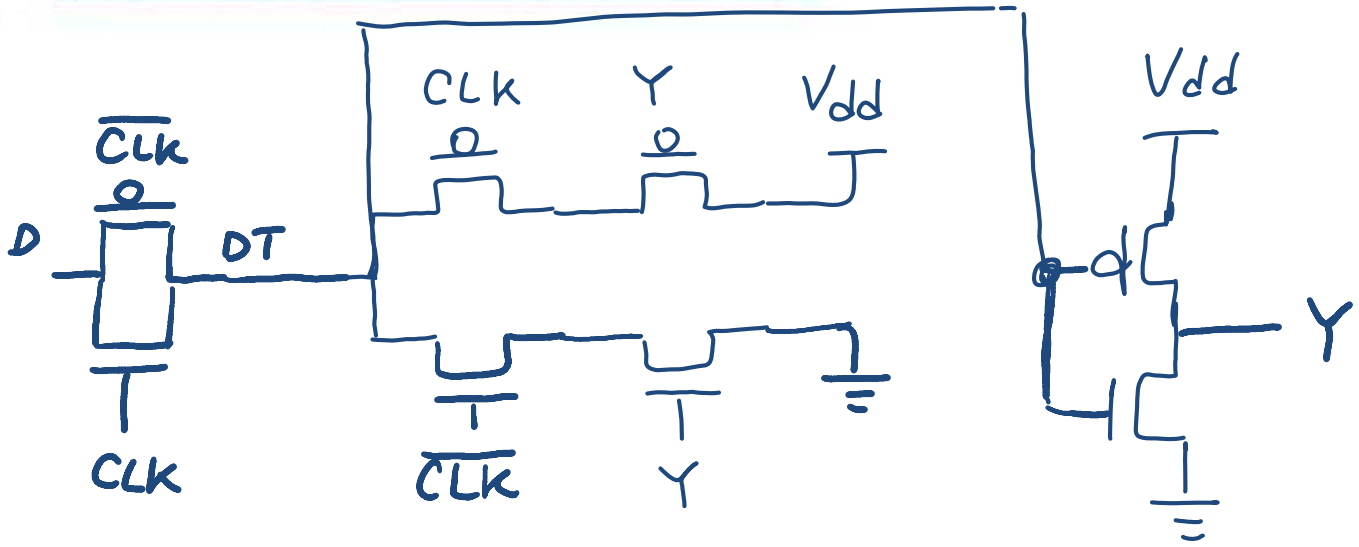
$R = \rho L / S$

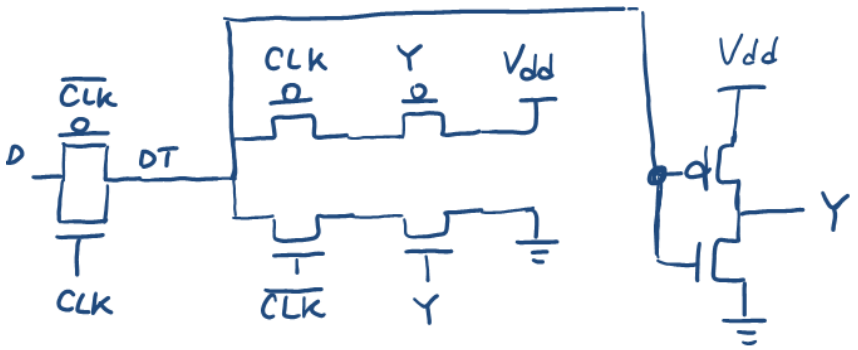


$10\lambda \approx 12\lambda$ = 1 extra track

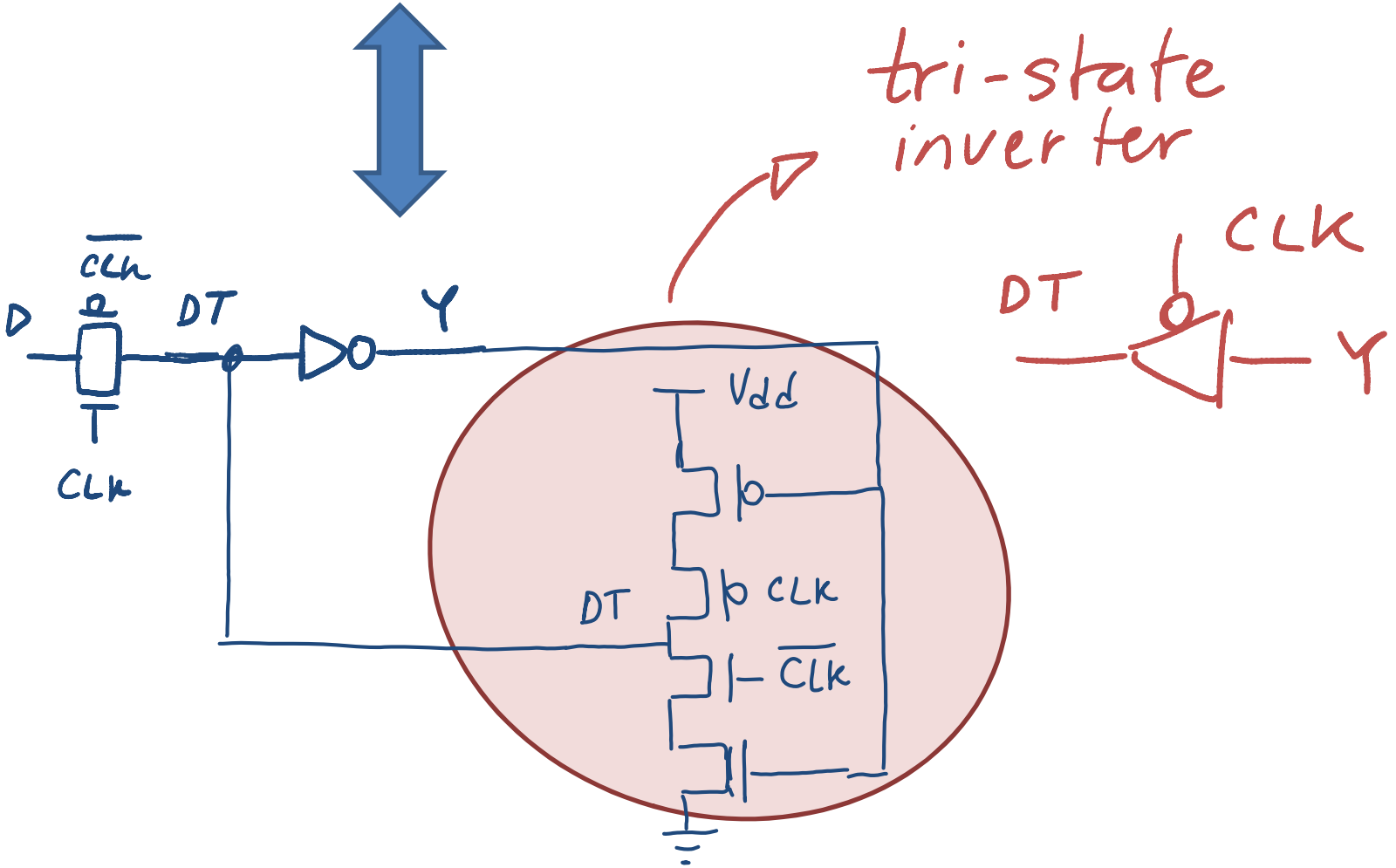
LVS






CLK
Y
Vdd
Vdd
CLK
D
DT
Y
CLK
CLK
Y

LVS


tri-state
inverter
CLK
DT
Y
CLK
D
DT
Y
CLK
Vdd
DT
CLK
CLK