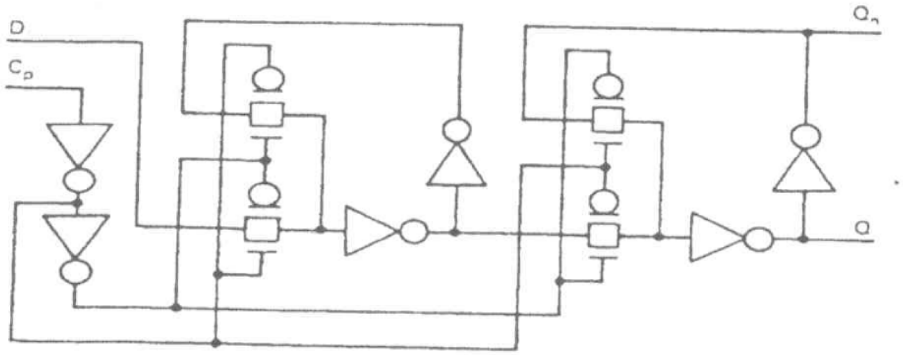
Source: J. DiGiacomo – VLSI Handbook- McGraw-Hill

7.7.2 *D/JK*-Type Flip-Flop

In a clocked system, synchronous flip-flops are preferred. Figure 7.35 shows a *D*-type flip-flop together with its excitation table. A *JK* flip-flop and its excitation table are shown in Fig. 7.36. Unlike the *RS* flip-flop, the *JK* flip-flop changes state when $J = K = 1$. Another example of a *JK* flip-flop with asynchronous SET-CLEAR capabilities is shown in Fig. 7.37. Active low signal CD (clear direct) and SD (set direct) will set the Q state to 0 and 1, respectively.

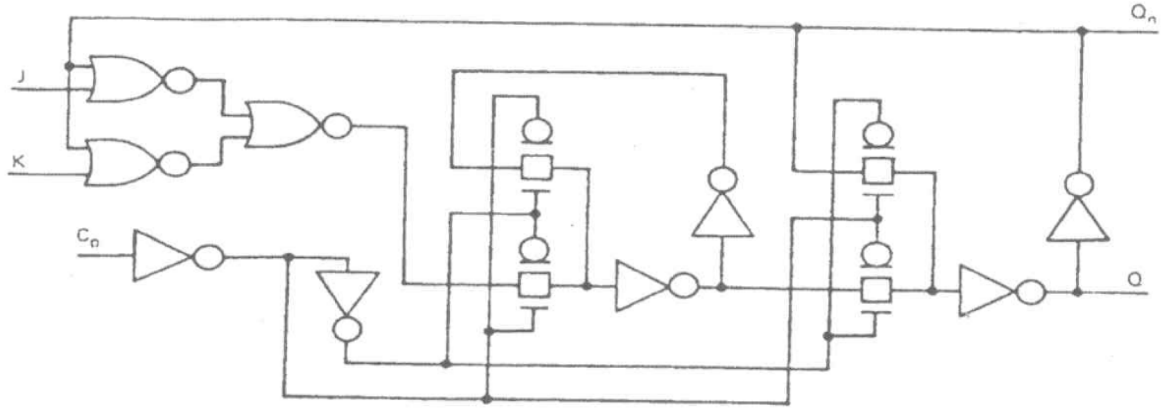
7.7.3 Data Setup Time

A flip-flop's setup time is the minimum time the data must be stable before the active edge of the clock occurs. The hold time is the minimum time the data must



D	C_p	Q	Q_n
0	↑	0	1
1	↑	1	0

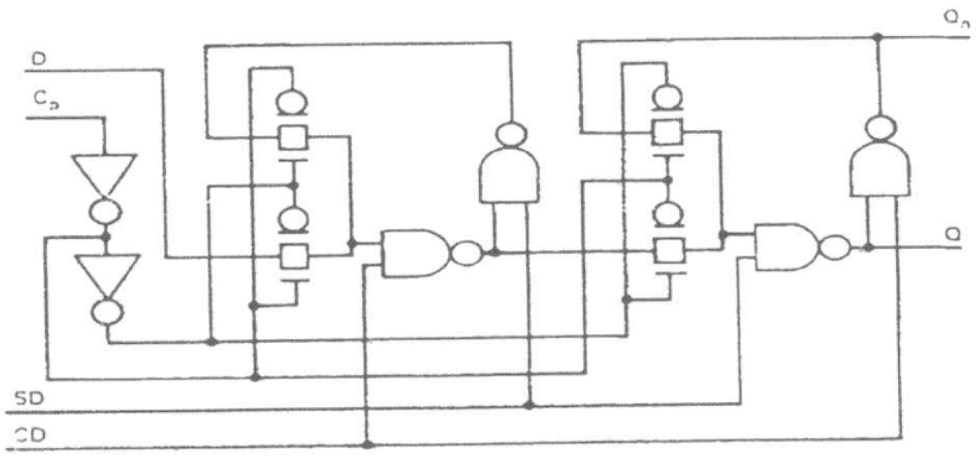
FIG. 7.35 *D*-type flip-flop.



J	K	C_p	Q	Q_n
0	0	↑	Q	Q_n
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	Q_n	Q

FIG. 7.36 *JK*-type flip-flop.

Source: J. DiGiacomo – VLSI Handbook- McGraw-Hill



D	C_p	CD	SD	Q	Q_n
0	↑	1	1	0	1
1	↑	1	1	1	0
×	×	0	1	0	1
×	×	1	0	1	0
×	×	0	0	1	1

FIG. 7.37 *D*-type flip-flop with clear direct and set direct.

be stable after the active edge of the clock. The timing is shown in Fig. 7.38. Both setup and hold times are functions of the internal delay of the master portion of the flip-flop only. They are independent of the loading on the Q and Q_n outputs. These timings can be calculated based on the various propagation delays of clock (C_p) and data (D, for example) signals.

In Fig. 7.39 when the clock input C_p is low, transmission gate G_4 is enabled and G_3 is disabled. Any signal changes occurring on the data pin will affect the outputs of G_5 and G_6. The result is a change in signal state that is set up on input of G_3. When the clock pin becomes high, G_3 is enabled and G_4 is disabled. As a result, the signal set up on G_3's input is latched in the master and transmitted to the slave latch. Since G_4 is disabled, any data changes occurring on the data pin are blocked out.

To meet the setup time requirement, the signal at G_3's input must be stable prior to the time that G_3 is enabled. Since any changes occurring on the data pin must go through G_4, G_5, and G_6 before reaching G_3, the setup time is the sum of the propagation delays through these latter three gates. However, the clock signal must go through G_1 and G_2 before enabling G_3. The setup time for the D flip-flop therefore is equal to the sum of the G_4, G_5, and G_6 propagation delays minus the sum of the G_1 and G_2 propagation delays:

$$T_{setup} = (T_{pdG_4} + T_{pdG_5} + T_{pdG6}) - (T_{pdG_1} + T_{pdG_2}) \qquad (7.34)$$

7.7.4 Data Hold Time

For the hold time requirement to be met, the data pin must not change state before G_4 is disabled (see the timing diagrams of Fig. 7.38 and Fig. 7.40). Since the clock signal must go through G_1 and G_2 before disabling G_4, the hold time is equal to the sum of the G_1 and G_2 propagation delays:

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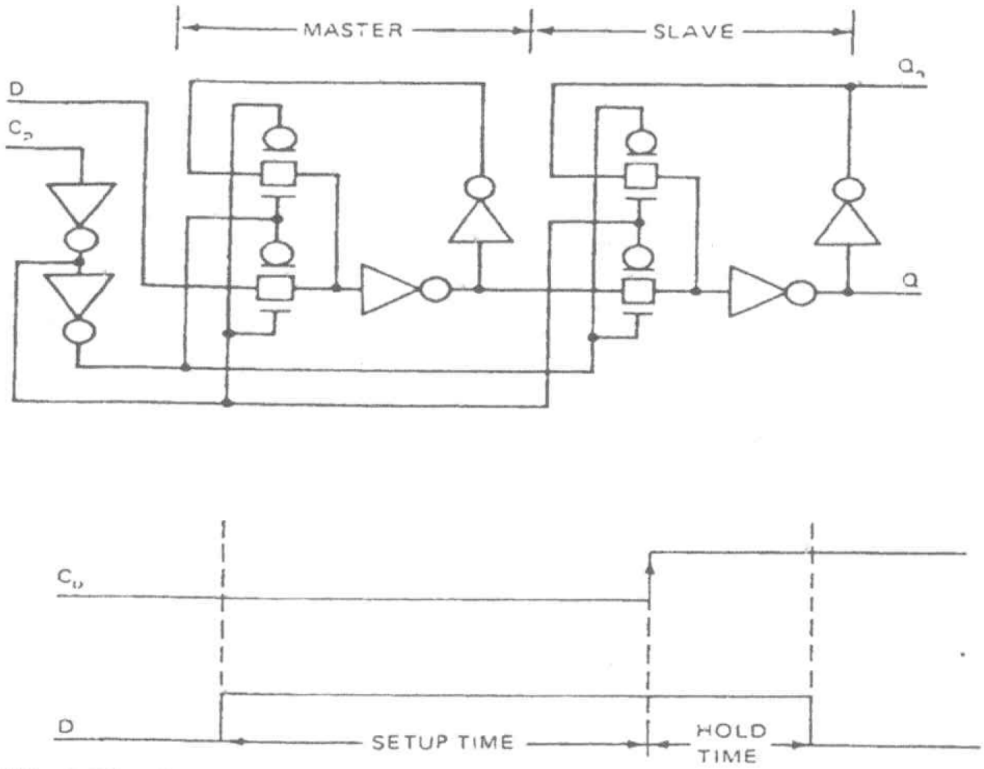

FIG. 7.38 Setup and hold time of *D* flip-flop.

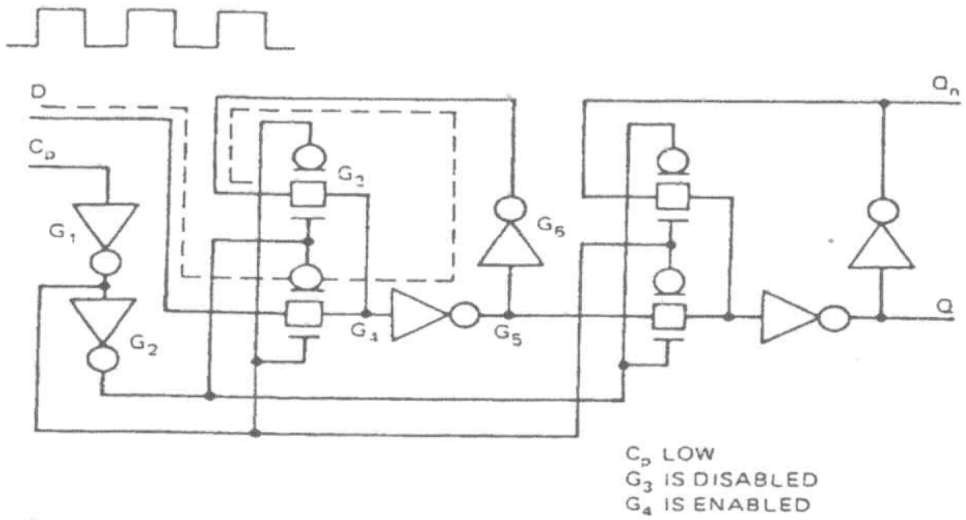

FIG. 7.39 Flip-flop setup time calculation with C_p low.

$$T_{\text{hold}} = T_{pdG_1} + T_{pdG_2} \tag{7.35}$$

7.7.5 Minimum Pulse Width

Another design consideration is the clock pulse width. As shown in Fig. 7.41, while the clock pin is low the signal from the data pin propagates through G_4, G_5,

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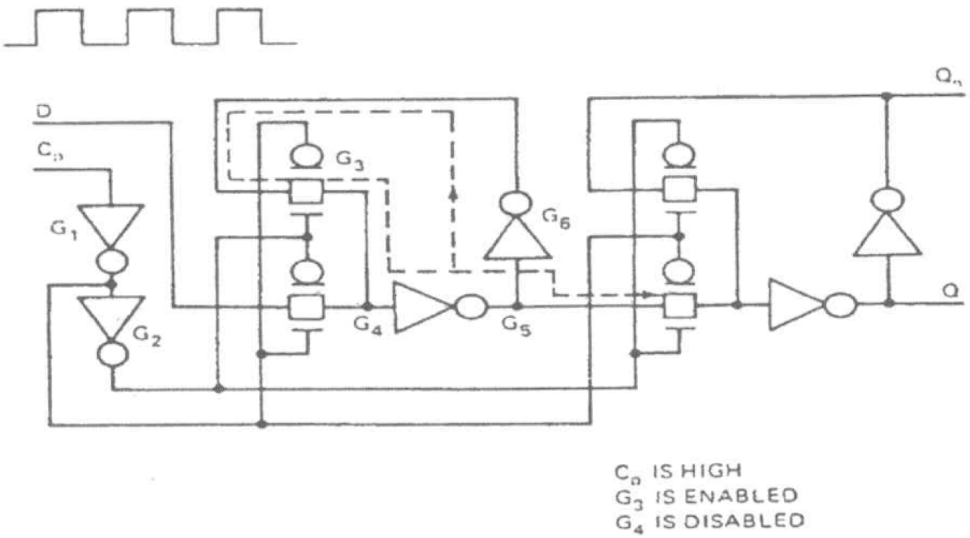

FIG. 7.40 Flip-flop hold time calculation with C_p high.

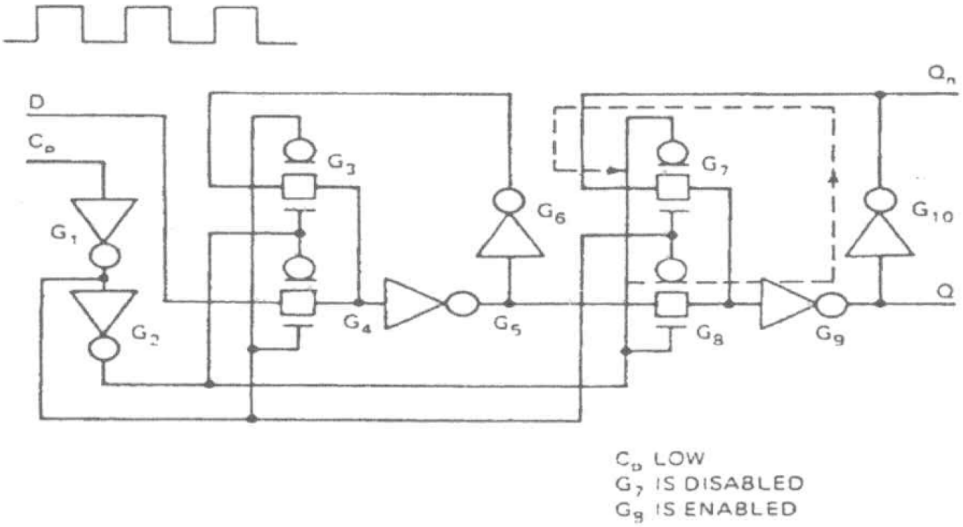

FIG. 7.41 Minimum positive clock width.

and G_6, and the signal is set up on the input of G_3. The clock signal must remain low during this period so that the master can latch in the correct data. The minimum negative pulse width is

$$T_{-pw} = T_{pdG_4} + T_{pdG_5} + T_{pdG_6} \tag{7.36}$$

As the clock is high, data are transferred from master to slave. The data signal propagates through G_8, G_9, and G_{10}, and the signal is set up on the input of G_7. The minimum positive pulse width is

$$T_{+pw} = T_{pdG_8} + T_{pdG_9} + T_{pdG_{10}} \tag{7.37}$$

The clock signal must remain high during this period, allowing the slave to latch in the correct data.

Since the master drives no external loads, the minimum negative pulse width T_{pw-} is independent of the loading on the Q and Q_n outputs. However, the slave drives external loads. If Q or Q_n drives high fan-out lines, then the propagation delay of G_9 and G_{10} increases the minimum clock pulse width for the flip-flop. This problem can be eliminated by adding inverters at Q and Q_n. The penalty is additional gate delay from the clock to Q and Q_n.

7.7.6 Other Considerations

The *RS* flip-flop in Fig. 7.33 is a level-sensitive element. It has the transparent property that the flip-flop output will follow the input changes. For edge-sensitive types of flip-flops (i.e., master-slave type), outputs change only when the clock input makes a specific transition. Subsequent changes of the data inputs have no effect until the next active transition occurs. These types of flip-flops are more often used in digital design.

From the above timing calculations, it is very obvious that clock skew is a serious concern in flip-flop design (clock skew concerns relative timing of the clock arriving at different flip-flops). A skewed clock signal will change all the timing requirements. To reduce the clock skew, keep clock line routing at a minimum, minimize the number of gates driven by the clock, and use a large buffer to drive all clock inputs. To reduce the effect of output loading on the minimum positive pulse width, buffer both Q and Q_n before using them to drive high fan-out lines.

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