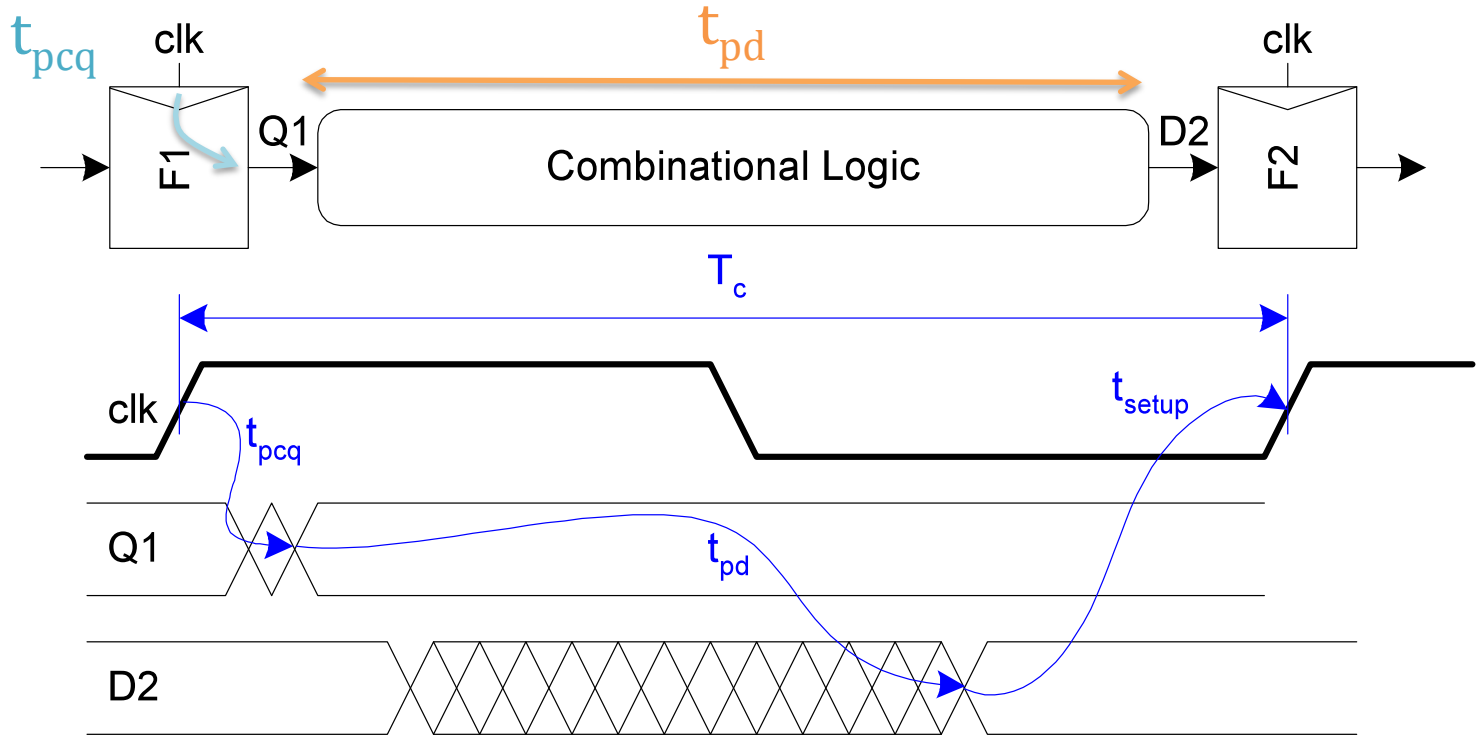
Flipflop based Sequential Systems: Max-delay, Min-delay, Clock Skew

Slides adapted from:

N. Weste, D. Harris, *CMOS VLSI Design*,

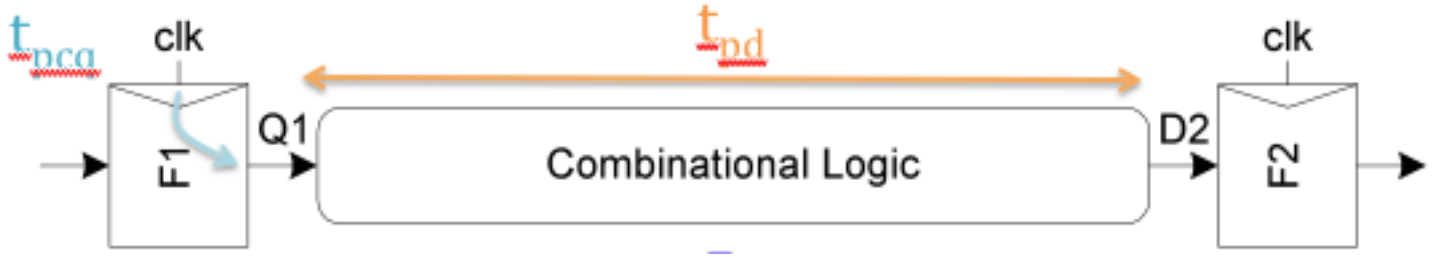
Max-Delay: Flip-Flops

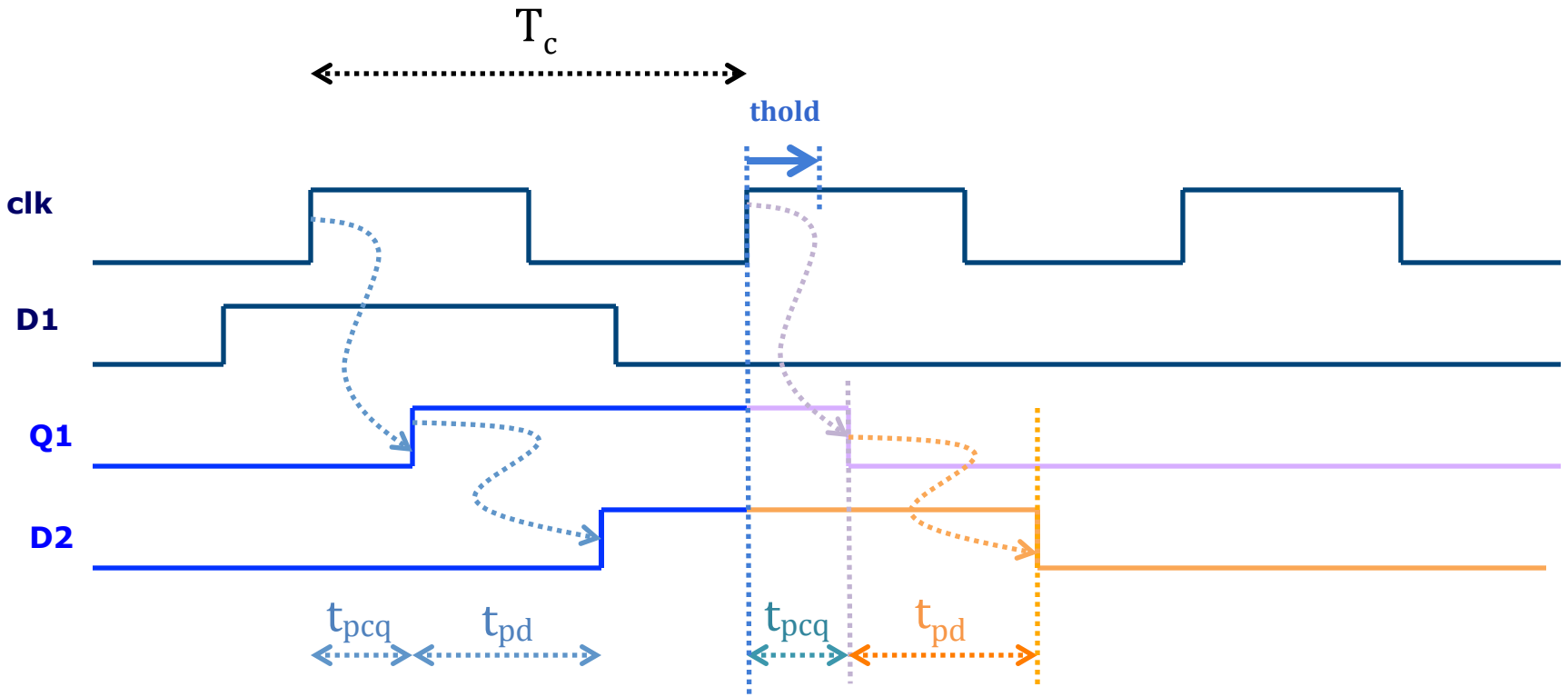


$$t_{pd} \leq T_c - \underbrace{\left(t_{\text{setup}} + t_{pcq}\right)}_{\text{sequencing overhead}}$$

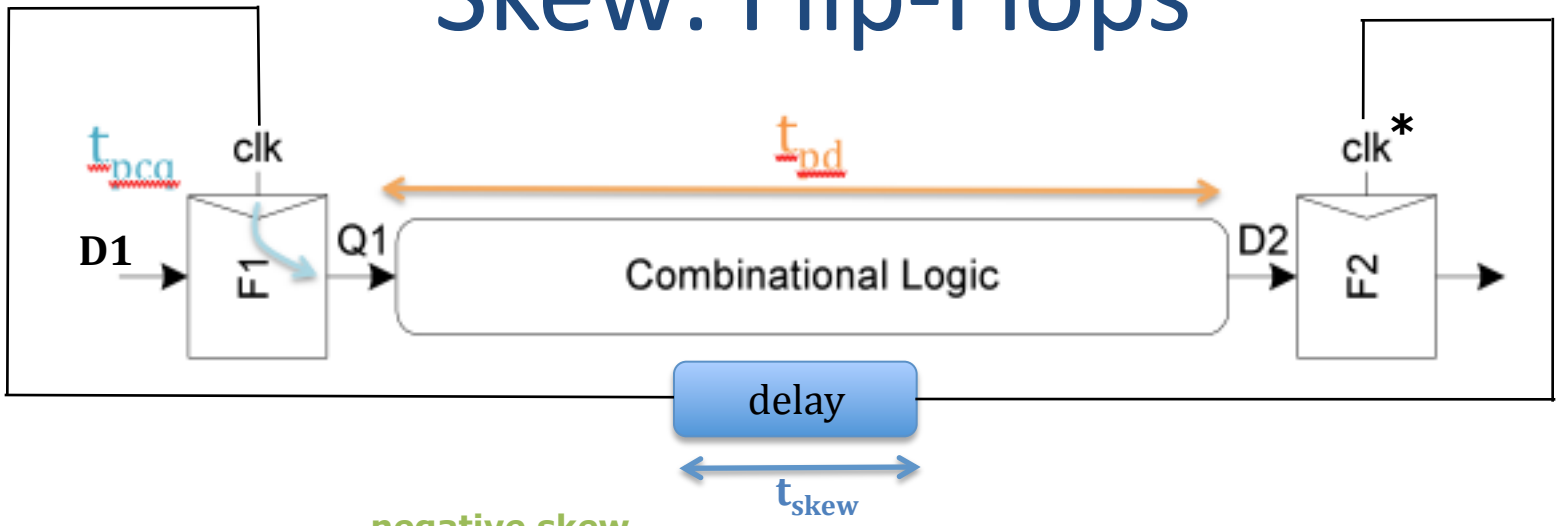
Min-Delay: Flip-Flops

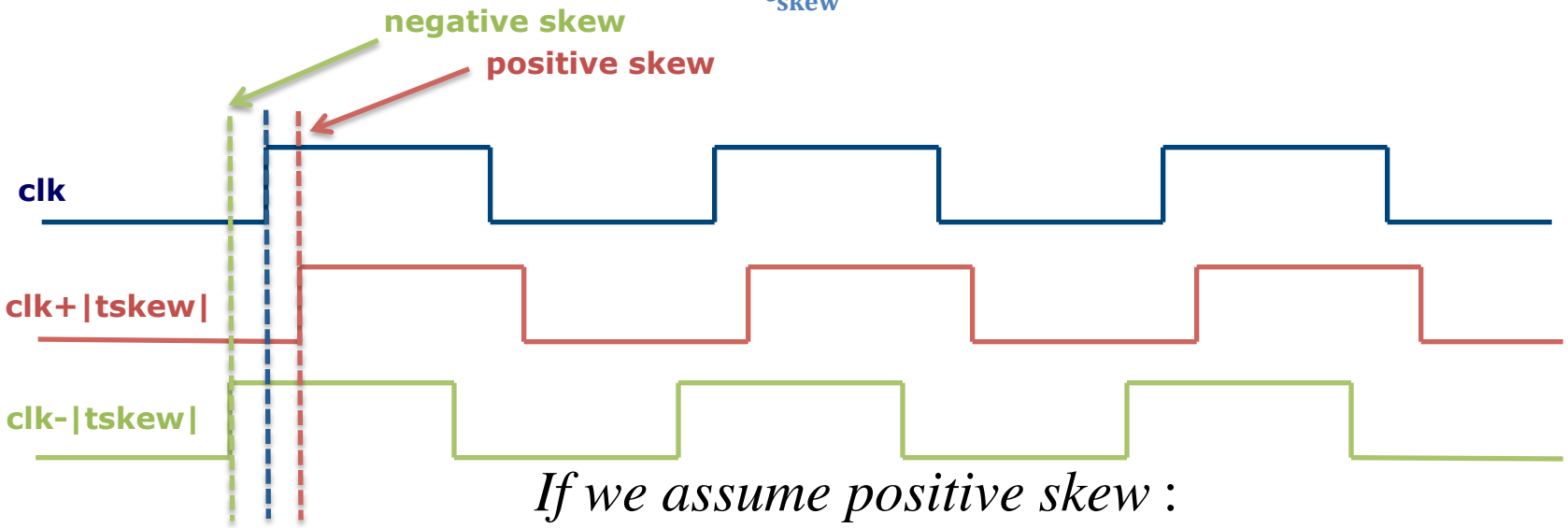
$$t_{pcq} + t_{pd} \geq t_{hold}$$





Skew: Flip-Flops





If we assume positive skew :

constraints gets "easier" → $T_c - t_{setup} \geq t_{pd} + t_{pcq} - |t_{skew}|$ ← Max-delay constraints

constraints gets "tougher" → $t_{hold} \leq t_{pd} + t_{pcq} - |t_{skew}|$ ← Min-delay constraints