Non Ideal Transistor Behavior

Slides adapted from:

N. Weste, D. Harris, *CMOS VLSI Design*,
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Non-ideal Transistor I-V effects

- Non ideal transistor Behavior
  - Channel Length Modulation
  - Threshold voltage effects
    - Body effect
    - Drain induced Barrier Lowering (DIBL)
    - Short Channel effects
  - High Field Effects
    - Mobility Degradation
    - Velocity Saturation
  - Leakage
    - Sub threshold Leakage
    - Gate Leakage
    - Junction Leakage
  - Process and Environmental Variations

Ideal Transistor I-V

- Schockley long channel transistor model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \ \& \ V_{gs} \geq V_t & \text{linear} \\ \dfrac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \ \& \ V_{gs} \geq V_t & \text{saturation} \end{cases}$$

$$\beta = \mu \frac{\varepsilon ox}{tox} \frac{W}{L}$$

Ideal vs. Simulated nMOS I-V plots

- 65 nm IBM process, VDD=1.0V

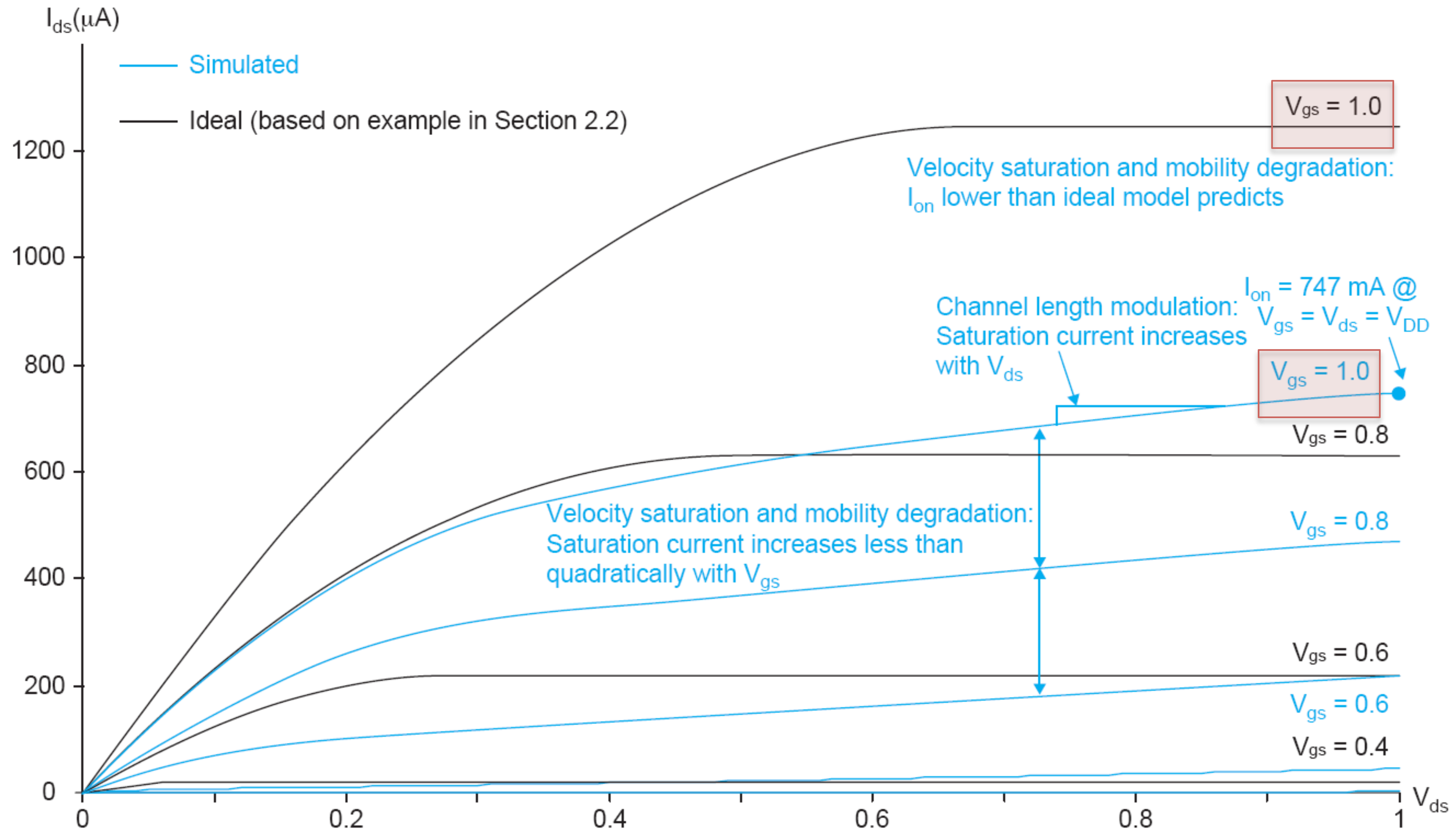
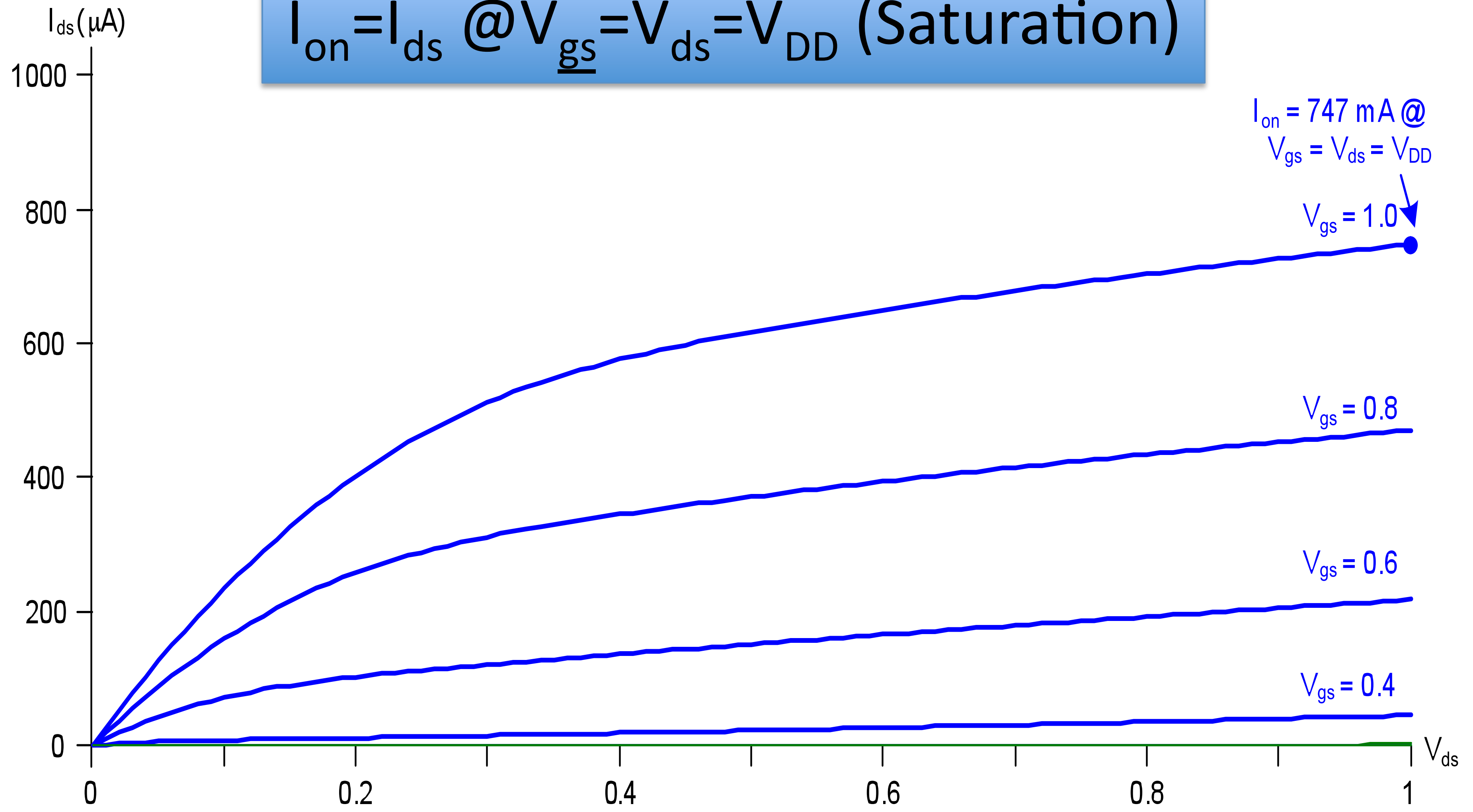


FIGURE 2.14 Simulated and ideal I-V characteristics

ON and OFF Current (1/3)



ON and OFF Current (2/3)

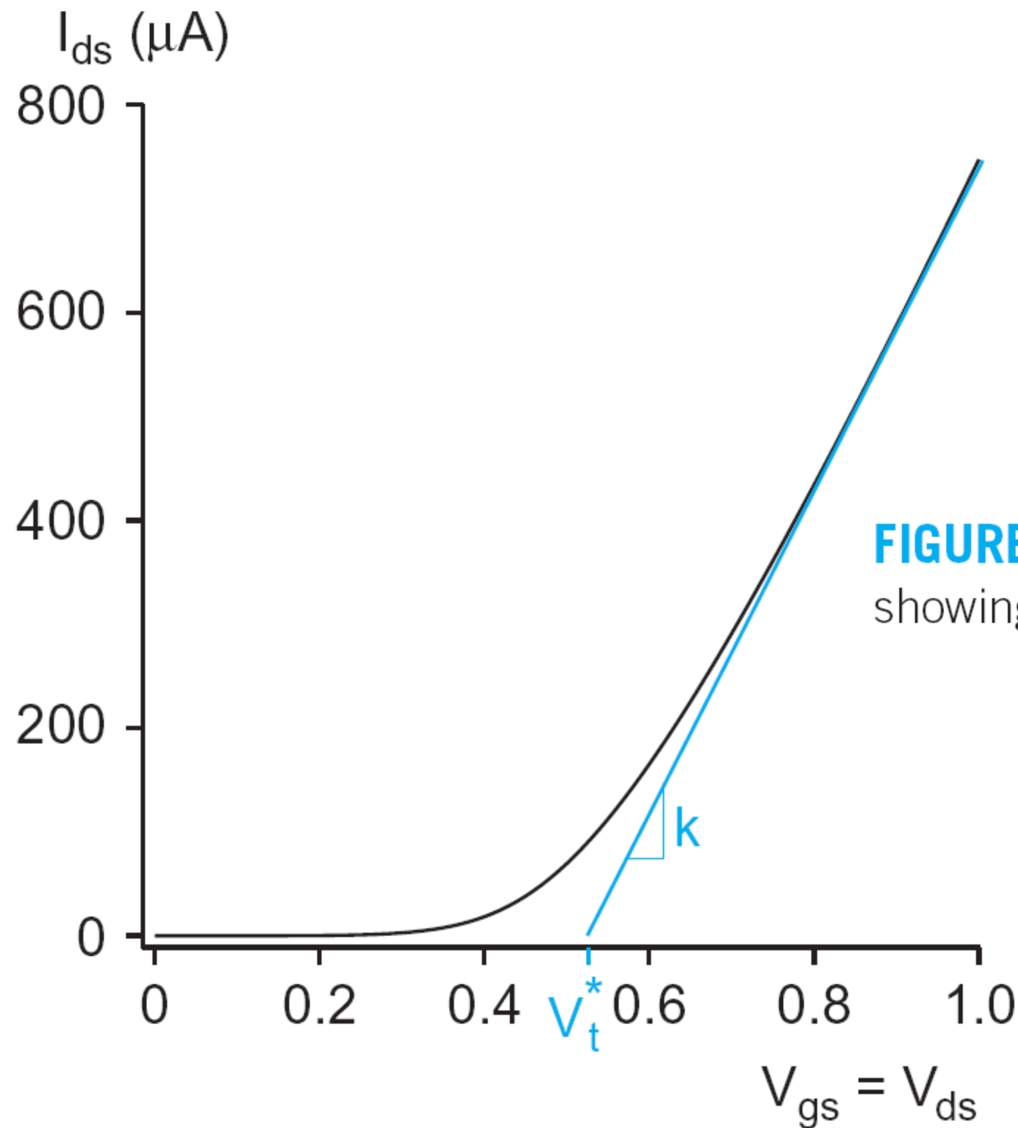
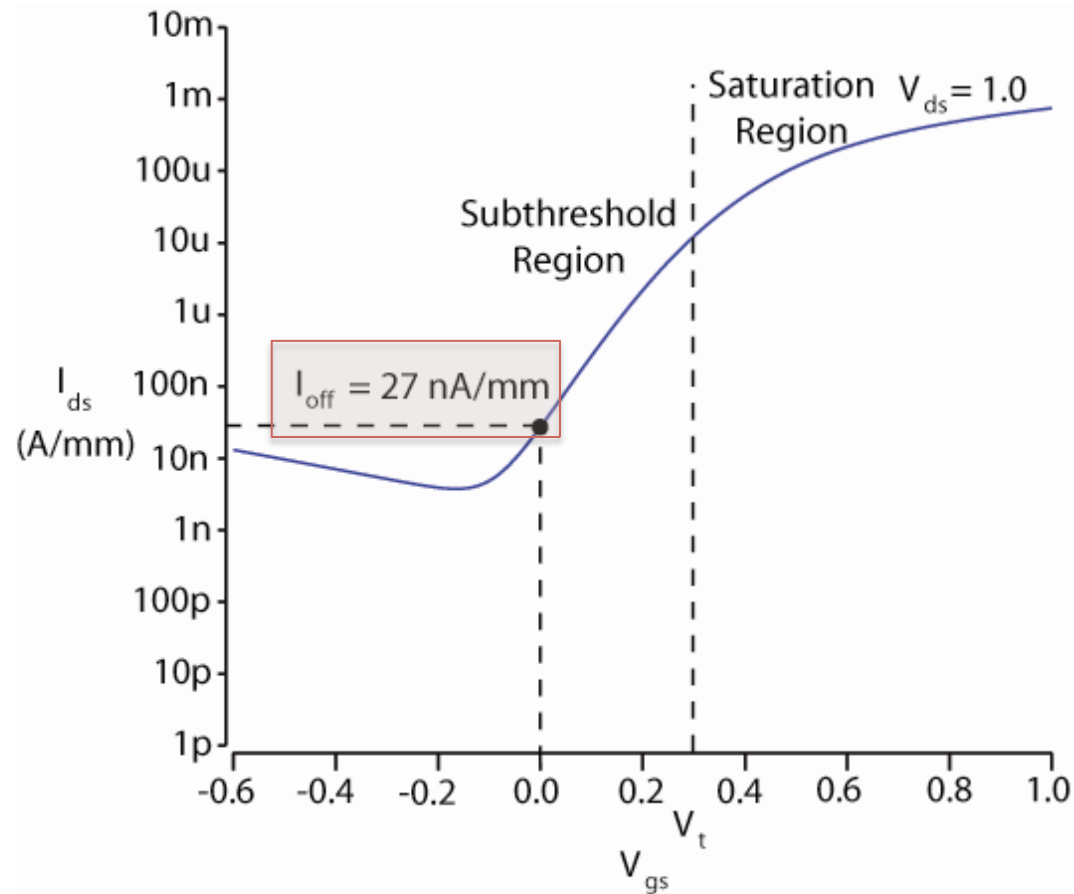


FIGURE 2.17 I_{ds} vs. V_{gs} in saturation, showing good linear fit at high V_{gs}

ON and OFF Current (3/3)

$I_{off} = I_{ds}$ @$V_{\underline{gs}} = 0$, $V_{ds} = V_{DD}$ (Cutoff)



Channel Length Modulation

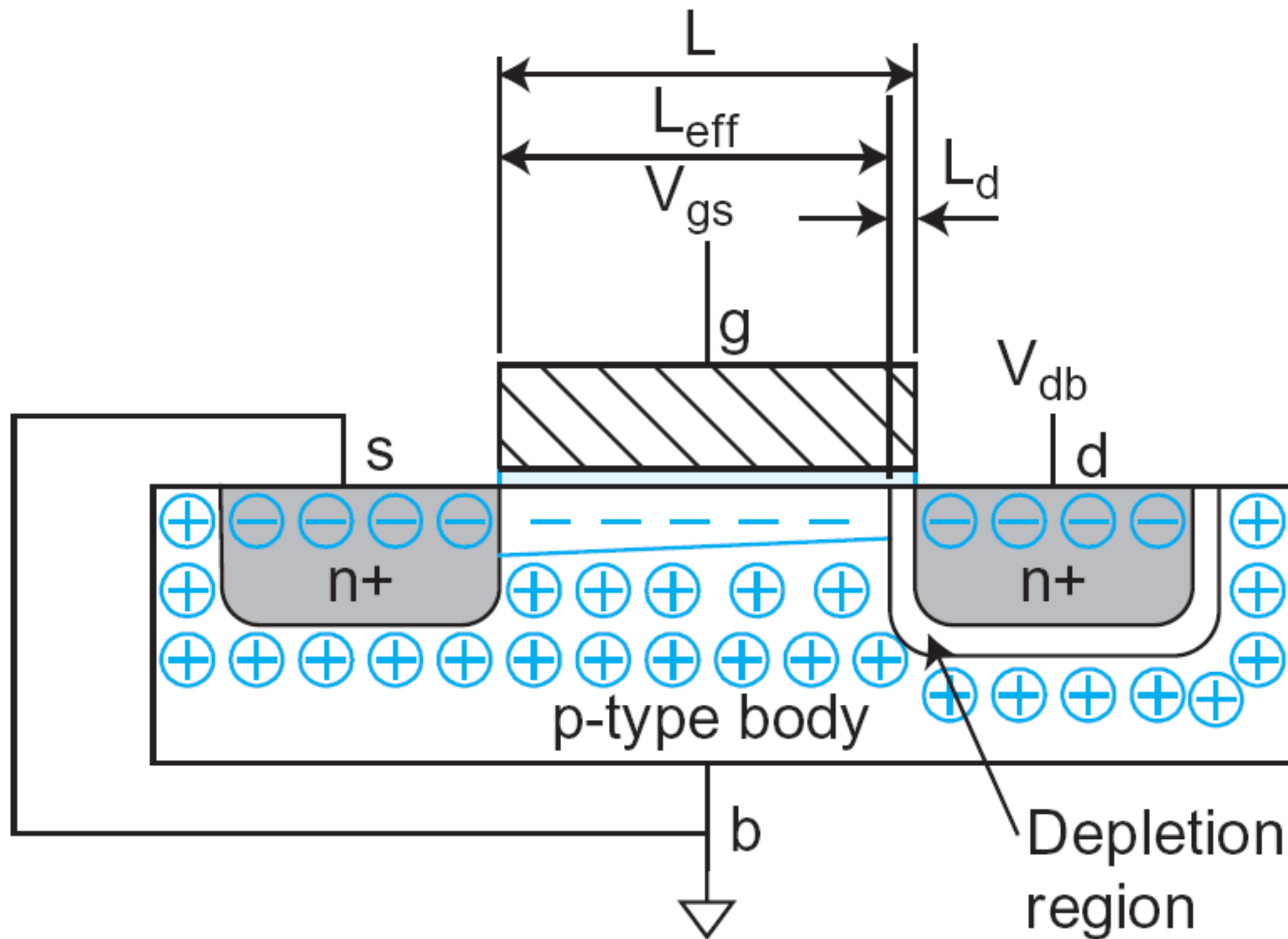
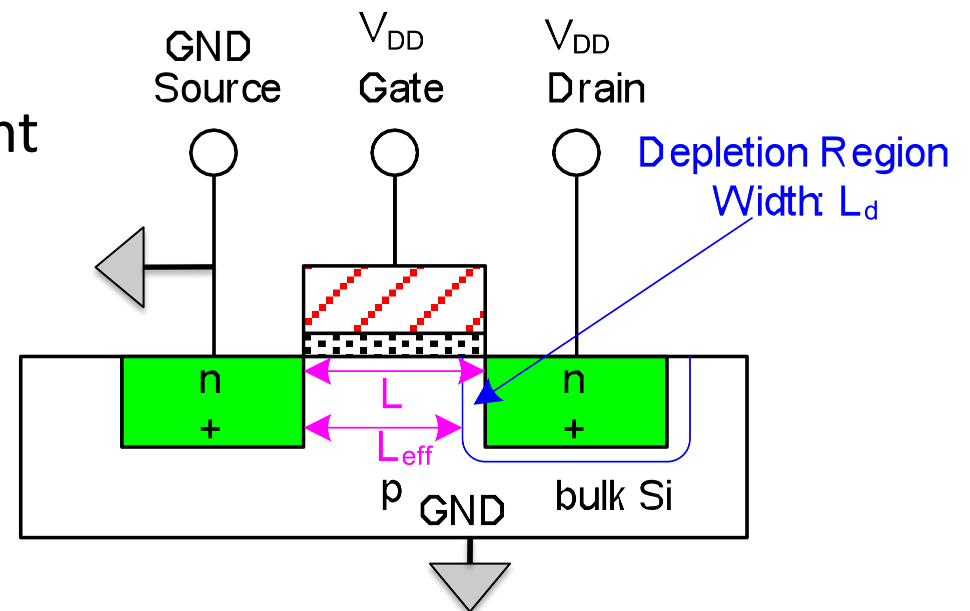


FIGURE 2.18 Depletion region shortens effective channel length

Channel Length Modulation

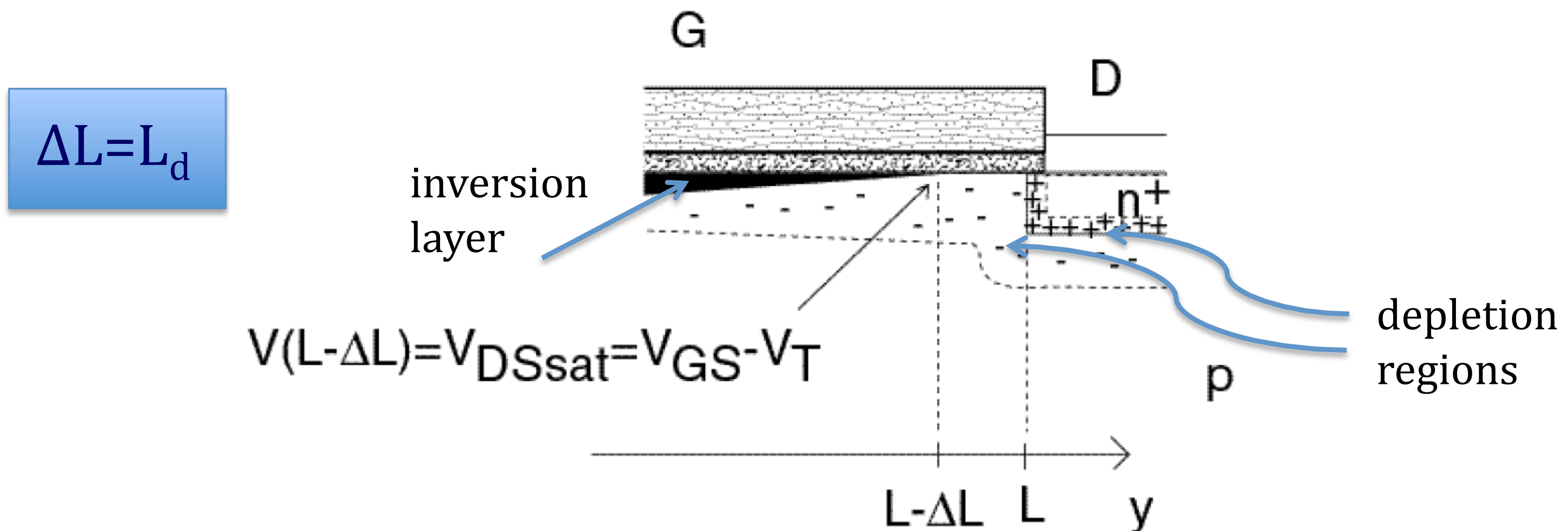
- Reverse-biased p-n junctions form a *depletion region*
  - Region between n (drain) and p (bulk) with no carriers
  - Width of depletion L_d region (between D and B) grows with reverse bias V_{db}
  - $L_{eff} = L – L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



Channel Length Modulation I/V (1/2)

- Increasing V_{ds} causes the depletion around the drain to widen.
- This pushes the pinch off point further away from the drain resulting in an effective shortening of the channel

$\Delta L = L_d$



Channel Length Modulation I-V (2/2)

$$I_{ds} \approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L - \Delta L(V_{ds})} (V_{gs} - V_t)^2$$

$$\approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L \cdot \left(1 - \frac{\Delta L(V_{ds})}{L}\right)} \cdot (V_{gs} - V_t)^2$$

Taylor's Approx

$$\approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(1 + \frac{\Delta L(V_{ds})}{L}\right) \cdot (V_{gs} - V_t)^2$$

$$\approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(1 + \lambda V_{ds}\right) \cdot (V_{gs} - V_t)^2$$

NOT THE FEATURE SIZE !!!

Lambda

- Lambda is inversely proportional to channel length

$$\lambda \propto \frac{1}{L}$$

- Lambda is a "fudge" factor (do not rely on a precise value of lambda)
- Improved but approximate model for the drain current in saturation:

$$I_{ds} \approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(1 + \lambda V_{ds}\right) \cdot (V_{gs} - V_t)^2 = \frac{\beta}{2} \cdot \left(1 + \lambda V_{ds}\right) \cdot (V_{gs} - V_t)^2$$

Electric Fields Effects

Mobility Degradation

Velocity Saturation

- Vertical electric field: $E_{vert} = V_{gs} / t_{ox}$
  - Attracts carriers into channel
  - Long channel: $Q_{channel} \propto E_{vert}$
- Lateral electric field: $E_{lat} = V_{ds} / L$
  - Accelerates carriers from drain to source
  - Long channel: $v = \mu E_{lat}$

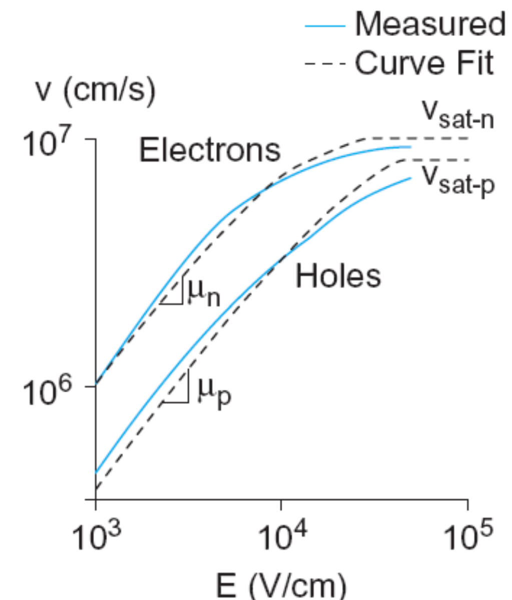
Mobility Degradation

- High E_{vert} effectively reduces mobility
  - Collisions with oxide interface (at high V_{gs}, carriers are buffeted against the oxide interface “wall”)

$$\mu_{\text{eff}-n} = \frac{540 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1 + \left(\frac{V_{gs} + V_t}{0.54 \frac{\text{V}}{\text{nm}} t_{\text{ox}}} \right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1 + \frac{\left| V_{gs} + 1.5 V_t \right|}{0.338 \frac{\text{V}}{\text{nm}} t_{\text{ox}}}}$$

Velocity Saturation

- At high E_{lat}, carrier velocity rolls off
  - Carriers scatter off (collide) atoms in silicon lattice (at high E_{lat} the carriers effective mass increases)
  - Velocity reaches v_{sat}
    - Electrons: 10^7 cm/s
    - Holes: 8×10^6 cm/s



$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \qquad E_c = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}}$$

Threshold Voltage Effects

- V_t is the value of V_{gs} for which the channel starts to invert
- Ideal models assume V_t is constant
- In reality it depends (weakly) on almost everything else:
  – Body voltage: *Body Effect*
  – Drain voltage: *Drain-Induced Barrier Lowering*
  – Channel length: *Short Channel Effect*

Body Effect

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{\Phi_s - V_{BS}} - \sqrt{\Phi_s}\right)$$

- The potential difference between source and body V_{SB} affects (increases) the threshold voltage
- Threshold voltage depends on:
  - V_{SB}
  - Process
  - Doping
  - Temperature

$$\gamma = \frac{\sqrt{2q\varepsilon_S N_{bulk}}}{\varepsilon_{ox}/t_{ox}} = Body\ \ Effect\ \ Coefficient \equiv GAMMA$$

$$\Phi_S = \frac{2KT}{q} \ln \frac{N_{bulk}}{n_i} = Surface\ \ Potential \equiv PHI$$

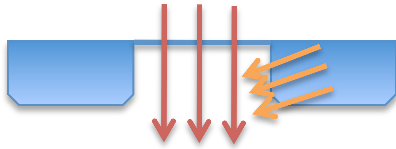
The higher the doping N_{bulk} the more voltage is required to produce an inversion layer: $N_{bulk} \uparrow \Rightarrow V_T \uparrow$

If C_{ox} is higher (= t_{ox} thinner) the less voltage is required to produce an inversion layer (Q=CV): $C_{ox} \uparrow \Rightarrow V_T \downarrow$

Body Effect

- V_{BS} affect the charge required to invert the channel
- For the same applied V_{GS}, the application of a negative V_{BS} *(we are only interested in a negative voltage to avoid forward biasing the bulk-to-source* pn junction) increases the width of the depletion region, thus the voltage required to invert the channel increases:

$$V_t = V_{t0} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$



DIBL

- So far we assumed the amount of charge in the channel is controlled only by the vertical field
- For short transistors and especially small oxide thickness the amount of charge also depends on the later field. The drain is essentially like another "gate".
- The drain cannot control the charge so well as the gate, but it also affect the amount of charge (and therefore the V_t)

$$V_t' = V_t - \eta V_{ds}$$

- High drain voltage causes current to increase

Short Channel Effect

- In small transistors the source/drain depletion regions extend into a significant portion of the channel
  - impacts the amount of change required to invert the channel
  - V_t typically increases with L (some processes exhibit a reverse short channel effect)

Leakage

- What about current in cutoff ?

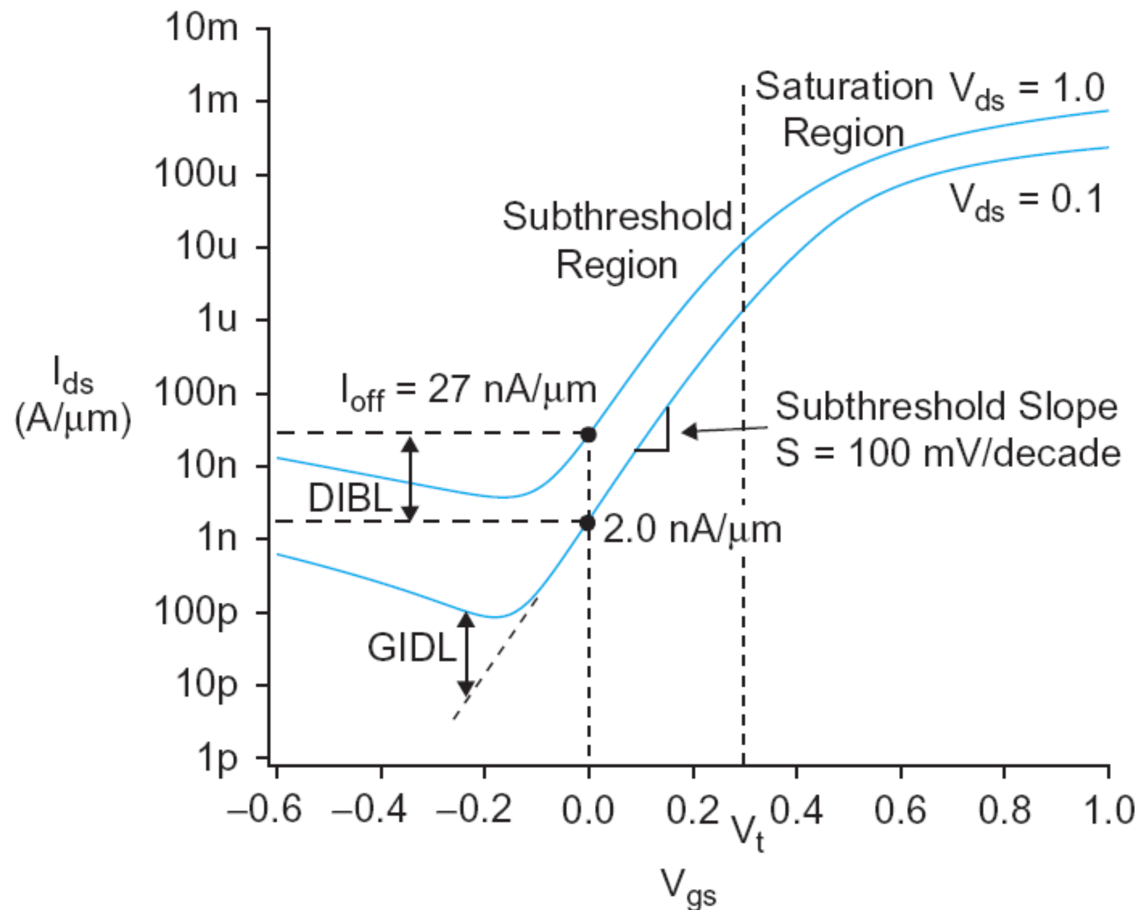


FIGURE 2.20 I-V characteristics of a 65 nm nMOS transistor at 70 °C on a log scale

Current doesn't go to 0 in cutoff !!!

Source of Leakage

- ***Subthreshold conduction***
  - Transistors can't abruptly turn ON or OFF
  - Dominant source in contemporary transistors
- ***Gate leakage***
  - Tunneling through ultrathin gate dielectric
- ***Junction leakage***
  - Reverse-biased PN junction diode current

Subthreshold Conduction

- In real transistors, current doesn't abruptly cut off below threshold, but rather drop off exponentially with V_{GS}
- This leakage current when the transistor is nominally OFF depends on:
  - process (ε_{ox}, t_{ox}) → hidden in K_γ
  - doping levels (N_{bulk}) → hidden in K_γ
  - device geometry (W, L) → hidden in I_{ds0}
  - temperature (T) → hidden in v_T=KT/q
  - Subthreshold voltage (V_t)

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_\gamma V_{sb}}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}} \right)$$

n is process dependent, typically 1.3-1.7

Gate Leakage

$$I_{gate} = WA\left(\frac{V_{DD}}{t_{ox}}\right)^2 e^{-B\frac{t_{ox}}{V_{DD}}}$$

A and B are tech constants

- There is a finite probability that carriers will tunnel through the thin gate oxide. This result in gate leakage current flowing into the gate. I_{gate} is greater for electrons (nMOS gates leak more)
- The probability drops off exponentially with t_{ox}
- For oxides thinner than 15-20 Å, tunneling becomes a critically important factor (at 65nm t_{ox}≈10.5 Å)

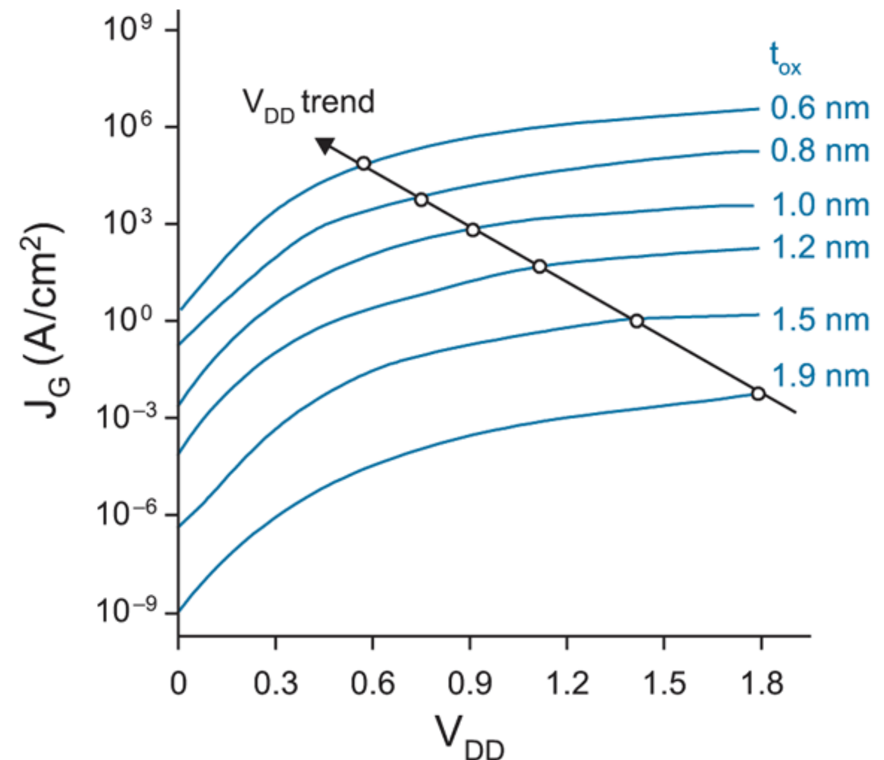


FIG 2.20 Gate leakage current from [Song01]

Junction Leakage

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- The p-n junctions between diffusion and the substrate or well for diodes.
- The well-to-substrate is another diode
- Substrate and well are tied to GND and VDD to ensure these diodes remain reverse biased
- But, reverse biased diodes still conduct a small amount of current that depends on: (I_S is typically < 1fA/μm^2)
  - Doping levels
  - Area and perimeter of the diffusion region
  - The diode voltage

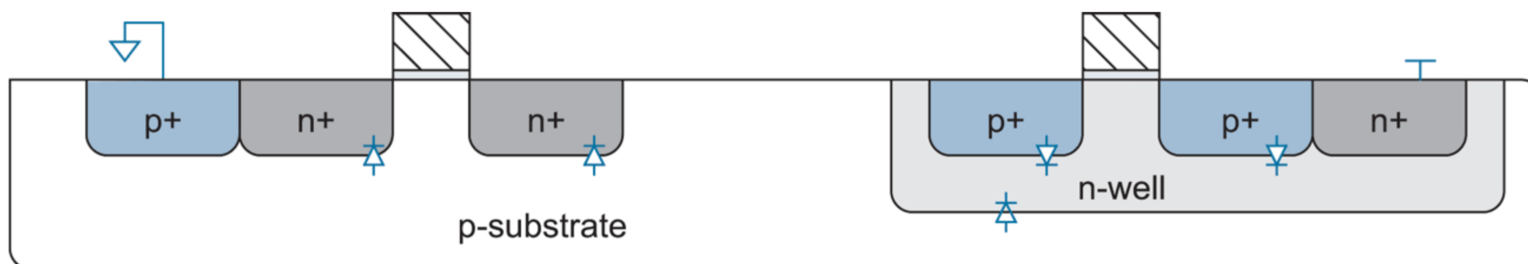


FIG 2.19 Reverse-biased diodes in CMOS circuits

Temperature dependence

- Transistor characteristics are influenced by temperature
  - µ decreases with T
  - V_t decreases linearly with T
  - $I_{leakage}$ increases with T
- ON current decreases with T
- OFF current increases with T
- Thus, circuit performances are worst at high temperature

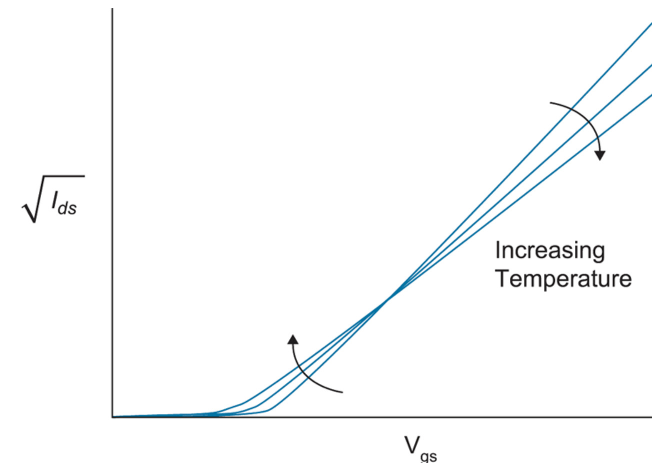


FIG 2.21 I–V characteristics of nMOS transistor in saturation at various temperatures

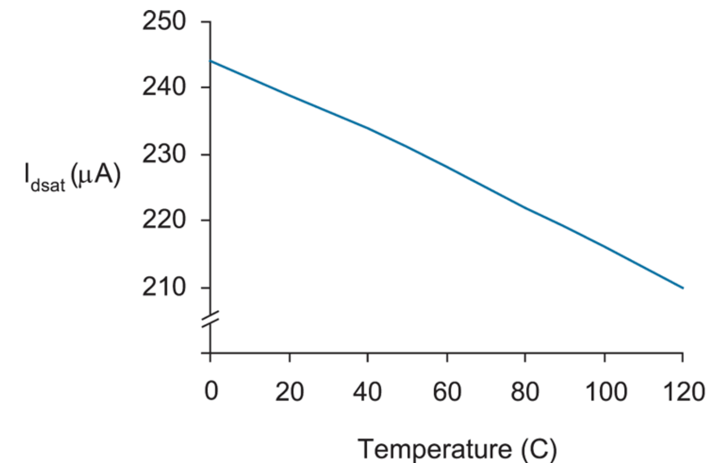


FIG 2.22 I_{dsat} vs. temperature

Geometry Dependence

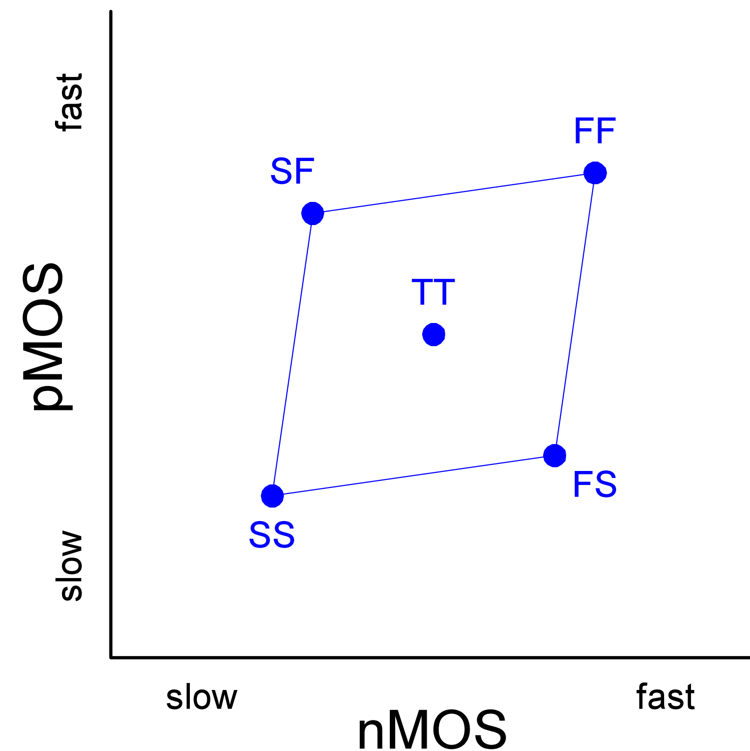
- Layout designers draw transistors with W_{drawn} L_{drawn}
- Actual dimensions may differ from some factor X_W and X_L
- The source and drain tend to diffuse laterally under the gate by L_D, producing a shorter effective channel
- Similarly, diffusion of the bulk by W_D decreases the effective channel width
- In process below 0.25 µm the effective length of the transistor also depends significantly on the orientation of the transistor

$$L_{eff} = L_{drawn} + X_L - 2L_D$$

$$W_{eff} = W_{drawn} + X_W - 2W_D$$

Process Variation

- Transistors have uncertainty in process parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
- Variation is around typical (T) values
- Fast (F)
  - L_{eff}: short
  - V_t: low
  - t_{ox}: thin
- Slow (S): opposite
- Not all parameters are independent
  for nMOS and pMOS



Environmental Variation

- V_{DD} and *Temperature* also vary in *time* and *space*
- *Fast:*
  - V_{DD}: high
  - T: low

Corner	Voltage	Temperature
F	1.98	0 C
T	1.8	70 C
S	1.62	125 C

Process Corners

- Process corners describe worst case variations
  - If a design works in all corners, it will ***probably*** work for any variation.
- Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

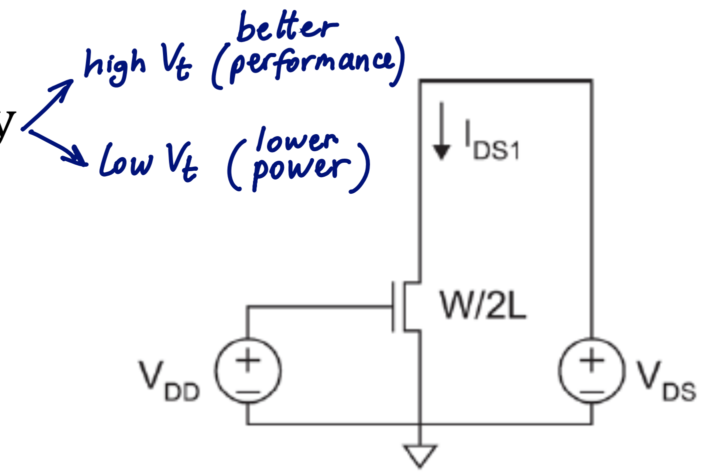
Important Corners

- Critical Simulation Corners include

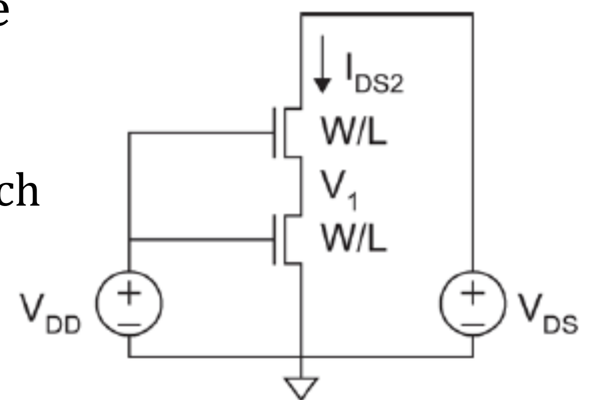
Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time	S	S	S	S
Power	F	F	F	F
Subthreshold leakage	F	F	F	S

Impact of non-ideal I-V effects

- Threshold is a significant fraction of the supply voltage
- Leakage is increased causing gates to
  - consume power when idle
  - limits the amount of time that data is retained
- Leakage increases with temperature
- Velocity saturation and mobility degradation result in less current than expected at high voltage
  - No point in trying to use high VDD to achieve fast transistors
  - Transistors in series partition the voltage across each transistor thus experience less velocity saturation
    - Tend to be a little faster than a single transistor
    - Two nMOS in series deliver more than half the current of a single nMOS transistor of the same width
- Matching: same dimension and orientation



(a)



(b)

FIG 2.37 Current in series transistors

So What?

- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Logical effort
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation