MOS Transistor Theory

Slides adapted from:

N. Weste, D. Harris, *CMOS VLSI Design*,

Outline

- The Big Picture
- MOS Structure
- Ideal I-V Characteristics
- MOS Capacitance Models
- Non ideal I-V Effects
- Pass transistor circuits
- Tristate Inverter
- Switch level RC Delay Models

The Big Picture

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V/\Delta t) \rightarrow \Delta t = (C/I)\Delta V$
  - Capacitance and current determine speed

MOS Transistor Symbol

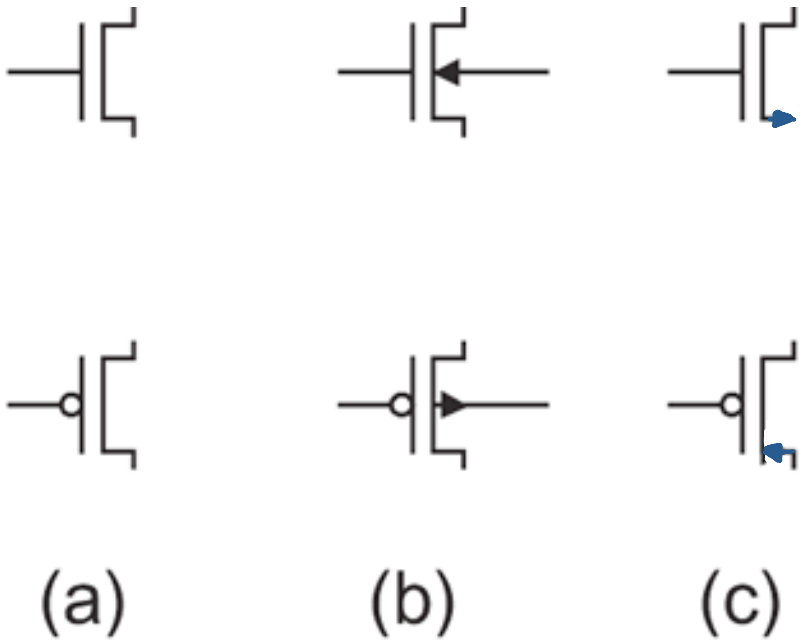
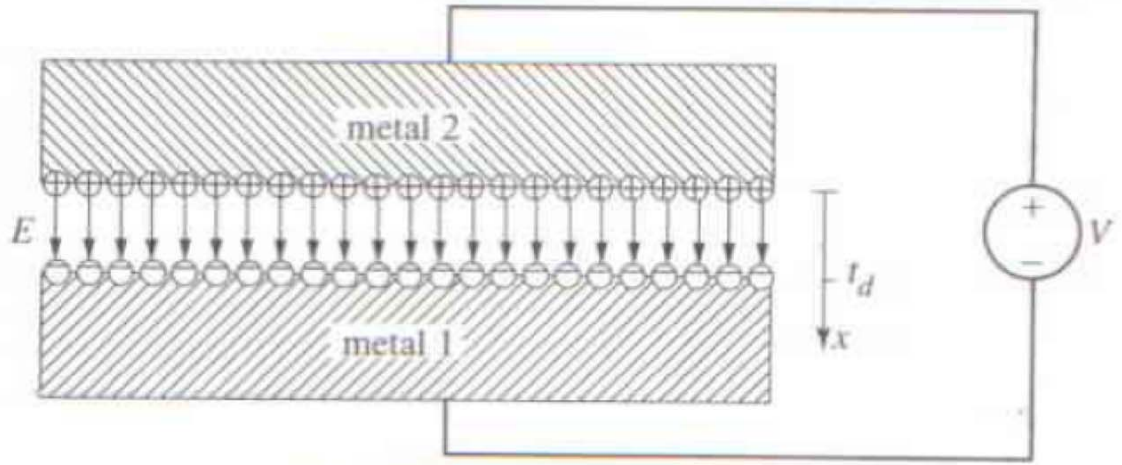


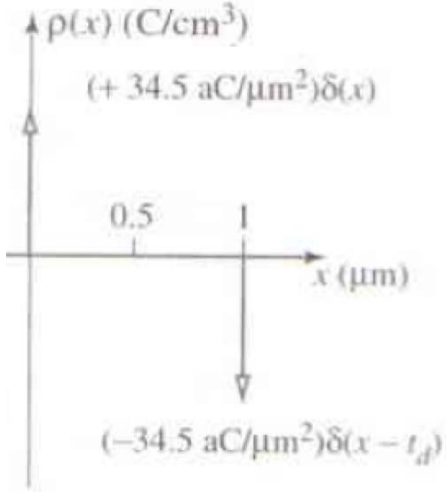
FIG 2.1 MOS transistor symbols

Metal-to-metal Capacitor

Source:
R. Howe, C. Sodini
Microelectronics. An Integrated Circuits Approach, Prentice Hall



➤ **Figure Ex3.1B** Close-up of metal-metal capacitor with applied voltage, showing surface charges on top and bottom metal plates and electric field lines.



Example:
Charge density for the capacitor with td=1μm, and silicon oxide as dielectric $\varepsilon ox=3.9\varepsilon_0$

MOS Structure

- Gate and body for MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion

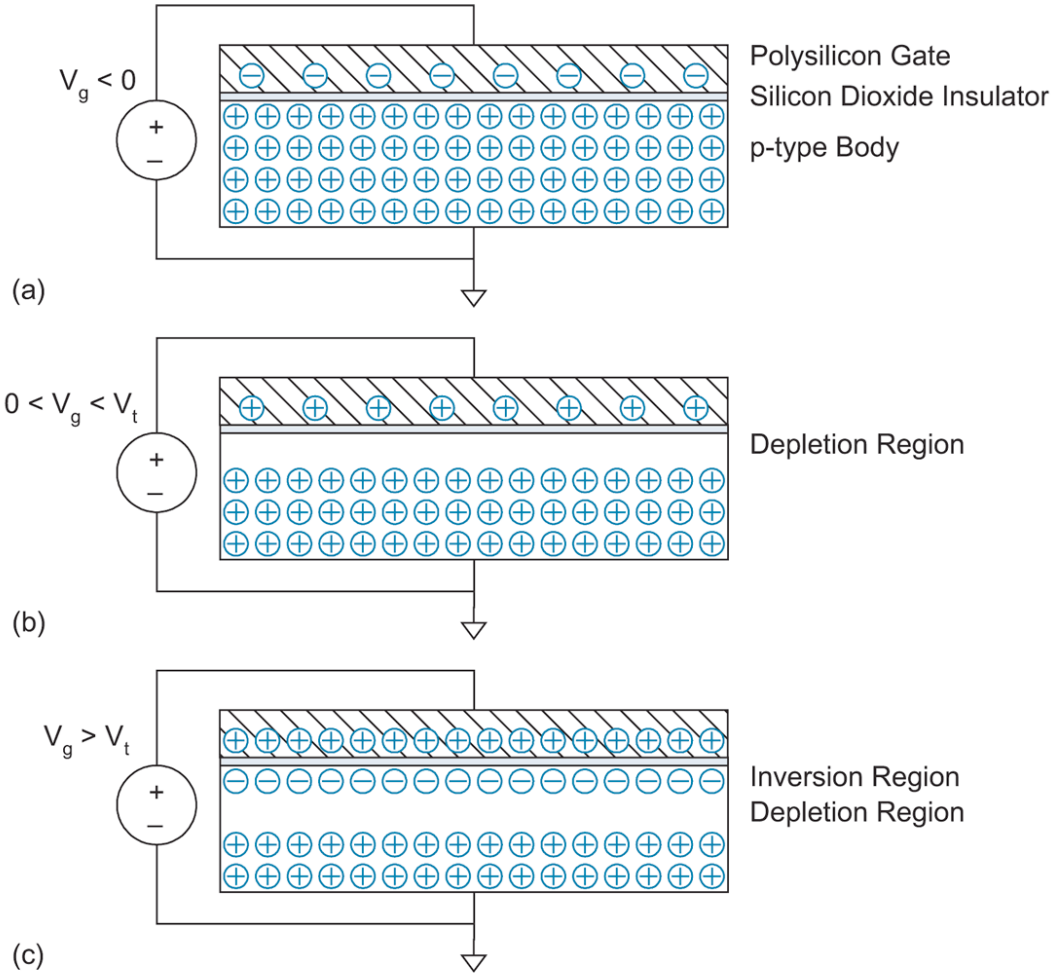
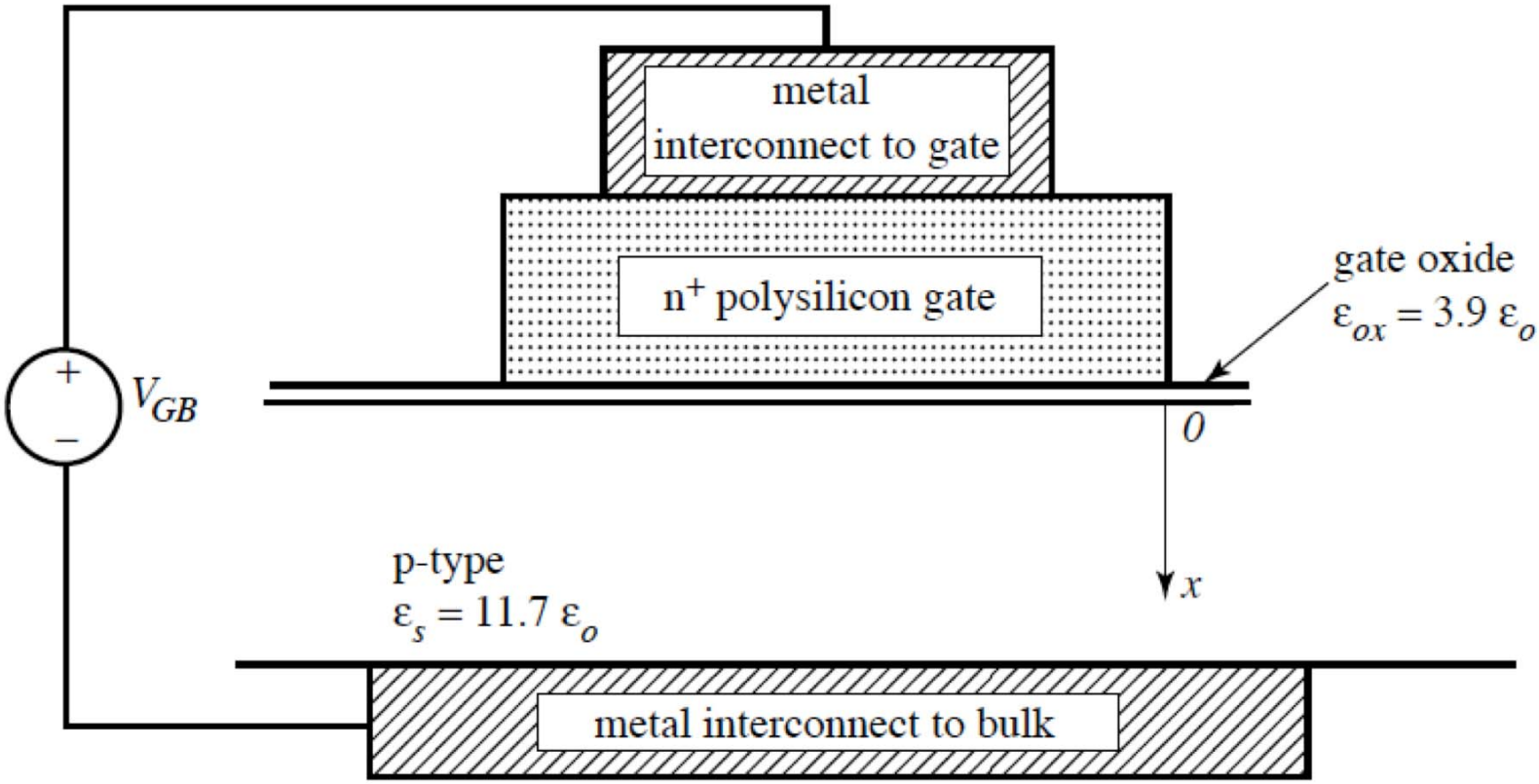
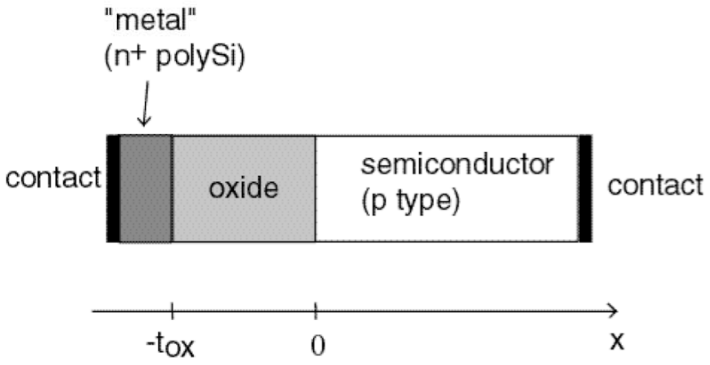


FIG 2.2 MOS structure demonstrating (a) accumulation, (b) depletion, and (c) inversion

MOS Structure (a more in depth look)



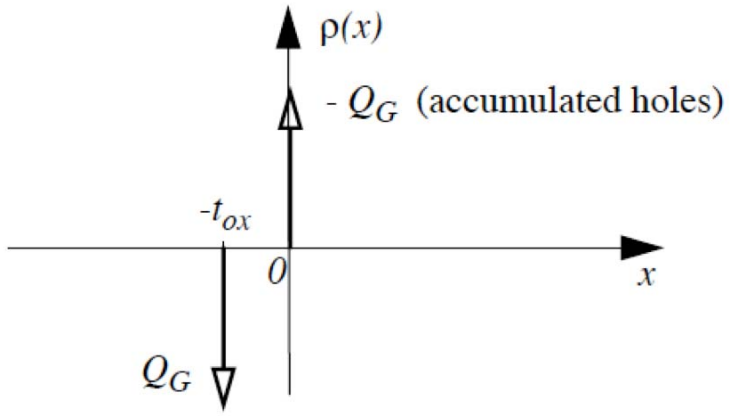


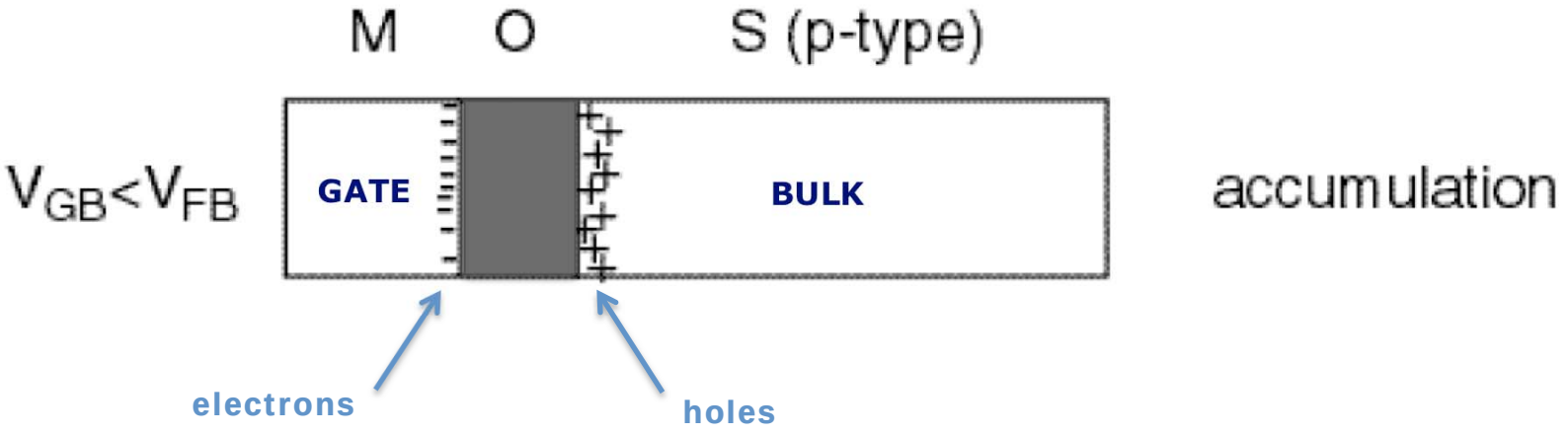
$$V_{FB} \equiv -\phi_B$$

MOS capacitor in accumulation

- $V_{GB} < V_{FB}$

charge density

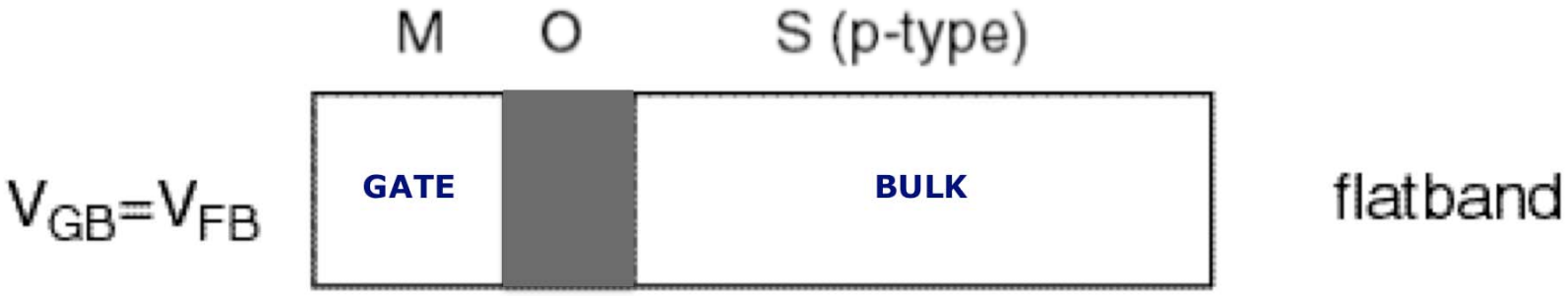




$$V_{FB} \equiv -\phi_B$$

MOS capacitor in flatband

- $V_{GB} = V_{FB}$



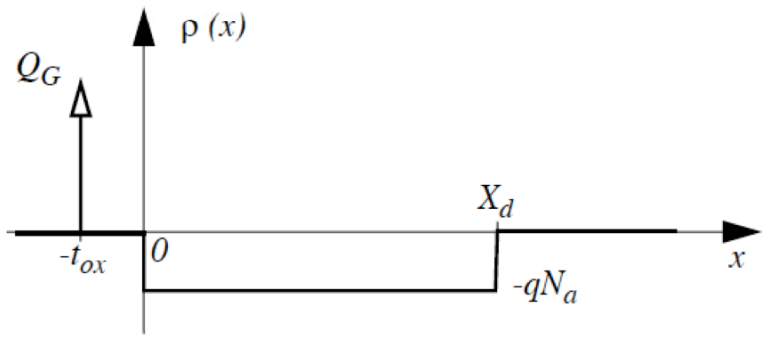
$$V_{FB} \equiv -\phi_B$$

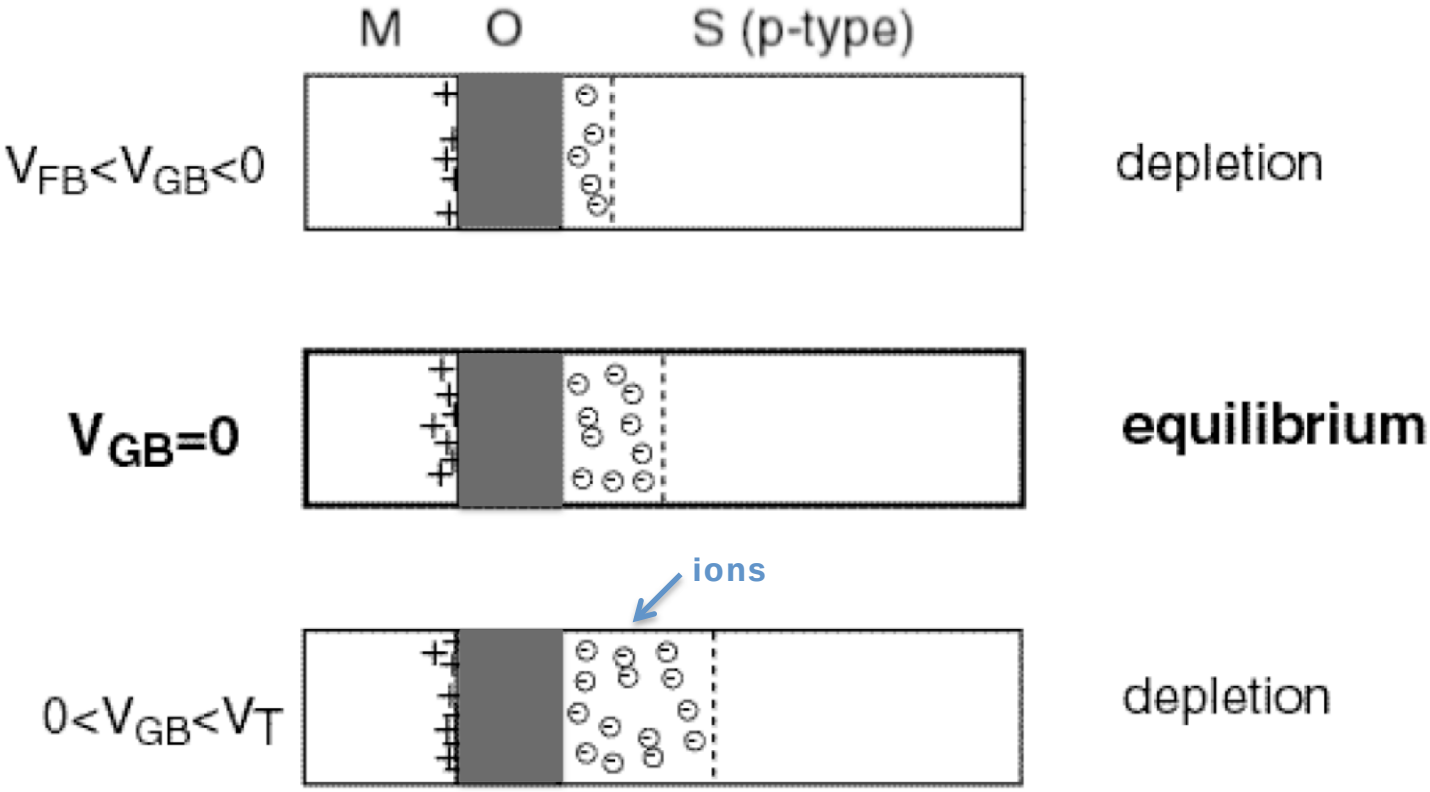
MOS capacitor in depletion

Note:
thermal equilibrium
falls in this range of
applied bias

- $V_{GB} > V_{FB}$

charge
density

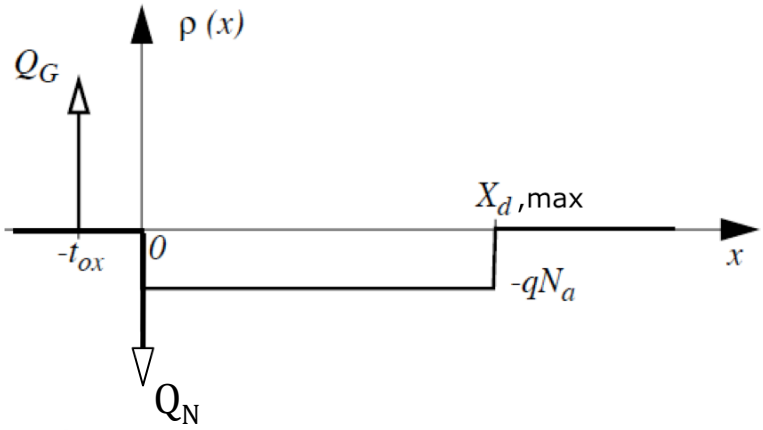


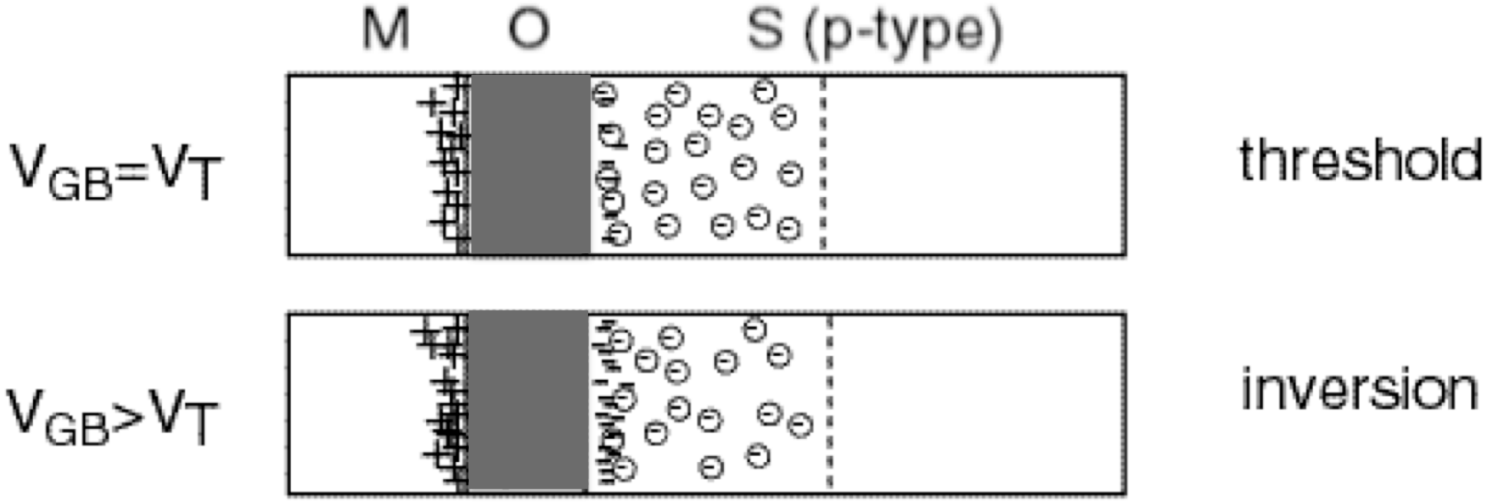


MOS capacitor in inversion

- $V_{GB} > V_T$

charge density

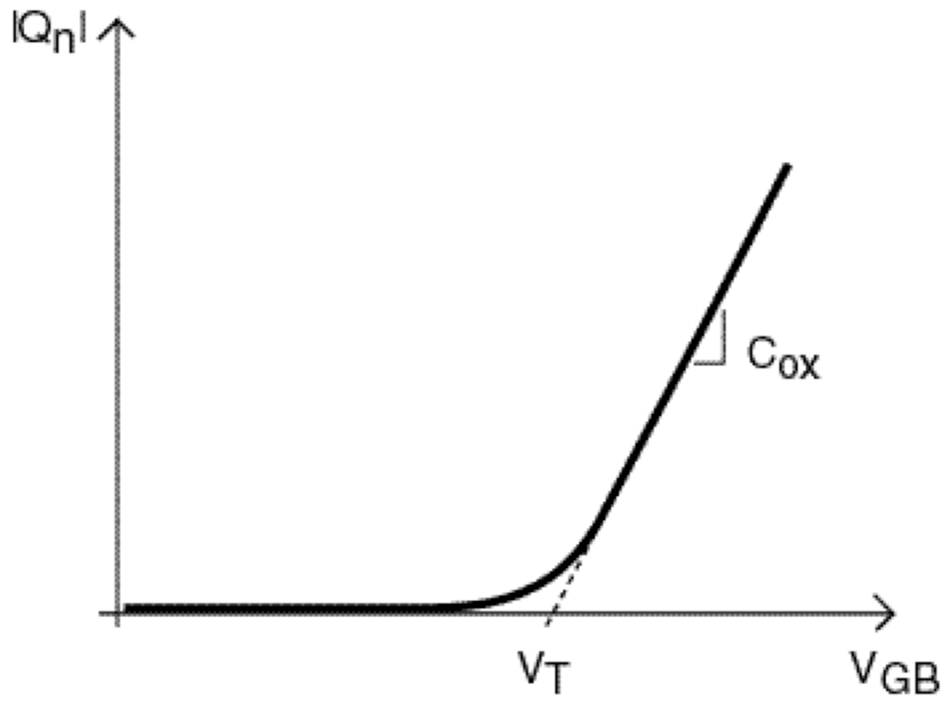




- Xd does not increase much beyond threshold
- All extra voltage beyond V_T used to increase inversion charge Q_N

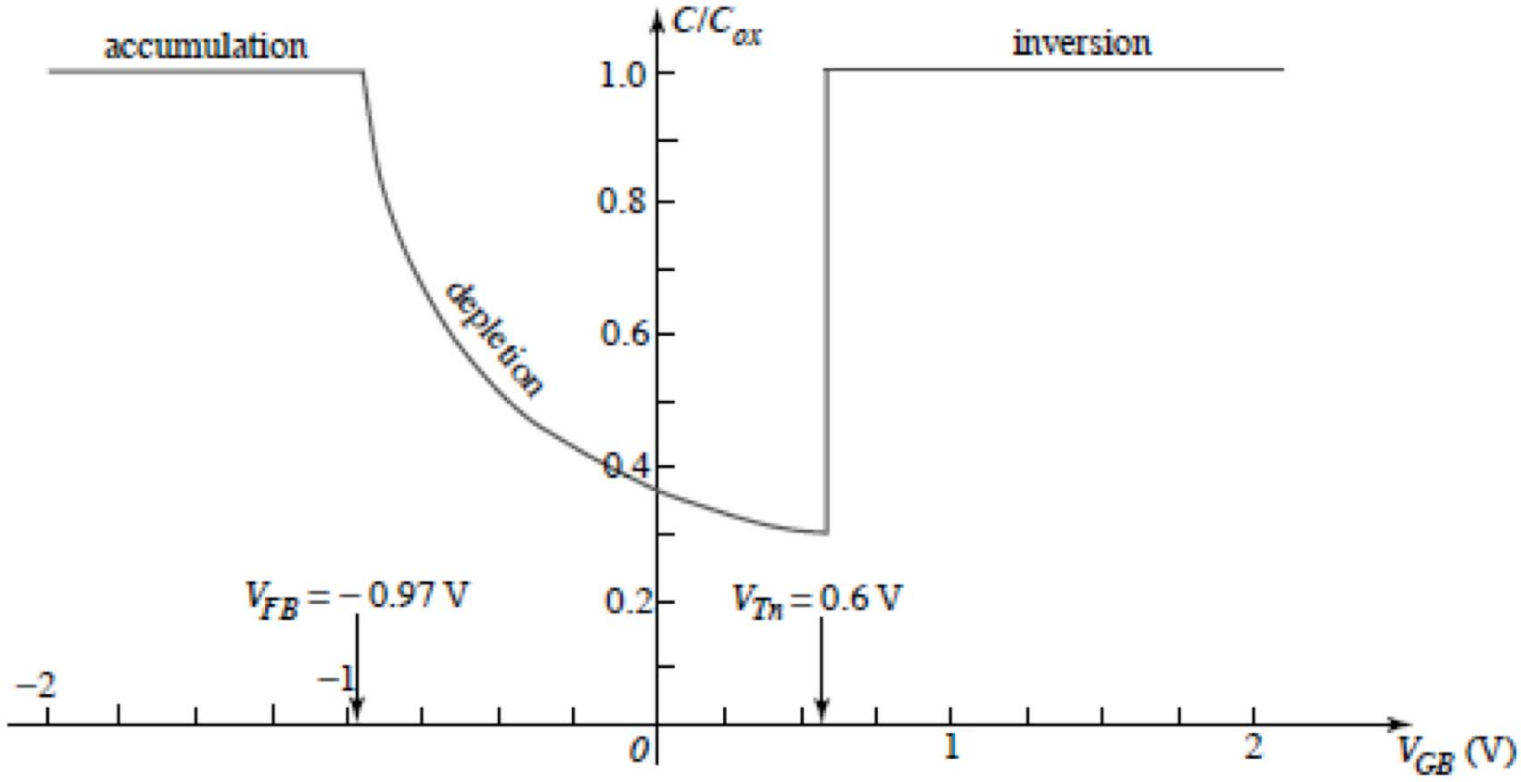
MOS Capacitor in inversion

- Existence of Q_N and control over Q_N by V_{GB} is the key to MOS electronics



$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{VGB}$$

MOS Capacitance

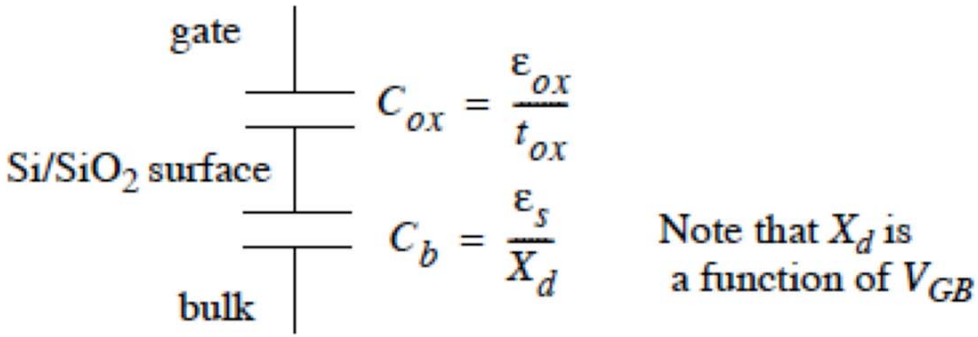


$$C(V_{GB}) \equiv C_{GB}$$

Physical interpretation of MOS capacitance

- *Accumulation*: parallel plate capacitor --> $C = C_{ox}$

- *Depletion*: increment in gate charge is mirrored at bottom of depletion region, so capacitance model is C_{ox} in series with the depletion region capacitance C_b



Note that X_d is a function of V_{GB}

$$C = C_{ox} || C_b$$

- *Inversion*: bulk charge is no longer changing with V_{GB} --> an increment in gate charge is mirrored in the inversion layer under the gate.

  The capacitance is therefore the same as in accumulation --> $C = C_{ox}$

Width of the depletion region

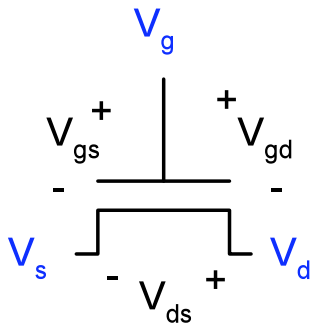
- VFB ≤ VGB ≤ VT

$$X_d(V_{GB}) = \sqrt{\frac{2\varepsilon_S(\phi_B - V_{GB})}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = X_{do}\sqrt{1 - \frac{V_{GB}}{\phi_B}}$$

$$X_{do} \equiv \sqrt{\frac{2\varepsilon_S\phi_B}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)}$$

equilibrium

nMOS Transistor Terminal Voltages

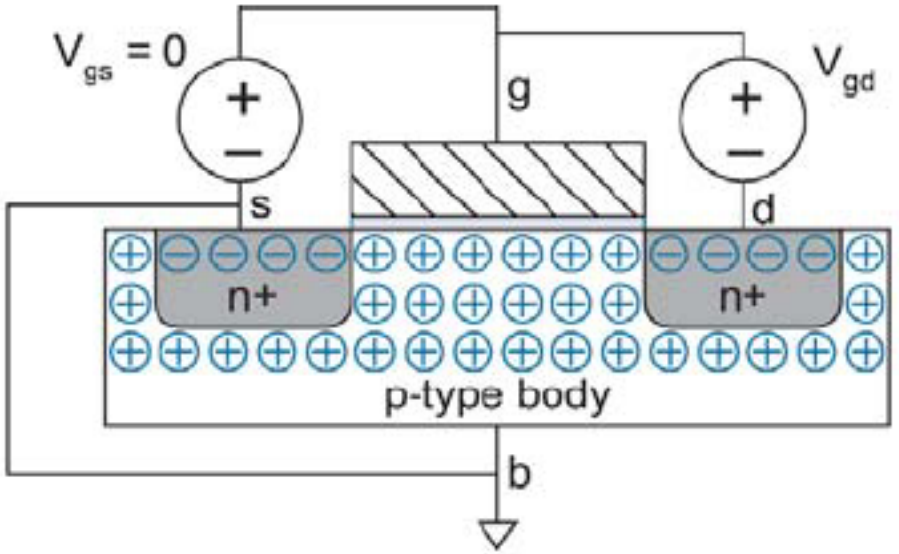


- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - Cutoff
  - Linear
  - Saturation

nMOS in cutoff operation mode (1/2)

- No channel
- $I_{ds} = 0$

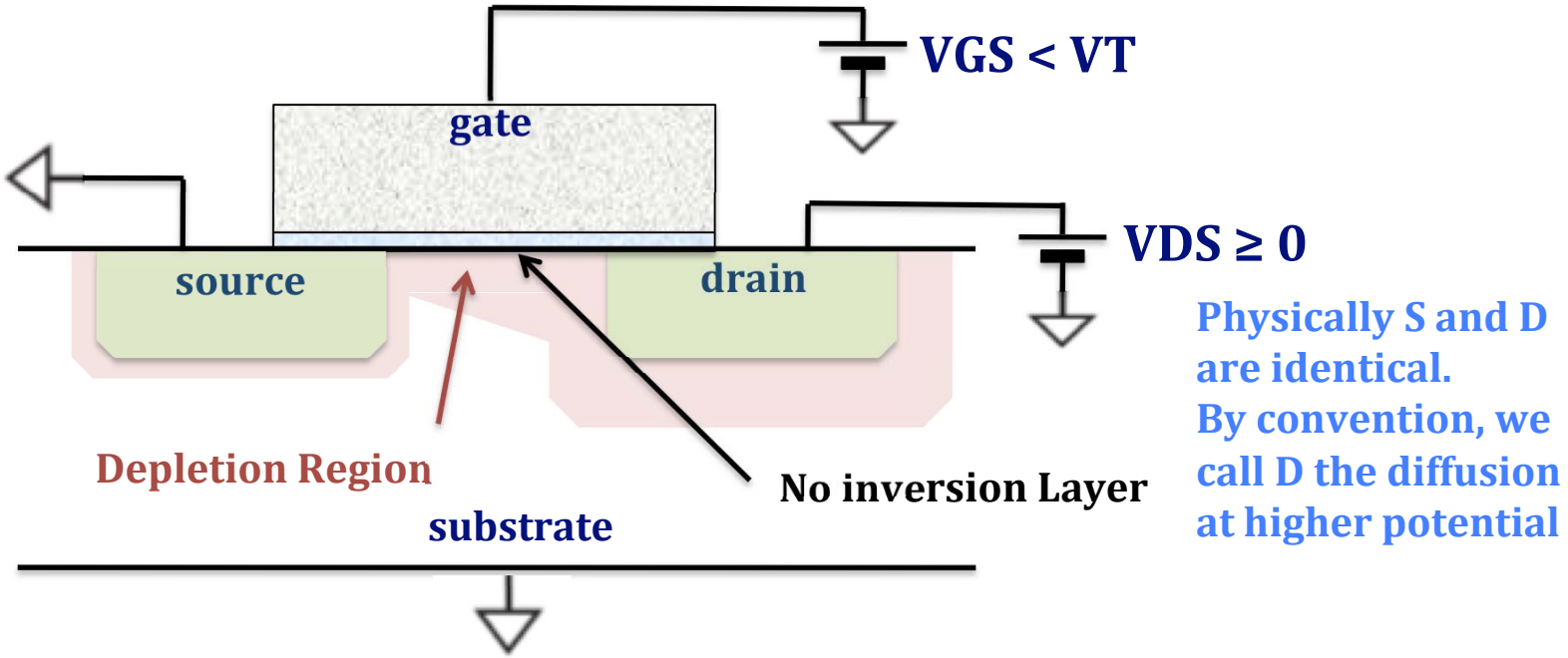
Simplifying assumption VB=VS



(a)

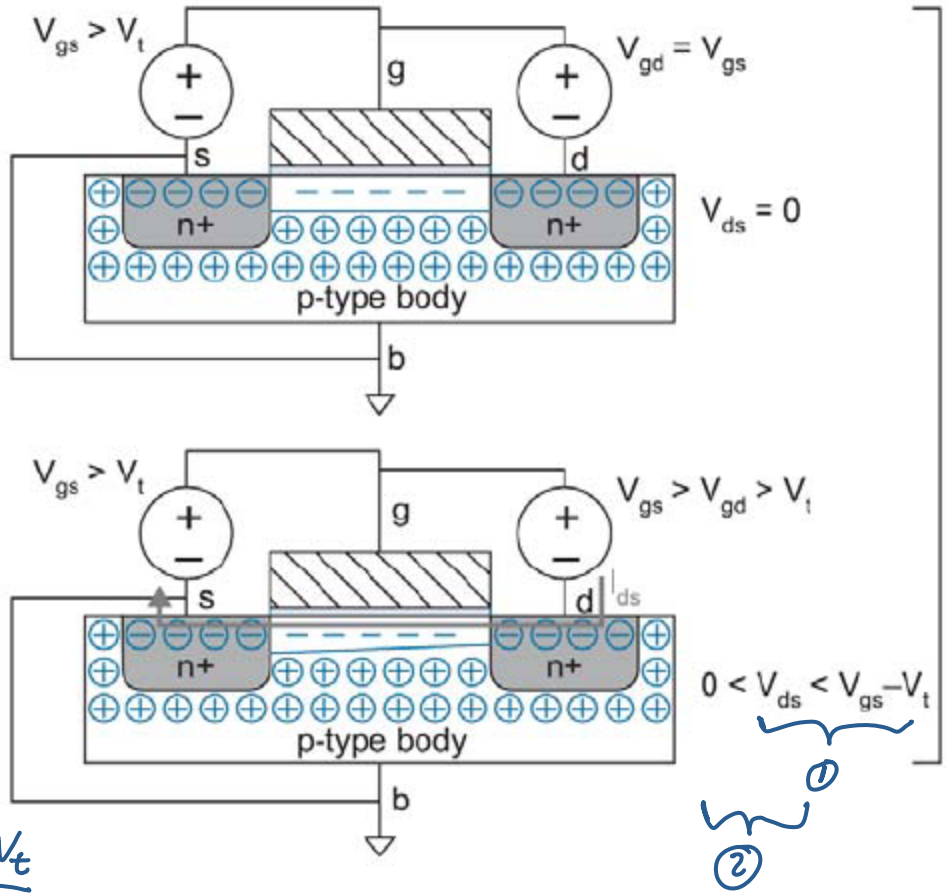
nMOS in cut-off mode (2/2)

- $V_{GS} < V_T$
- Q_N= inversion charge =0
- V_{DS} drops across the depletion region
- I_{DS}=0



nMOS in linear operation mode (1/3)

- Channel forms
- Current flows from D to S
  - e^- from S to D
- I_{ds} increases with V_{ds} (b)
- Similar to linear resistor



① $V_{ds} < V_{gs} - V_t$

$V_{ds} - V_{gs} < -V_t$

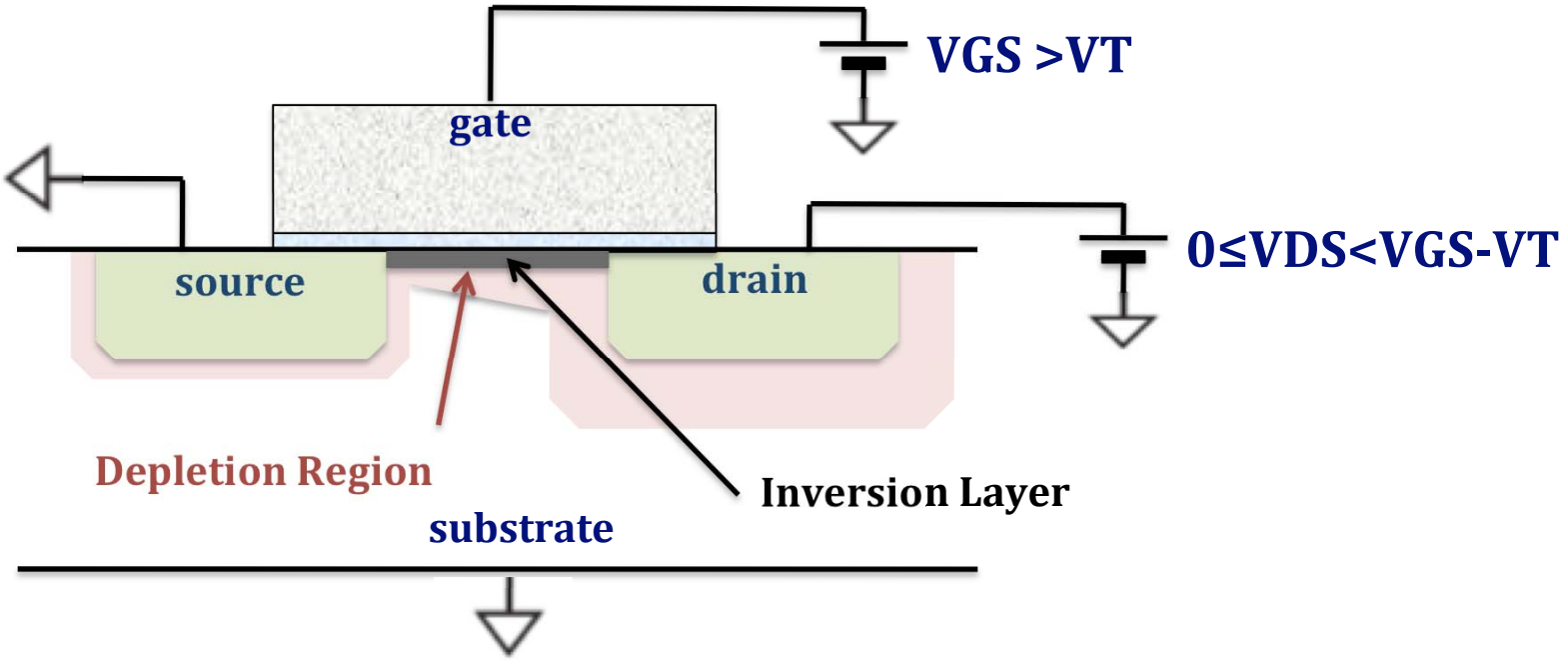
$V_d - V_s - V_g + V_s < -V_t$

$V_{dg} < -V_t \leftrightarrow -V_{gd} < -V_t \leftrightarrow V_{gd} > V_t$

② $V_{ds} > 0 \leftrightarrow V_{gs} - V_{gd} > 0 \leftrightarrow V_{gs} > V_{gd}$

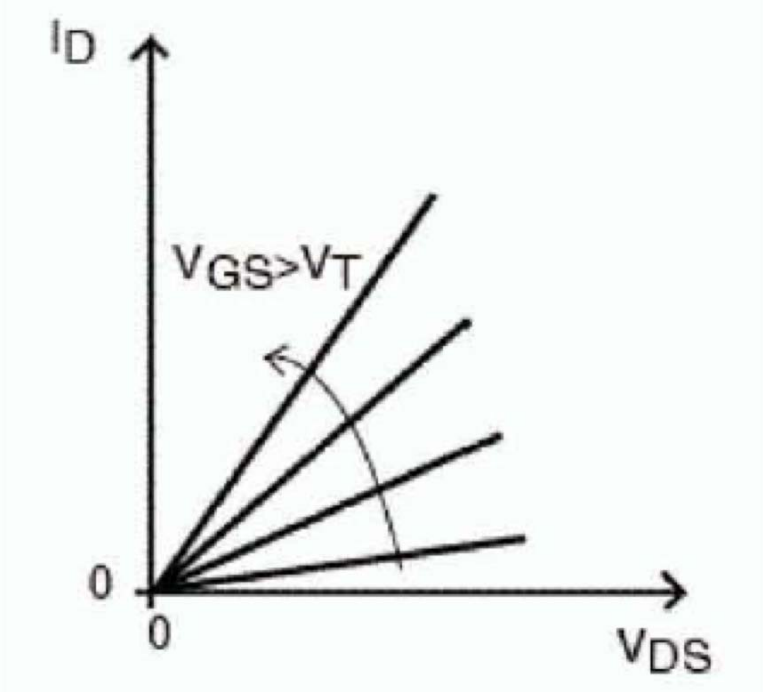
nMOS in linear (=triode) mode (2/3)

- $V_{GS} > V_T$ and $V_{GD} > V_T$ ($V_{GD} > V_T \Leftrightarrow V_{DS} < V_{GS}-V_T$)
- $V_{GS}\uparrow \Rightarrow Q_N\uparrow \Rightarrow I_{DS}\uparrow$
- $V_{DS}\uparrow \Rightarrow E_{lateral}\uparrow \Rightarrow I_{DS}\uparrow$



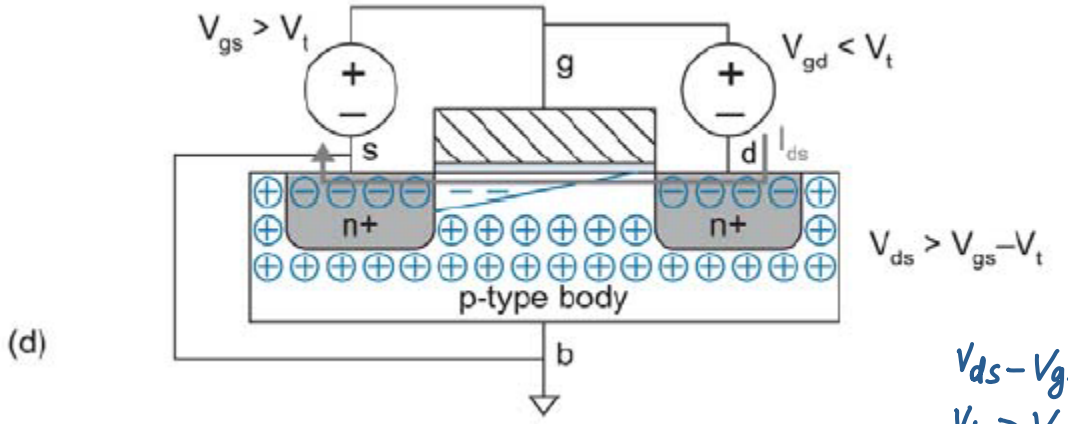
nMOS in linear (=triode) mode (3/3)

- V_{GS} ↑ (more electrons in the inversion layer)
- V_{DS} ↑ (higher lateral electric field ⇔ electrons in the channel move faster)



nMOS in Saturation operation mode (1/6)

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source



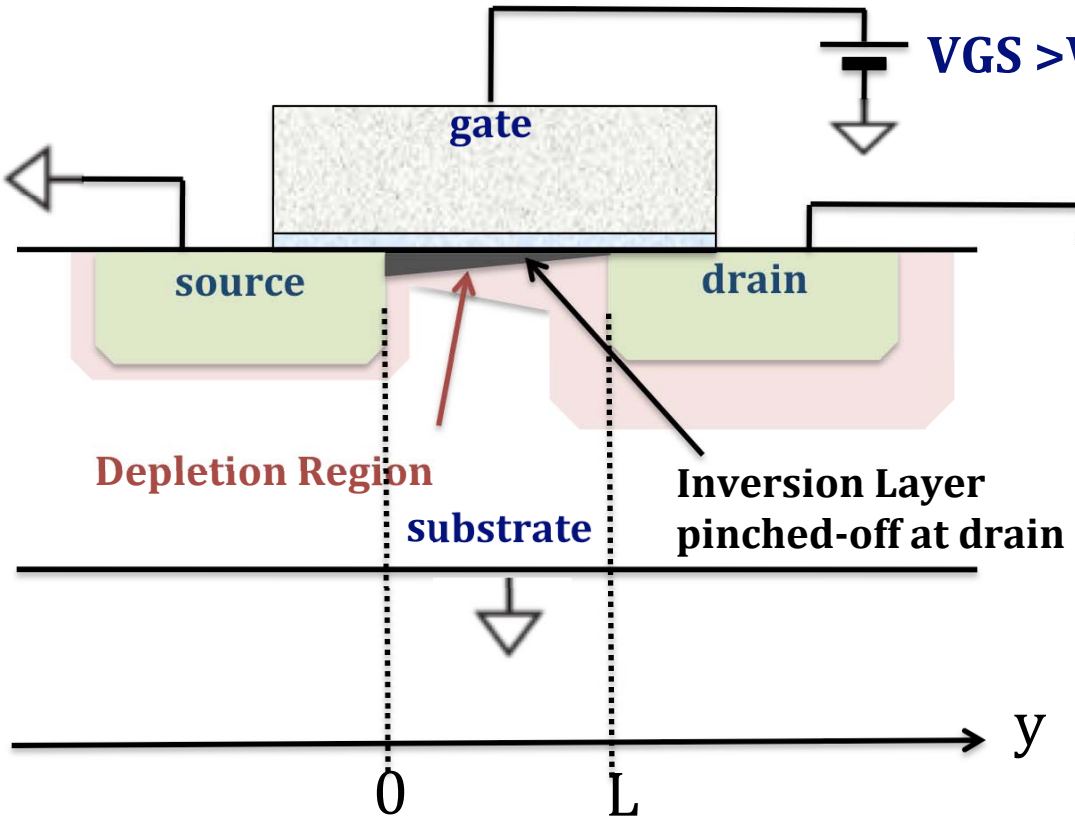
$V_{ds} - V_{gs} > -V_t$

$V_t > V_{gs} - V_{ds}$

$V_t > V_{gd} \rightarrow V_{gd} < V_t$

nMOS in saturation mode (2/6)

- $V_{GS} > V_T$ and $V_{GD} < V_T$ ($V_{GD} < V_T \Leftrightarrow V_{DS} > V_{GS}-V_T$)



The inversion layer thin down from S to D

nMOS in saturation mode (3/6)

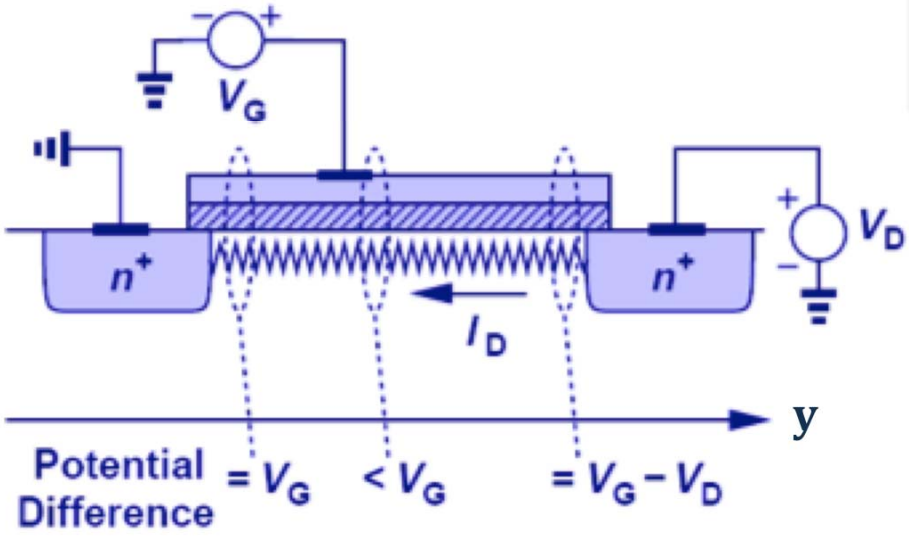
- When $V_{DS} > V_{GS}-V_T$ ($V_{GD} < V_T$) ⇒ $Q_N(y=L)=0$
- Initial thought: lack of a channel at the drain means that I_D must drop to zero. **WRONG … !!**
- Drain terminal loses control over channel ⇒ Drain current saturates and remain approximately constant at the value given by $V_{DS,\,SAT}$ ($=V_{GS}-V_T$)

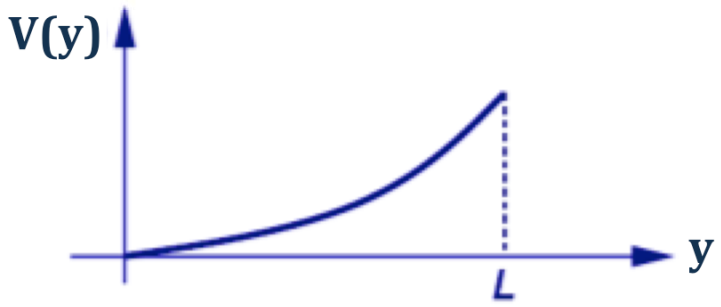
- I_D becomes independent of V_{DS}: $I_D=I_{D,SAT}$

nMOS in saturation mode (4/6)

$$Q_N(y) = C_{ox} \cdot [V_{GC}(y) - V_T]$$

$$V_{GC}(y) = V_G - V(y)$$





Gate-Channel potential difference $V_{GC}(y)$

nMOS in saturation mode (5/6)

- Current flux is the same across any section y along the channel. Thus as y increases down the channel
  $V(y)\uparrow \Rightarrow Q_N(y)\downarrow \Rightarrow E(y)\uparrow$ (*fewer carriers moving faster*)
- General expression of channel current (*current= charge/time*) :

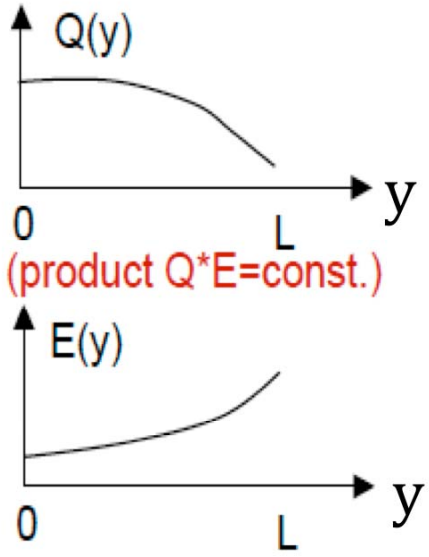
$$I_y(y) = I_D(y) = Q_N(y) \cdot W \cdot v_y(y)$$

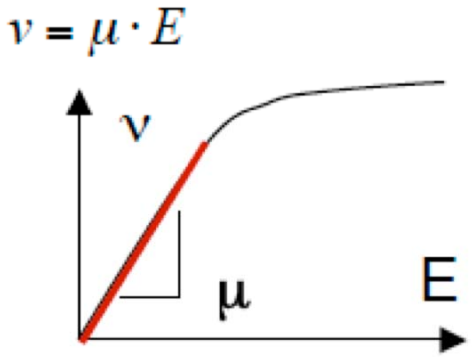
$$v_y(y) = \mu \cdot E_y(y)$$

charge per area

carriers velocity

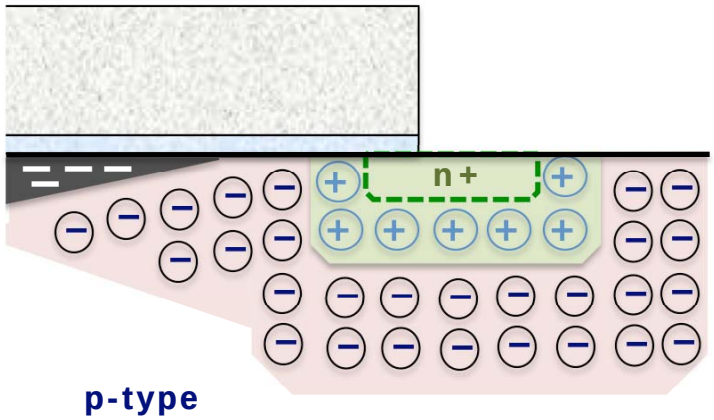
carriers mobility

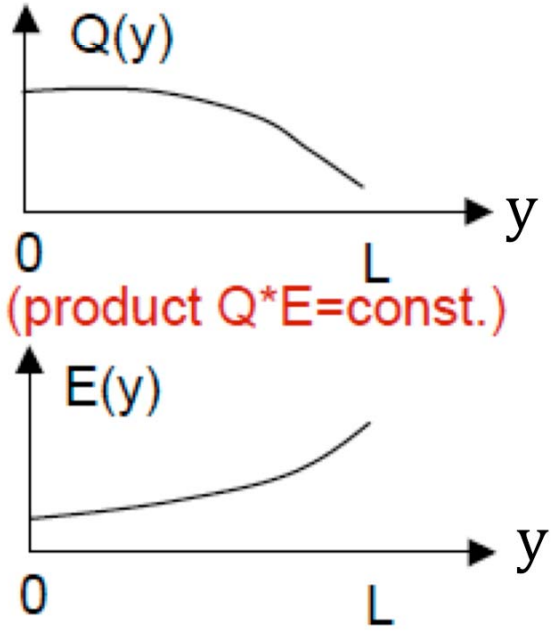




nMOS in saturation mode (6/6)

- Increase in E_y ($E_y\uparrow \Leftrightarrow V_{DS}\uparrow$) is compensated by decrease in Q_N
- When Q_N=0 at drain then I_D saturates





After channel charge goes to 0, there is a high lateral field that 'sweeps' the carriers to the drain*, and drops the extra voltage (this is a depletion region of the drain junction)

* It is important to remember what a reverse biased PN junction does to minority carriers.
Electrons (in the p-type material) get swept back into the n-region

pMOS Transistor

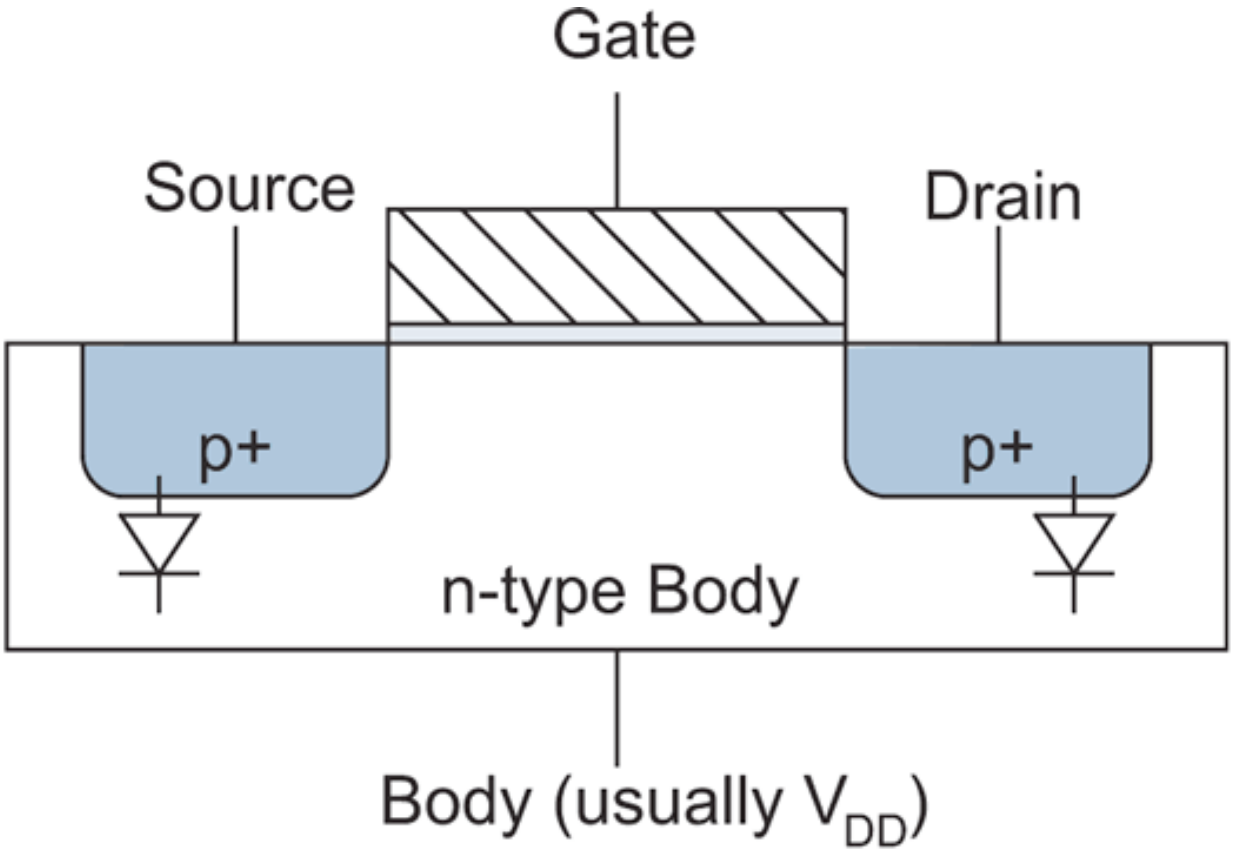
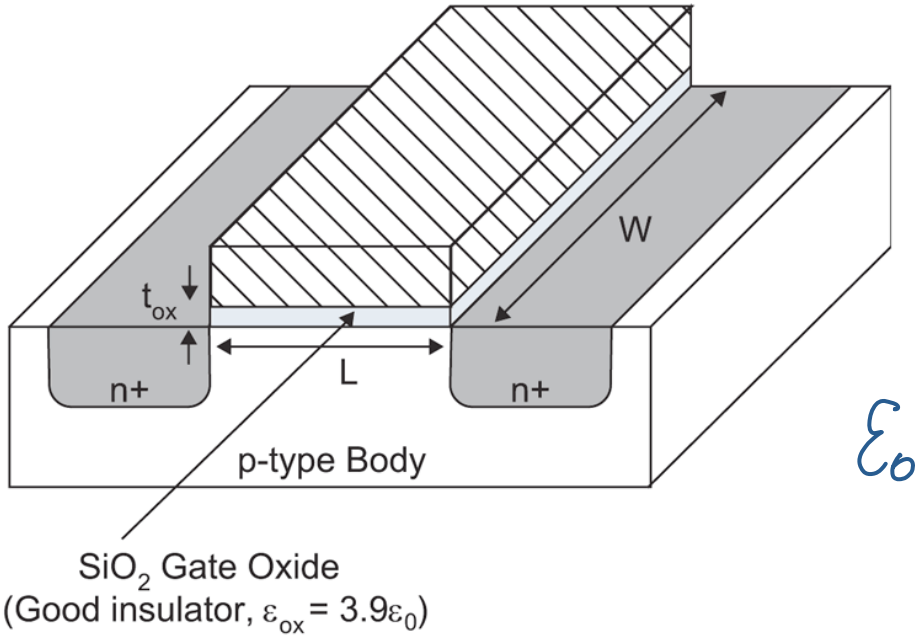


FIG 2.4 pMOS transistor

I-V Characteristics (nMOS)

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?



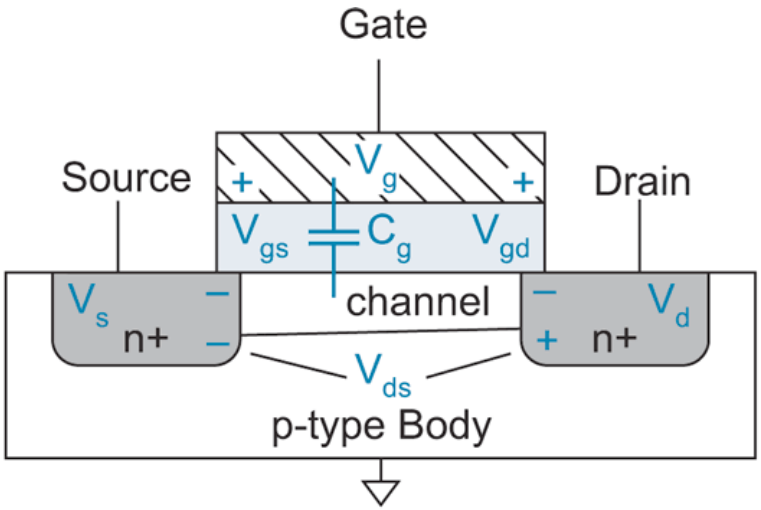
$\varepsilon_0 = 8.85 \times 10^{-12}$ F/m

FIG 2.6 Transistor dimensions

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion:
  - Gate – oxide – channel
- $Q_{channel} = C*V$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = c_{ox}WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

$$c_{ox} = \varepsilon_{ox} / t_{ox}$$



Average gate to channel potential:

$$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$$

FIG 2.5 Average gate to channel voltage

$$V_{gc} = \frac{V_{gs} + V_{gd}}{2} = \frac{V_{gs} + V_{gs} - V_{ds}}{2} = V_{gs} - \frac{V_{ds}}{2}$$

Carrier velocity

- Charge is carried by e−
- Carrier velocity ν proportional to lateral E-field between source and drain
- $\nu = \mu E$ (μ called mobility)
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / \nu$

nMOS Linear (a.k.a. triode) I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

Many textbooks define:

$K' = \mu C_{ox}$ ← technology dependent parameters

$$I_{ds} = \frac{Q_{\text{channel}}}{t} =$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

but be careful !!!

MOSIS:

$K' = \mu \frac{C_{ox}}{2}$

technology and geometric parameters

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Triode I-V characteristic

$$I_D = Q_N(y) \cdot W \cdot v_y(y)$$

$$v_y(y) = \mu \cdot E_y(y)$$

$$E_y(y) = \frac{dV(y)}{dy}$$

$$Q_N(y) = C_{ox}[V_{GS} - V(y) - V_T]$$

$$I_D dy = \mu \cdot Cox \cdot W \cdot [V_{GS} - V(y) - V_T] \cdot dV$$

$$I_D \int_0^L dy = \mu \cdot Cox \cdot W \cdot \int_0^{VDS} [V_{GS} - V(y) - V_T] \cdot dV$$

$$I_D = \mu \cdot Cox \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

with $\beta = \mu C_{ox} \frac{W}{L}$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

nMOS I-V Summary

- first order (Shockley model) transistor models (ideal models)

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ & \text{(and } V_{gs} > V_t\text{)} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \\ & \text{(and } V_{gs} > V_t\text{)} \end{cases}$$

I-V characteristics of nMOS Transistor

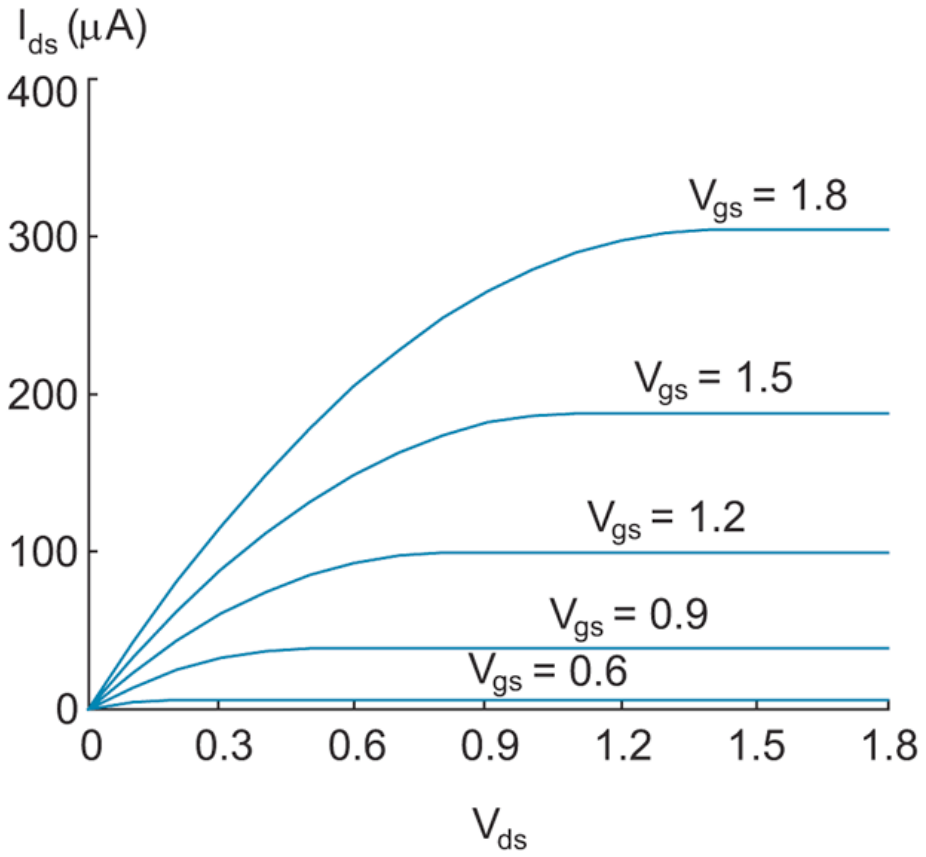
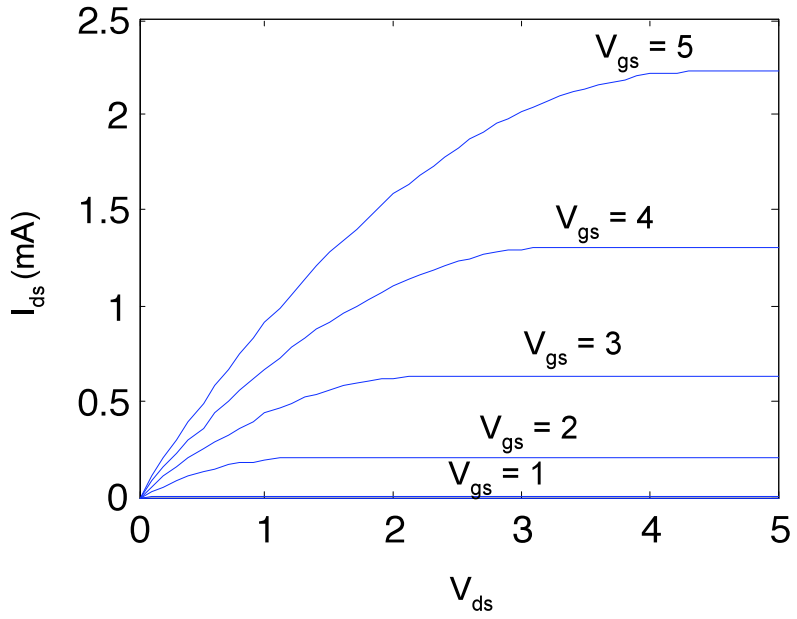


FIG 2.7 I-V characteristics of ideal nMOS transistor

Example

- 0.6 μm process from AMI Semiconductor
  - t_{ox} = 100 Å
  - μ = 350 $cm^2/(V*s)$
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85\cdot 10^{-14}}{100\cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\mu A/V^2$$

pMOS I-V Characteritics

- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V*s$ in AMI 0.6 mm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

pMOS I-V Summary

- first order (ideal) transistor models (a.k.a. Shockley model)

$$I_{ds} = \begin{cases} 0 & V_{gs} > V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} > V_{dsat} \quad \text{linear} \\ & (\text{and } V_{gs} < V_t) \\ \dfrac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} < V_{dsat} \quad \text{saturation} \\ & (\text{and } V_{gs} < V_t) \end{cases}$$

I-V characteristics of pMOS Transistor

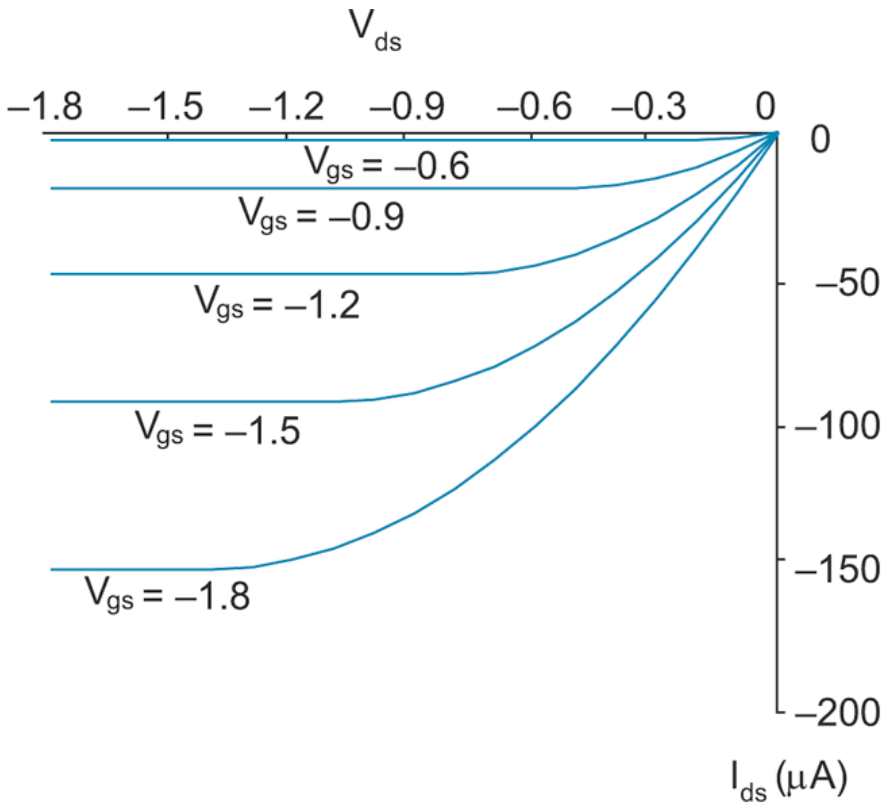
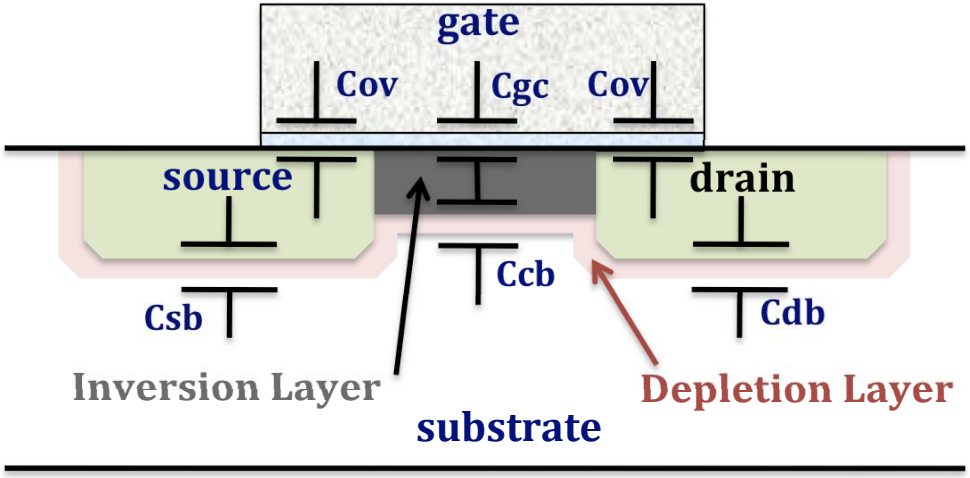


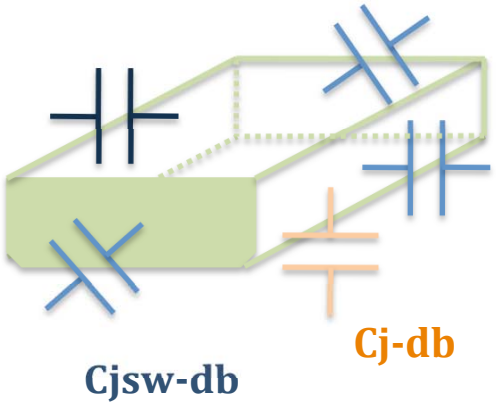
FIG 2.8 I-V characteristics of ideal pMOS transistor

MOS Transistor's Capacitances

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation (intrinsic capacitance)
- Source and drain have capacitance to body (parasitic capacitance)
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

MOS transistor's Capacitances





Cgc modeled through Cgs and Cgd

Ccb mododel through Cgb

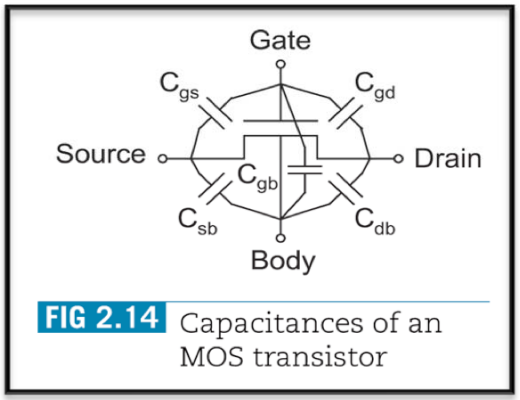


FIG 2.14 Capacitances of an MOS transistor

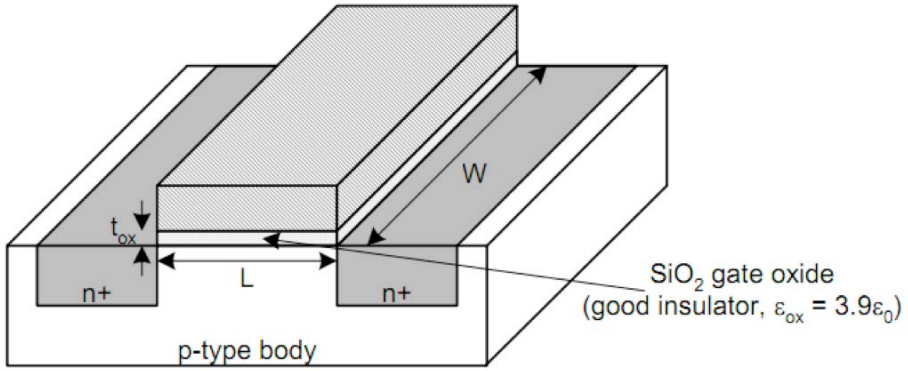
$Csb = AS \times Cj\text{-}sb + PS \times Cjsw\text{-}sb$

$Cdb = AD \times Cj\text{-}db + PD \times Cjsw\text{-}db$

bottom junction cap. per area

Side wall junction cap. per perimeter

Gate Capacitance



- When the transistor is off, the channel is not inverted
  $C_g = C_{gb} = C_{ox}WL \,||\, \varepsilon_{si}WL/X_d < \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$
- Let's call $C_{ox}WL = C_0$
- When the transistor is on, the channel extends from the source to the drain (if the transistor is unsaturated, or to the pinch off point otherwise)
  $C_g = C_{gb} + C_{gs} + C_{gd}$

Gate Capacitance

Table 2.1 Approximation of intrinsic MOS gate capacitance

Parameter	Cutoff	Linear	Saturation
C_{gb}	$\approx C_0$	0	0
C_{gs}	0	$C_0/2$	$2/3\ C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	$\approx C_0$	C_0	$2/3\ C_0$

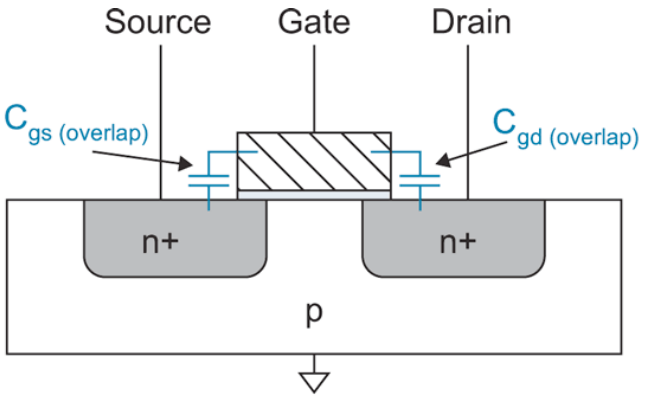


FIG 2.10 Overlap capacitance

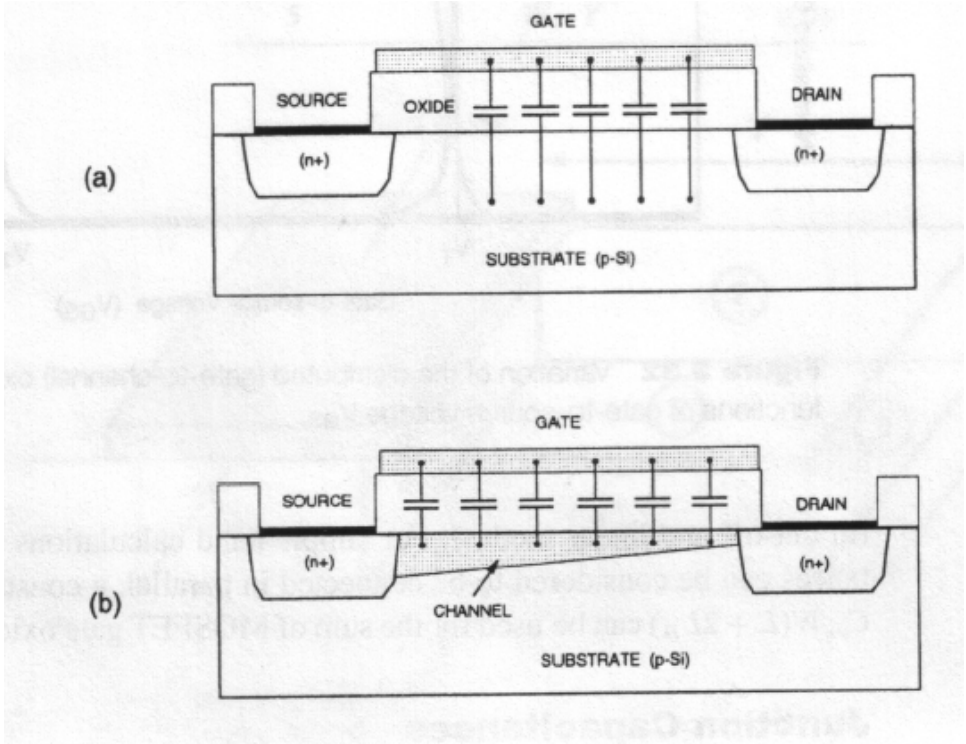
In reality the gate overlaps source and drain. Thus, the gate capacitance should include not only the intrinsic capacitance but also parasitic overlap capacitances:

$C_{gs}(\text{overlap}) = C_{ox}\ W\ L_{ov}$

$C_{gs}(\text{overlap}) = C_{ox}\ W\ L_{ov}$

Detailed Gate Capacitance

Capacitance	Cutoff	Linear	Saturation
C_{gb} (total)	$\approx C_0$	0	0
C_{gd} (total)	$C_{ox}WL_{ov}$	$C_0/2 + C_{ox}WL_{ov}$	$C_{ox}WL_{ov}$
C_{gs} (total)	$C_{ox}WL_{ov}$	$C_0/2 + C_{ox}WL_{ov}$	$2/3\ C_0 + C_{ox}WL_{ov}$



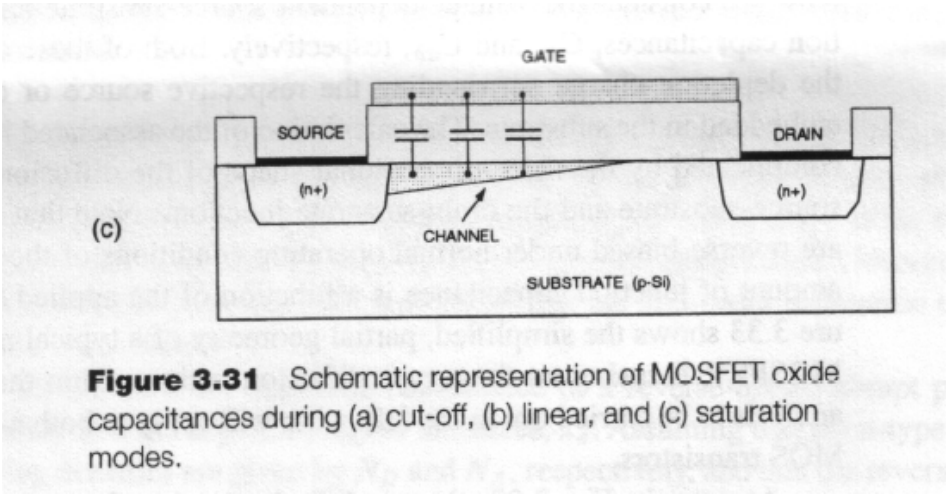


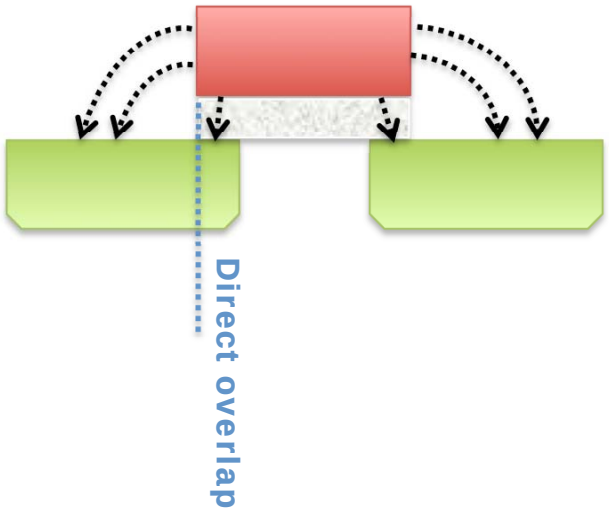
Figure 3.31 Schematic representation of MOSFET oxide capacitances during (a) cut-off, (b) linear, and (c) saturation modes.

Source: M-S Kang, Y. Leblebici, *CMOS Digital ICs*, 3/e, 2003, McGraw-Hill

Overlap Capacitance

- It has two components
  - Direct overlap ≈ $C_{ox}WL_{ov}$
  - Additional component due to fringing fields

$$Cov = Cov' \cdot W$$



$$C_{ov-GS} = CGSO \cdot W$$
$$C_{ov-GD} = CGDO \cdot W$$

Junction Capacitance

- C_{sb}, C_{db}
- Undesired capacitance (parasitic)
- Due to the reverse biased p-n junctions between source and body and drain and body
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_g for contacted diffusion
  - ½ C_g for uncontacted
  - Varies with process

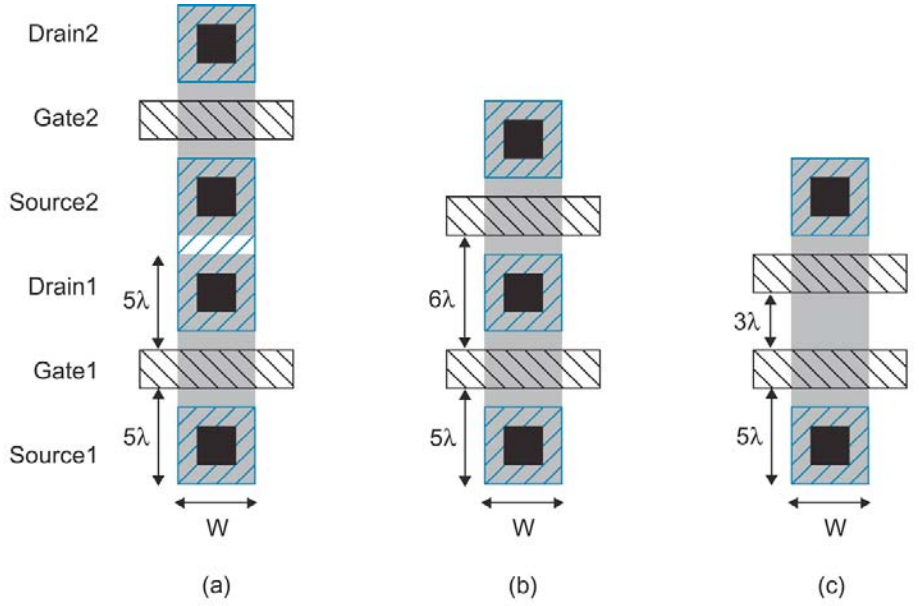


FIG 2.9 Diffusion region geometries

(a) Isolated contacted diffusion

(b) Shared contacted diffusion

(c) Merged uncontacted diffusion

Junction Capacitance

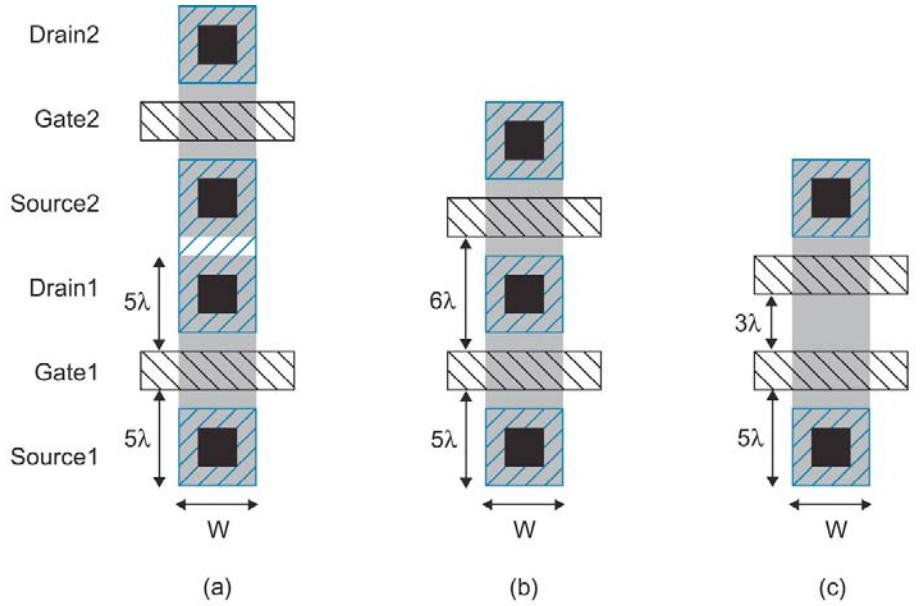
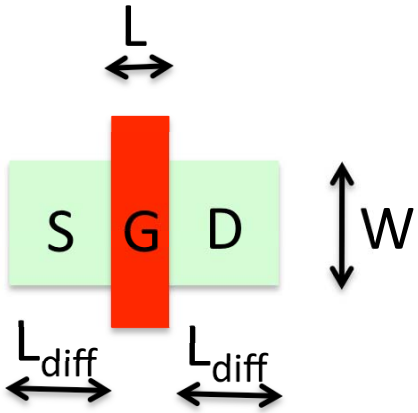


FIG 2.9 Diffusion region geometries

	AD1/AD2	PS1/PD2	AD1/AS2	PD1/PS2
(a) Isolated contacted diffusion	Wx5	2xW+10	Wx5	2xW+10
(b) Shared contacted diffusion	Wx5	2xW+10	Wx3	W+6
(c) Merged uncontacted diffusion	Wx5	2xW+10	Wx1.5	W+3

Junction Capacitance



$$AS = W \cdot L_{diff}$$

$$PS = W + 2L_{diff}$$

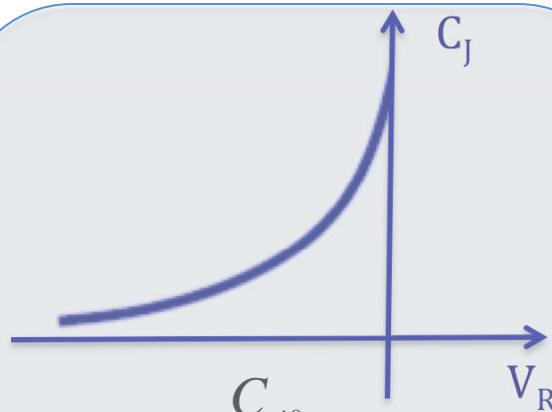
$$AD = W \cdot L_{diff}$$

$$PD = W + 2L_{diff}$$

For long channel transistors the side of the perimeter abutted to the gate is shielded by the electrons in the channel

$$Cjdb = \frac{AD \cdot CJ}{\left(1 + \frac{VDB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VDB}{PBSW}\right)^{MJSW}}$$

$$Cjsb = \frac{AS \cdot CJ}{\left(1 + \frac{VSB}{PB}\right)^{MJ}} + \frac{PS \cdot CJSW}{\left(1 + \frac{VSB}{PBSW}\right)^{MJSW}}$$



$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\phi_B}}}$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{\phi_B}}$$

Lumped representation of the MOSFET capacitances

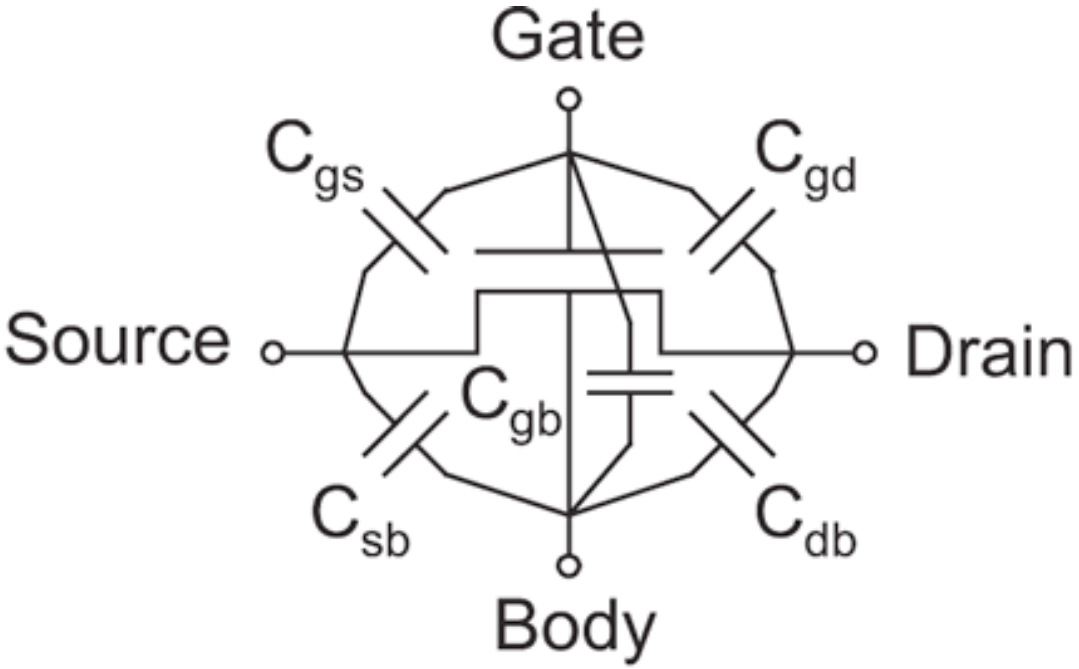


FIG 2.14 Capacitances of an MOS transistor

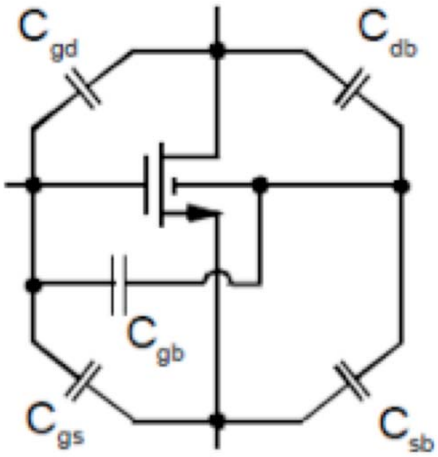
MOS transistor's caps Summary

extrinsic cap. intrinsic cap.

	Subthreshold	Triode	Saturation
C_{gs}	C_{ov}	$\frac{1}{2}WLC_{ox}+C_{ov}$	$\frac{2}{3}WLC_{ox}+C_{ov}$
C_{gd}	C_{ov}	$\frac{1}{2}WLC_{ox}+C_{ov}$	C_{ov}
C_{gb}	$\left(\frac{1}{C_{CB}}+\frac{1}{WLC_{ox}}\right)^{-1}$	0	0
C_{sb}	C_{jsb}	$C_{jsb}+\frac{1}{2}C_{CB}$	$C_{jsb}+\frac{2}{3}C_{CB}$
C_{db}	C_{jdb}	$C_{jdb}+\frac{1}{2}C_{CB}$	C_{jdb}

$$C_{CB}=\frac{\varepsilon_{si}}{X_d}\cdot WL$$

Xd is the width of the depletion region at the silicon interface



Non-ideal I-V effects

- The saturation current increases less than quadratically with increasing V_{gs}
  - Velocity saturation
  - Mobility degradation
- Channel length modulation
- Body Effect
- Leakage currents
  - Sub-threshold conduction
  - Junction leakage
  - Tunneling
- Temperature dependence and supply dependence (environmental dependence)
- Geometry Dependence (process dependence)

Pass Transistors

- nMOS pass transistors pull no higher than V_{DD}-V_{tn}
  - Called a degraded “1”
  - Approach degraded value slowly (low I_{ds})
- pMOS pass transistors pull no lower than $|V_{tp}|$
  - Called a degraded “0”
  - Approach degraded value slowly (low I_{ds})

Pass transistor Circuits

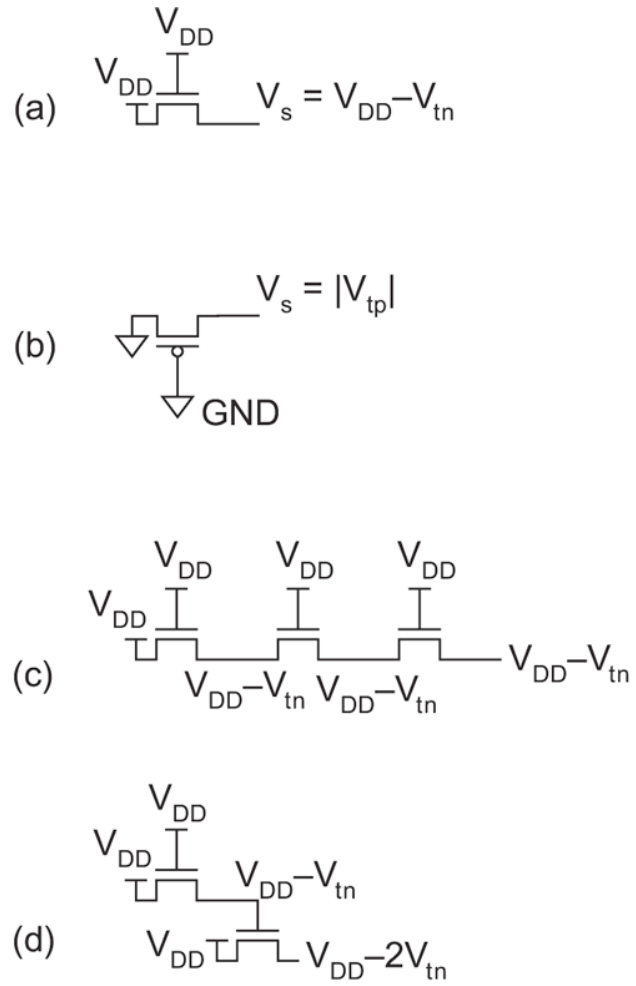
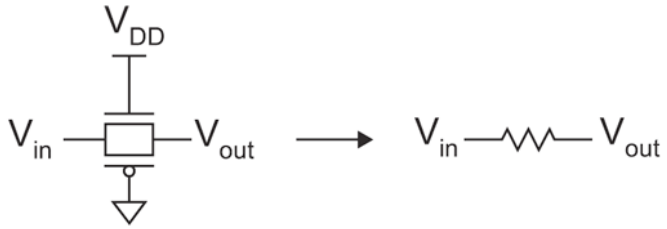


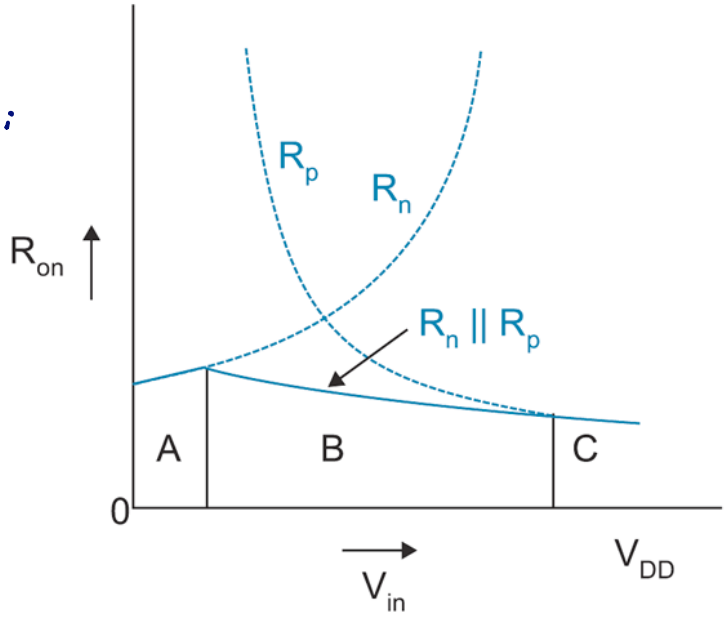
FIG 2.31 Pass transistor threshold drops

Transmission gate ON resistance



At a given operating point:

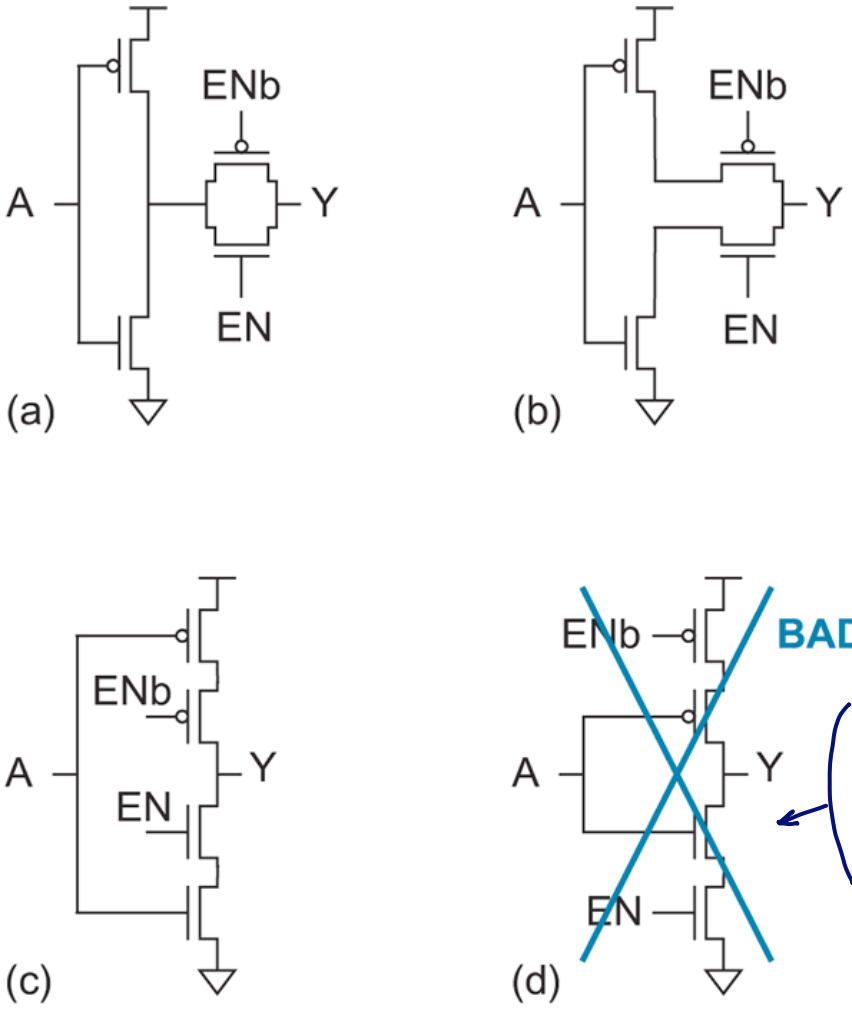
$$R = \left(\frac{\partial I_{ds}}{\partial V_{ds}}\right)^{-1}$$



Input voltage Vin is swept from GND to VDD

FIG 2.32 Resistance of a transmission gate as a function of input voltage

Tri-state Inverter



If the output is tri-stated but A toggles, charge from the internal nodes (= caps) may disturb the floating output node

FIG 2.33 Tristate inverter

Effective resistance of a transistor

- First-order transistor models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for hand analysis
- Simplification: treat transistor as resistor
  - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
  - $I_{ds} = V_{ds}/R$
  - R averaged across switching range of digital gate
- Too inaccurate to predict current at any given time
  - But good enough to predict RC delay (propagation delay of a logic gate)

RC Values

- Capacitance
  - $C = C_g = C_s = C_d = 2$ fF/μm of gate width
  - Values similar across many processes
- Resistance
  - $R \approx 6$ KΩ*μm in 0.6um process
  - Improves with shorter channel lengths
- Unit transistors
  - May refer to minimum contacted device (4/2 λ)
  - or maybe 1 μm wide device
  - Doesn't matter as long as you are consistent

RC Delay Models

- Use equivalent circuits for MOS transistors
  - ideal switch + capacitance and ON resistance
  - unit nMOS has resistance R, capacitance C
  - unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width

Switch level RC models

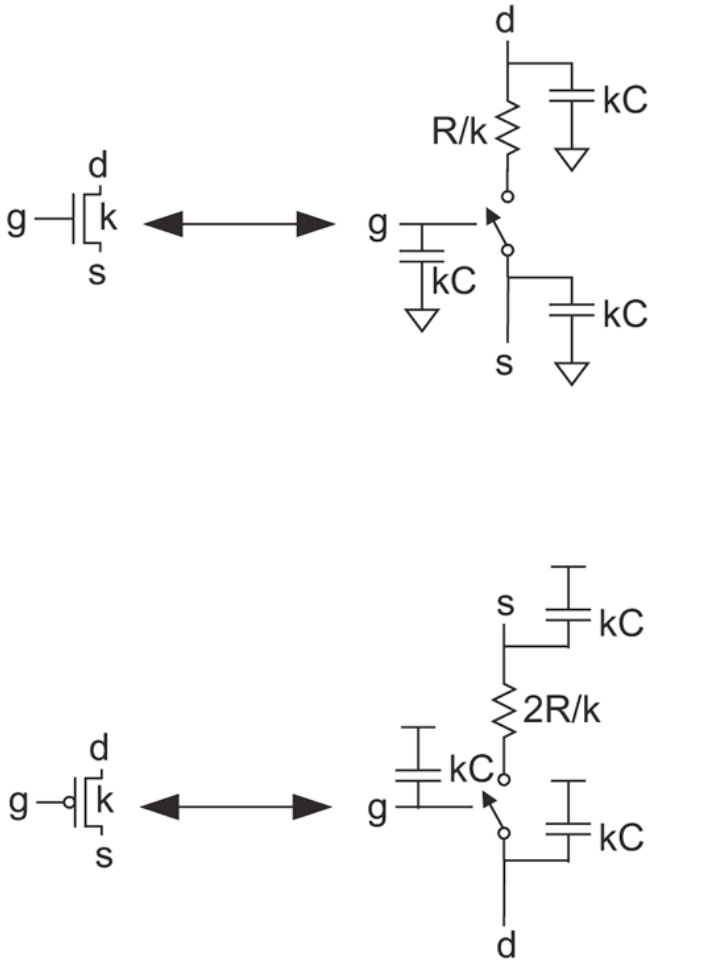


FIG 2.34 Equivalent RC circuit models

Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter

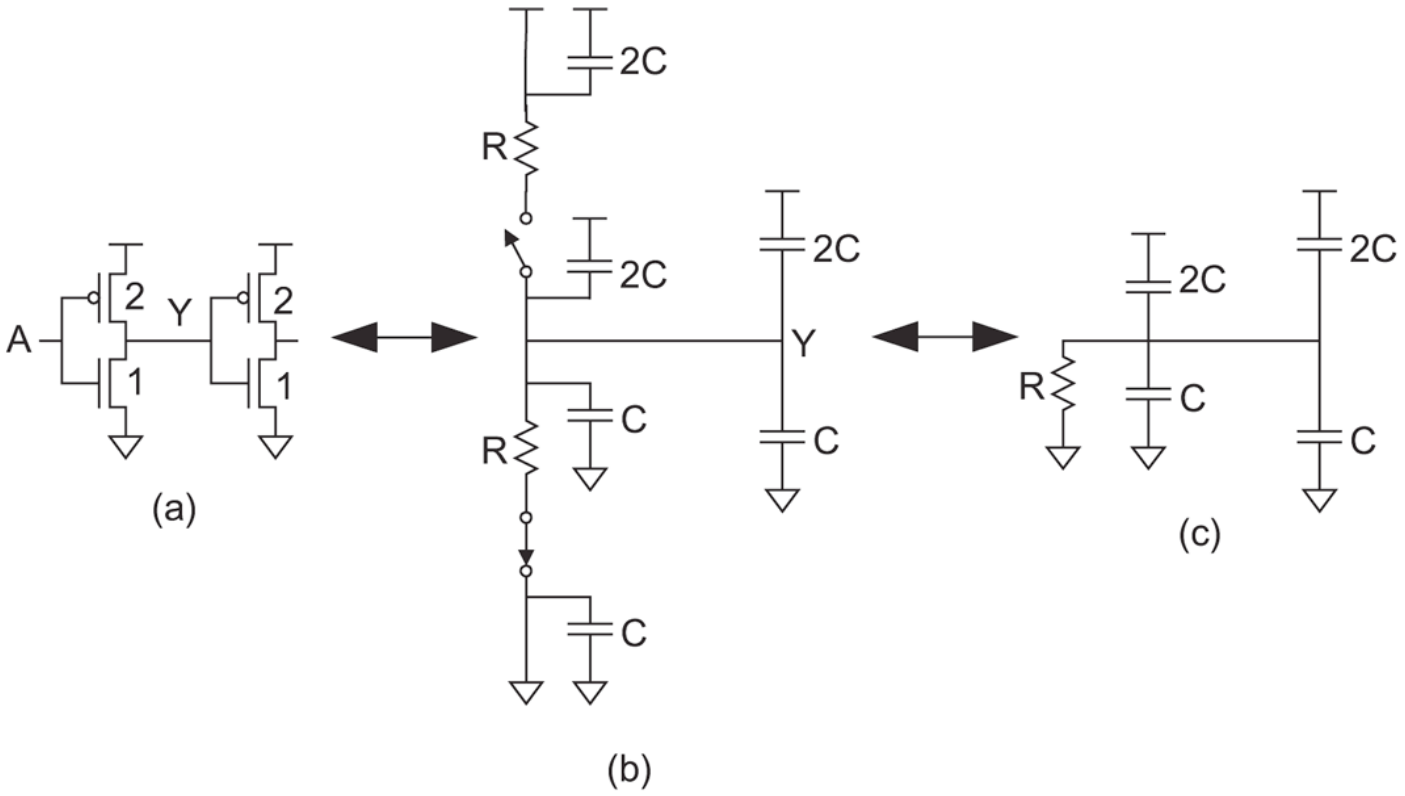


FIG 2.35 Inverter propagation delay

delay = 6RC

Resistance of a unit transmission gate

- The effective resistance of a transmission gate is the parallel of the resistance of the two transistor
- Approximately R in both directions
- Transmission gates are commonly built using equal-sized transistors
- Boosting the size of the pMOS only slightly improve the effective resistance while significantly increasing the capacitance

Effective resistance of a transistor passing a value in its poor direction ≈ double

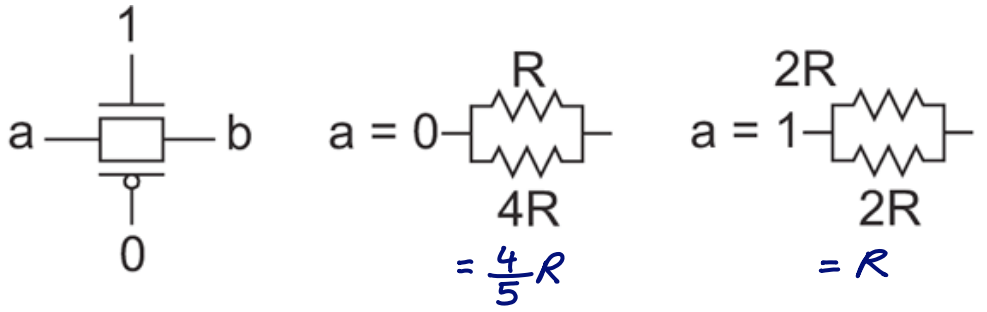


FIG 2.36 Effective resistance of a unit transmission gate

Summary

- Models are only approximations to reality, not reality itself
- Models cannot be perfectly accurate
  - Little value in using excessively complicated models, particularly for hand calculations
- To first order current is proportional to W/L
  - But, in modern transistors L_{eff} is shorter than L_{drawn}
    - Doubling the L_{drawn} reduces current more than a factor of two
    - Two series transistors in a modern process deliver more than half the current of a single transistor
- Use Transmission gates in place of pass transistors
- Transistor speed depends on the ratio of current to capacitance
  - Sources of capacitance (voltage dependents)
    - Gate capacitance
    - Diffusion capacitance