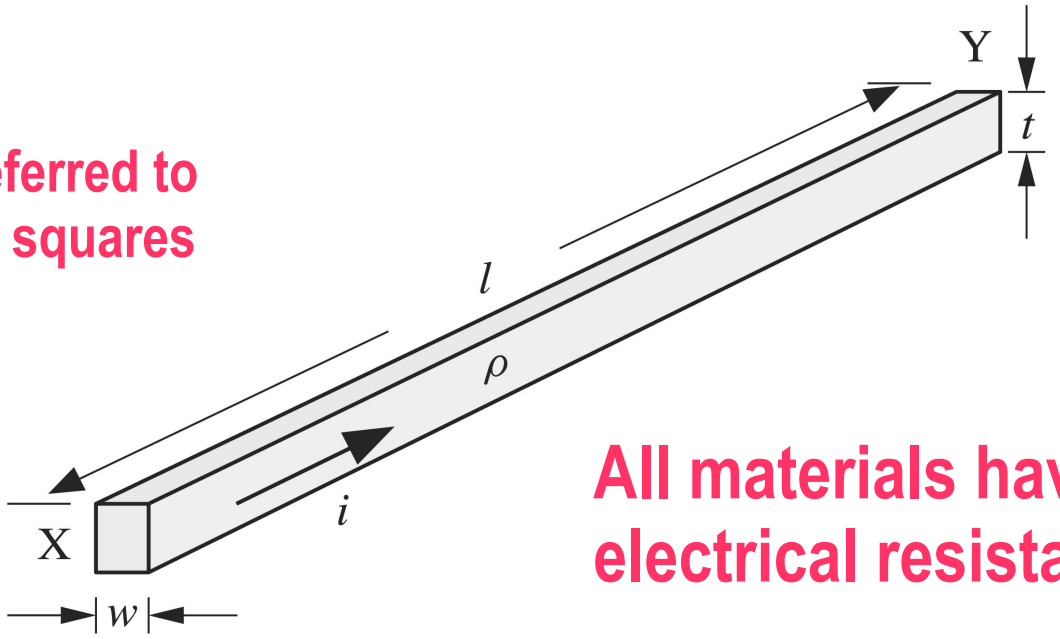
Interconnects

Figure 2.15:
Line geometry



The ratio l/w is referred to as the number of squares of wire

All materials have electrical resistance

$$v_{XY} = R \cdot i$$

Sheet Resistance

$$R = \rho \frac{l}{A} = \rho \frac{l}{t \cdot w} = \frac{\rho}{t} \frac{l}{w} = R_{\square} \frac{l}{w}$$

Resistance

To keep the resistance of long wire small we must make its width big

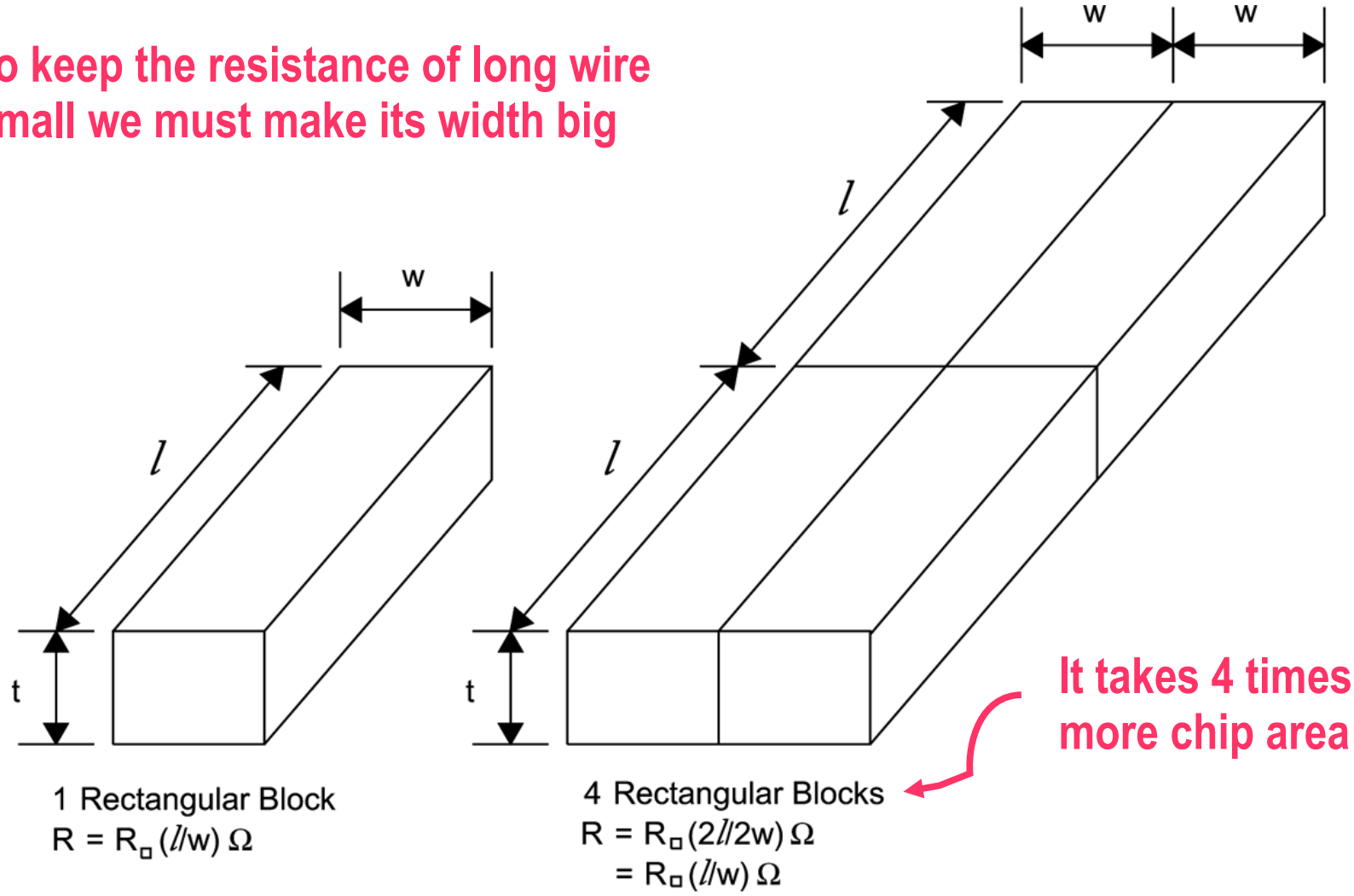


FIG 4.32 Two conductors with equal resistance

Resistivity

Resistivity depends on temperature

Table 4.6 Bulk resistivity of pure metals at 22° C	
Metal	**Resistivity (μΩ • cm)**
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Molybdenum (Mo)	5.3
Titanium (Ti)	43.0

Sheet Resistance

Table 4.7 Sheet resistances

Layer	Sheet Resistance (Ω / □)
Diffusion (silicided)	3–10
Diffusion (unsilicided)	50–200
Polysilicon (silicided)	3–10
Polysilicon (unsilicided)	50–400
Metal1	0.08
Metal2	0.05
Metal3	0.05
Metal4	0.03
Metal5	0.02
Metal6	0.02

Silicide:
process of coating a material with a refractory metal such as tugsten to decrease the overall resistivity

A refractory material is one that retains its strength at high temperatures

Polysilicon and Diffusion have high resistance (even if silicided)

Polysilicon and Diffusion

- Diffusion has high resistance and high capacitance (about 2 fF/μm: comparable to gate capacitance)
- Avoid diffusion (*runners)* for wires !

- Polysilicon has lower capacitance but still high resistance
- Use for transistor gates
- Only occasionally for very short wires between gates

Resistance of Contacts and Vias

- Contacts and vias have resistance associated with them (2 – 20 Ω)
- Use multiple small contacts rather a single large contact

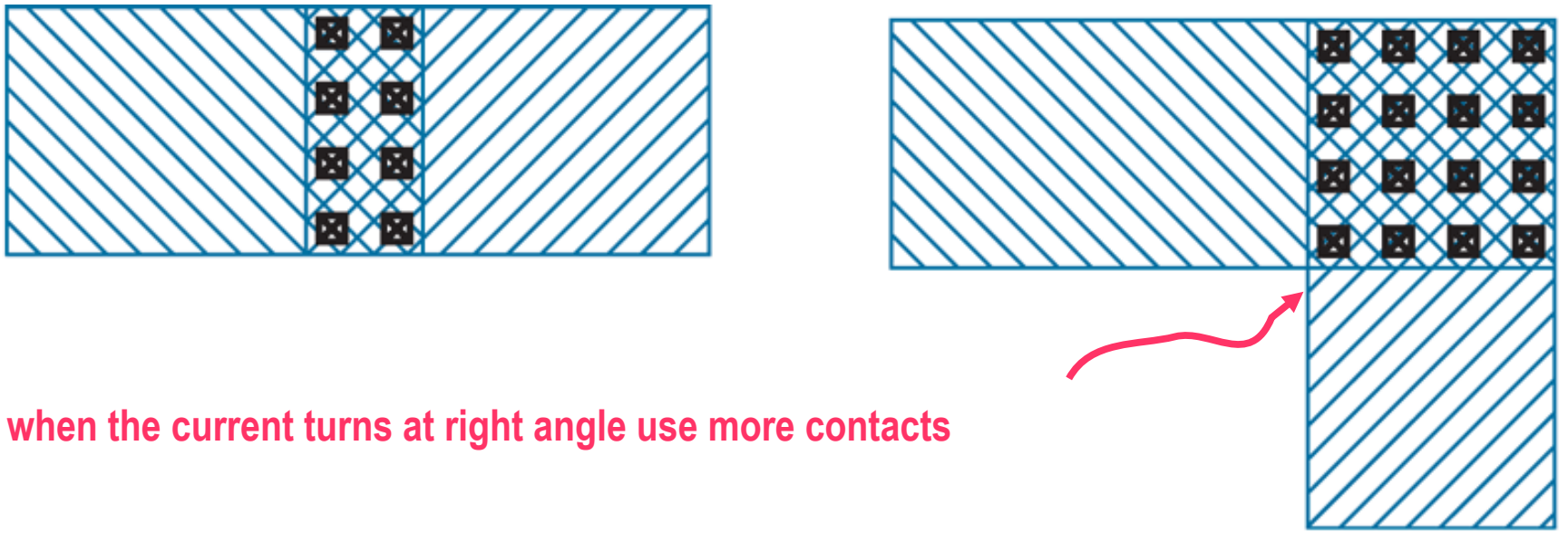
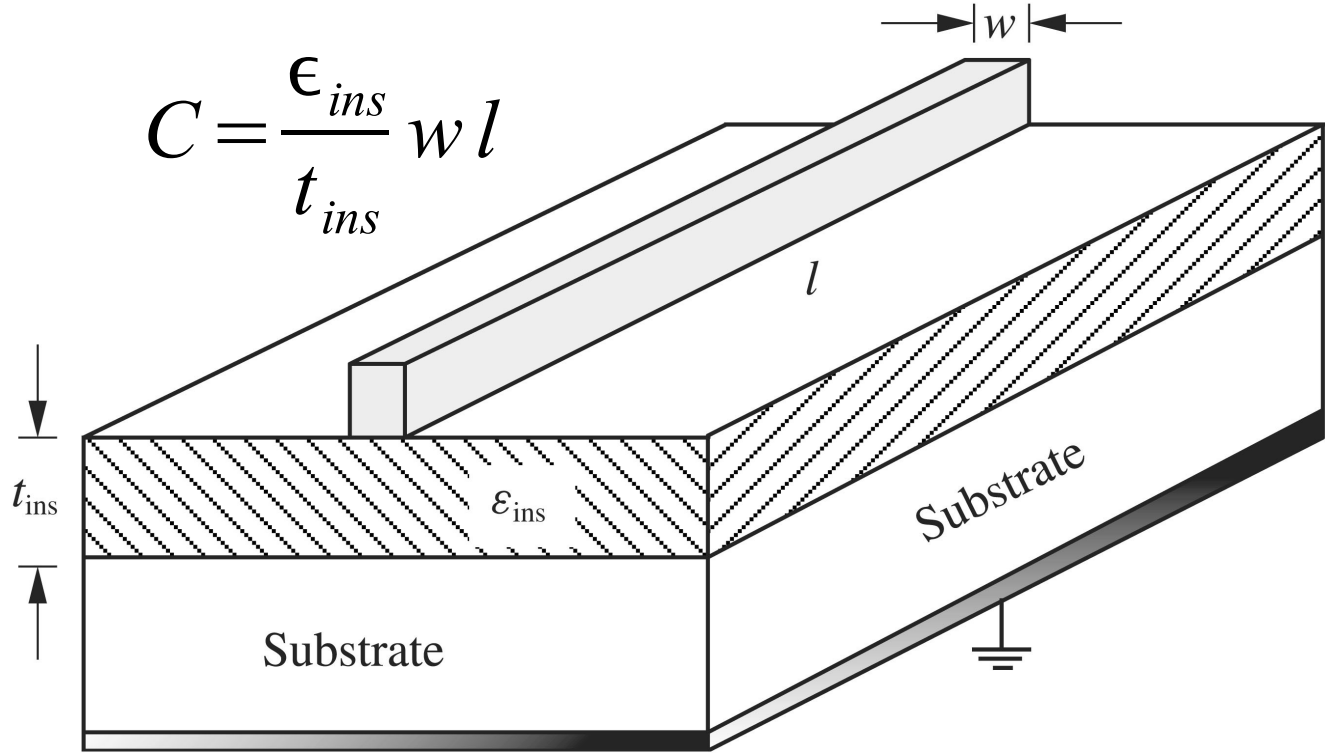


FIG 4.33 Multiple vias for low-resistance connections

Interconnects

A conducting line patterned on top of an insulating layer creates a capacitance w.r.t. the silicon substrate

$$C = \frac{\epsilon_{ins}}{t_{ins}} w\, l$$



$$i = C \frac{dv}{dt}$$

Changing the capacitor voltage by an amount Δv requires a time interval:

$$\Delta t = \frac{C}{i} \Delta v$$

In other words there is a delay in the transmission of the electric signal

Fringe Capacitance

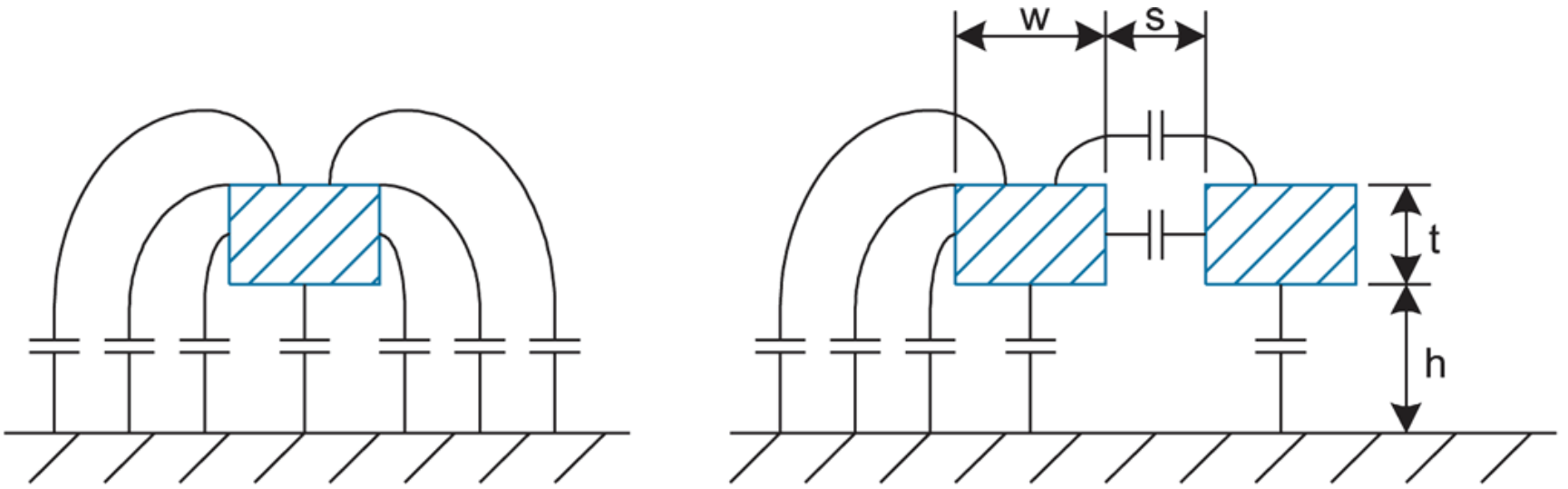
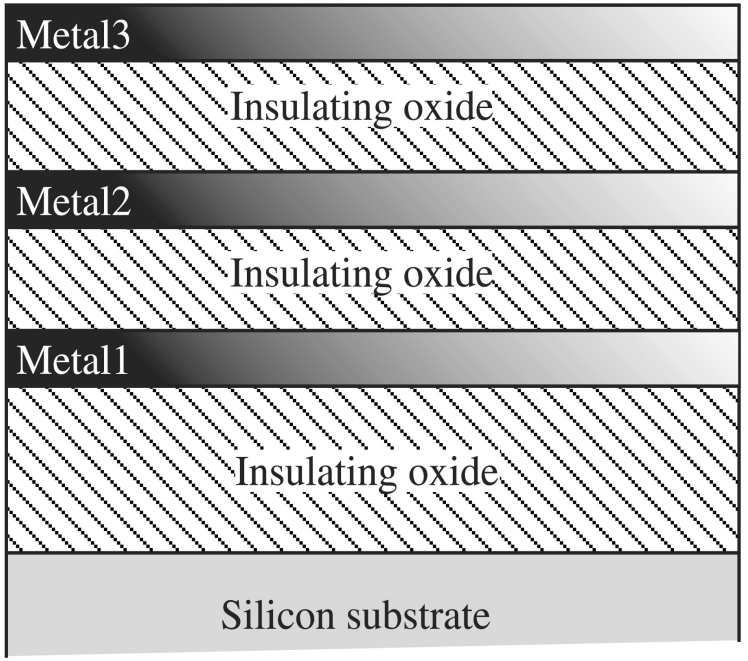
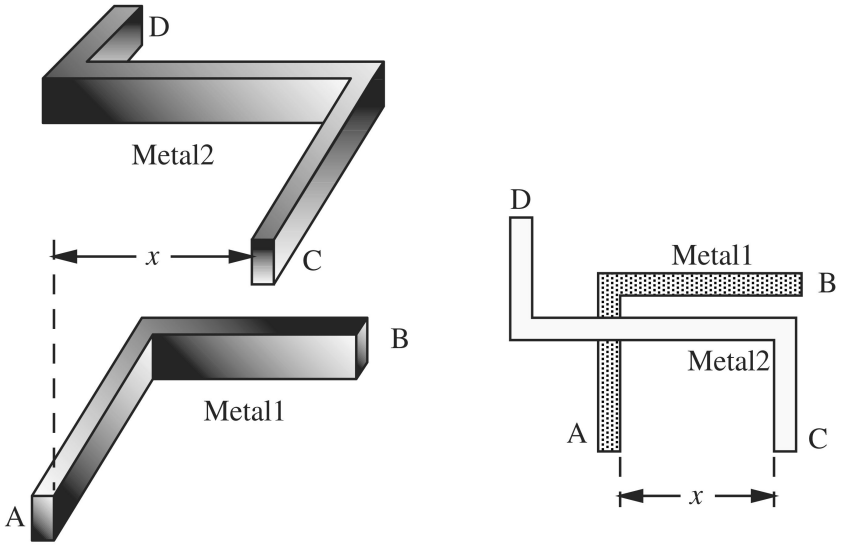


FIG 4.34 Effect of fringing fields on capacitance

Multilayer Capacitance





(a) 3-dimensional perspective (b) Top view

- Line to to Line capacitance
- Overlap capacitance

$$C_{total} = C_{bot} + C_{top} + 2C_{adj}$$

$$C_{gnd} = C_{bot} + C_{top}$$

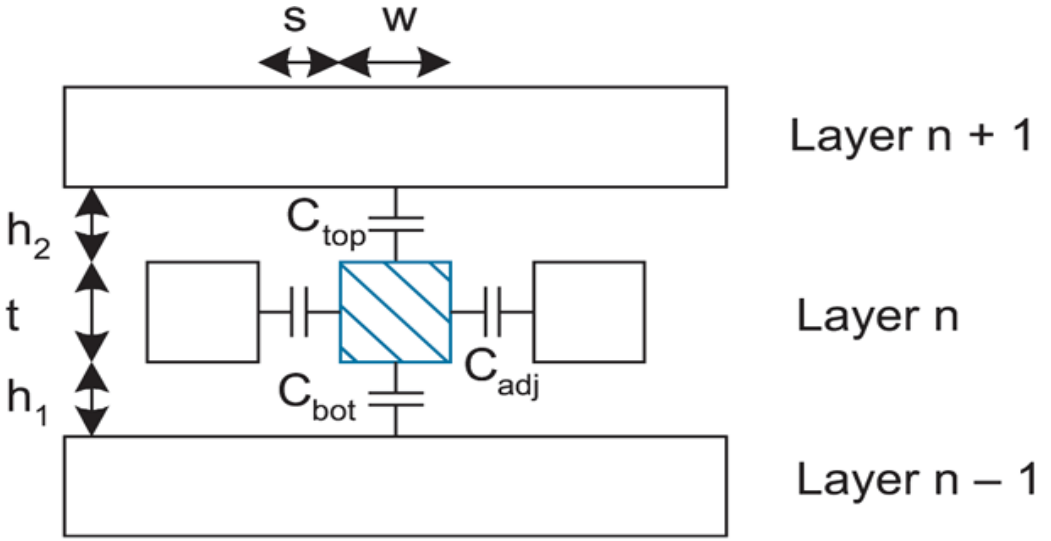
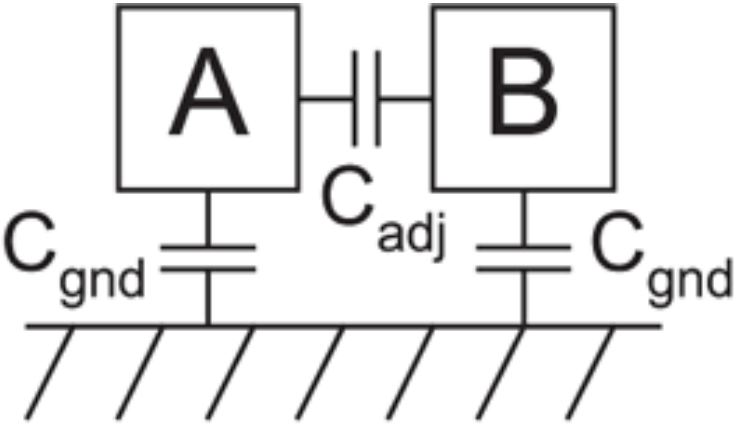
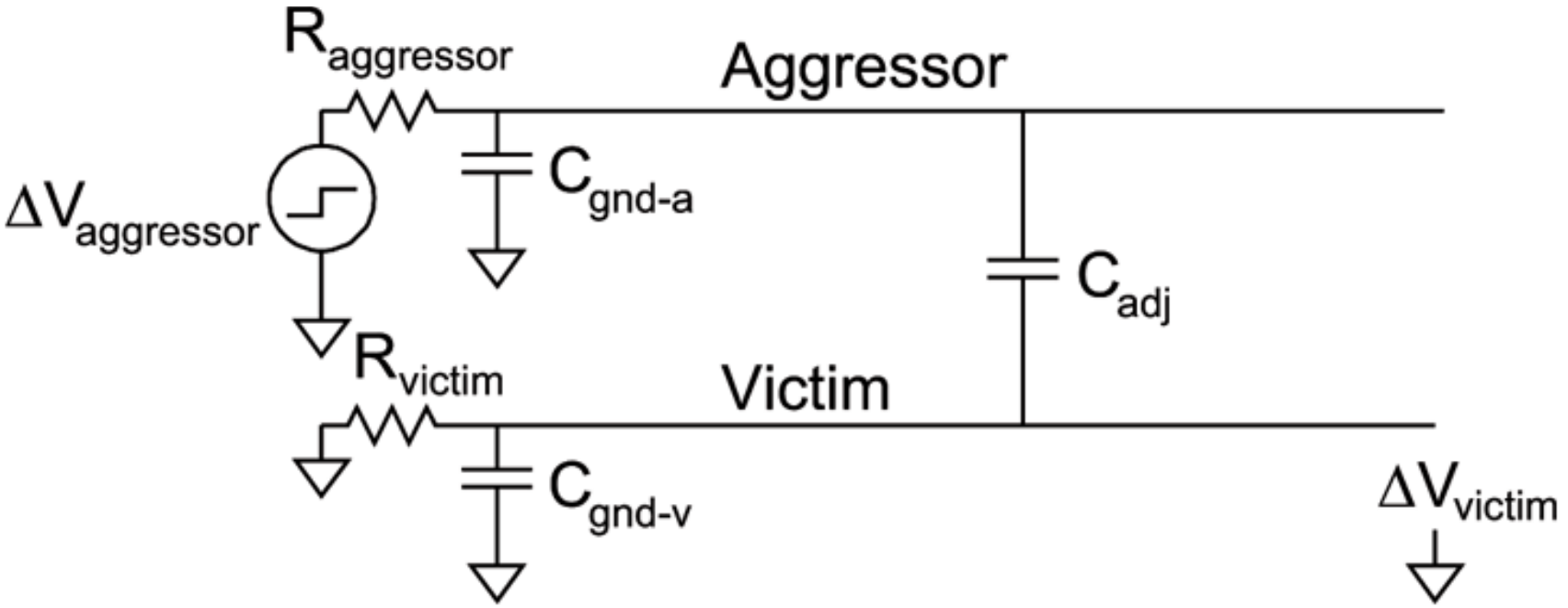


FIG 4.36 Multilayer capacitance model

Crosstalk

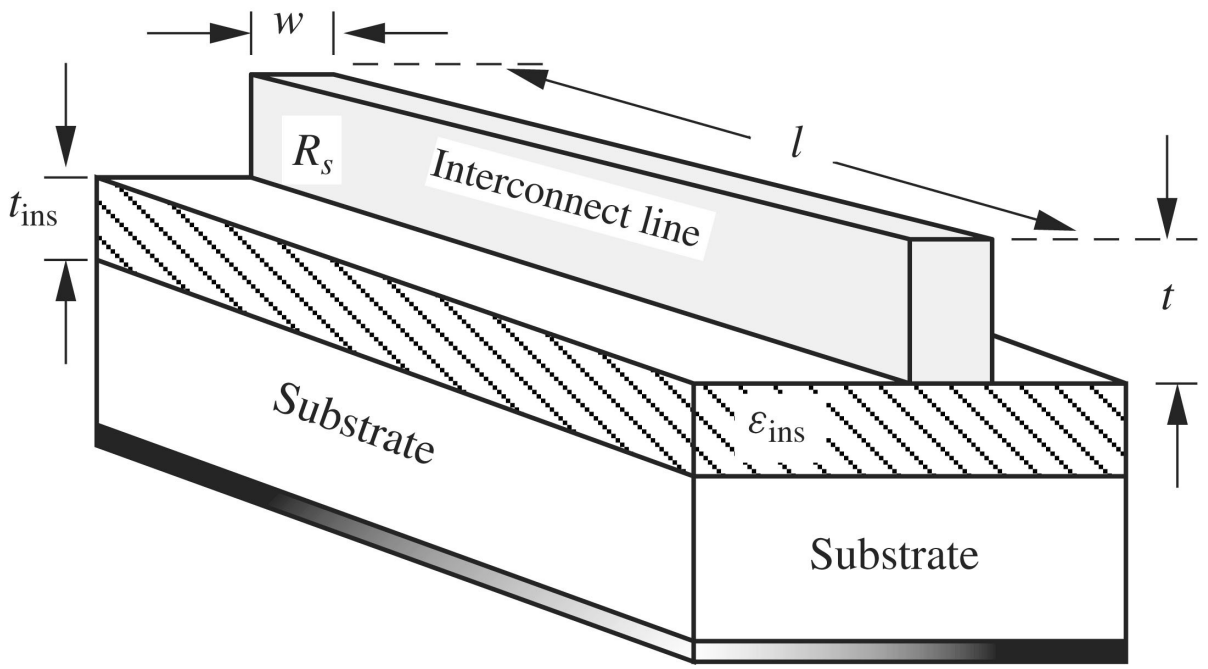
- Delay effects
- Noise Effects





Modeling a single interconnect line

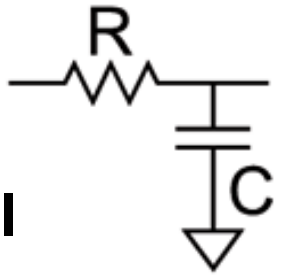
Figure 12.1: Interconnect line geometry



$$R = \frac{\rho}{t}\frac{l}{w}$$

$$C = \frac{\epsilon_{ins}}{t_{ins}} w\, l$$

Simple RC lumped model



L-model

$$\tau = RC = \frac{\rho\,\epsilon_{ins}}{t\,t_{ins}} l^2 = \kappa\, l^2$$

The time delay on an RC line is proportional to the square of its length

Delay and Rise Time of a simple RC

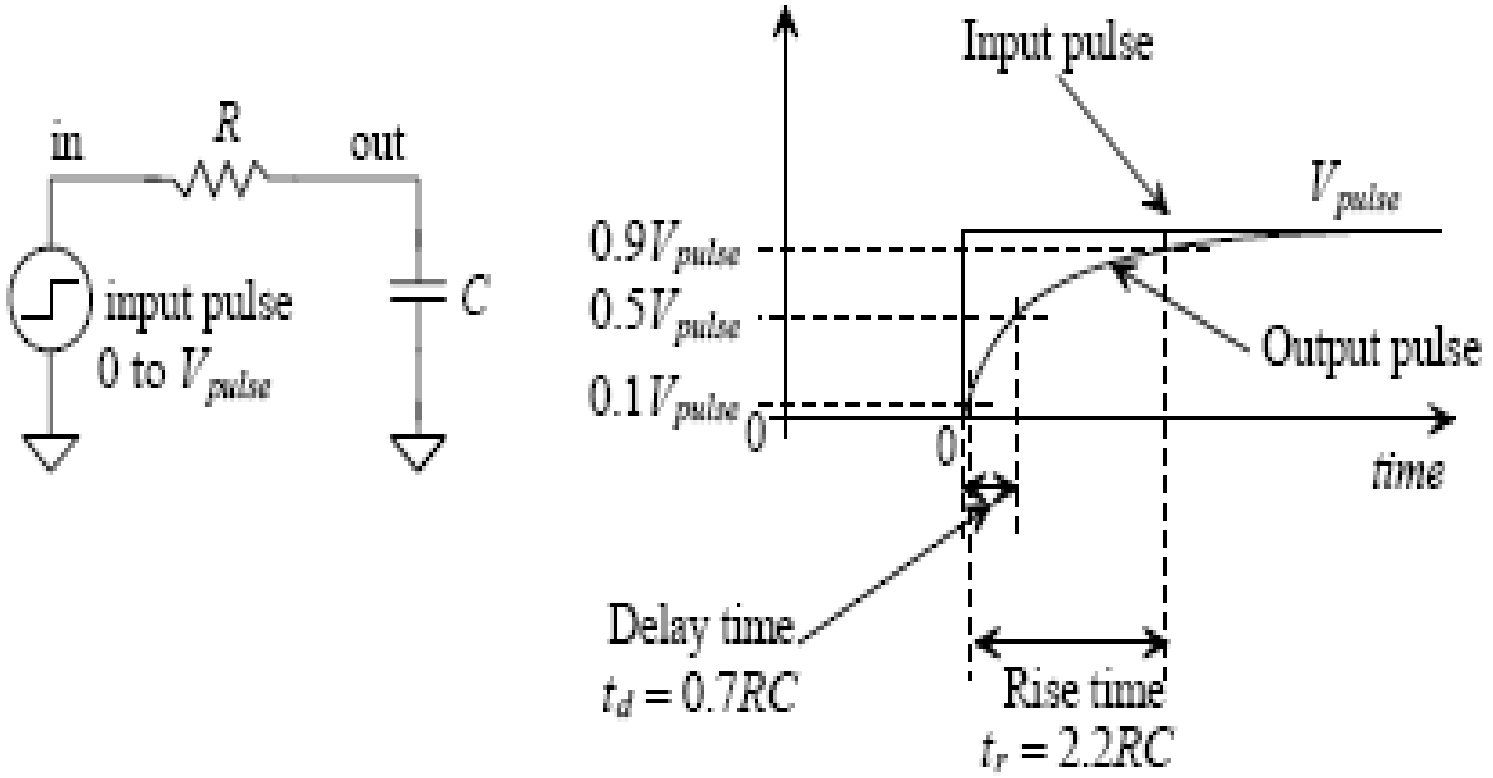


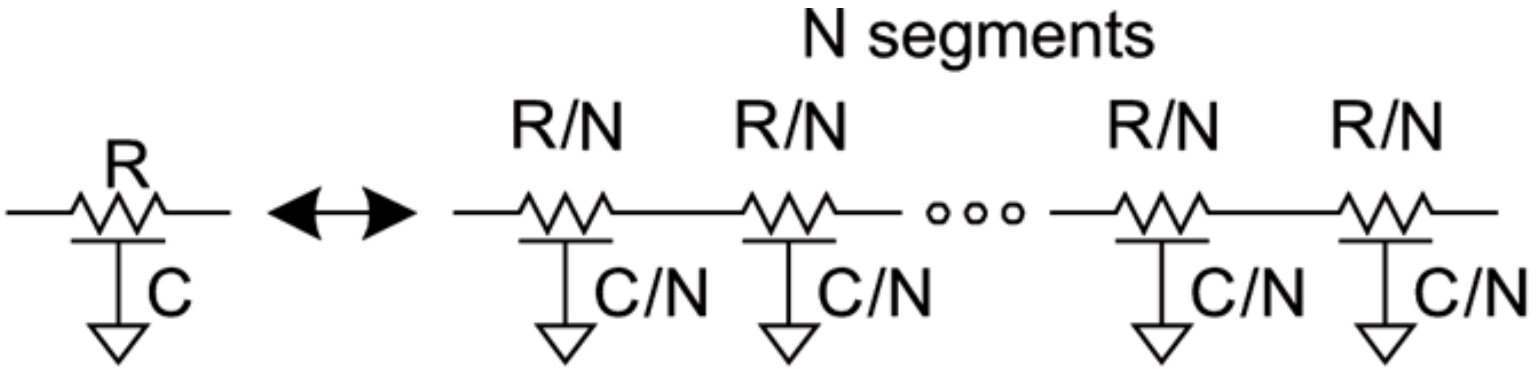
Figure 2.21 Rise and delay times in an RC circuit.

$$V_{inp}(t) = V_{pulse} \cdot u(t)$$

$$V_{out}(t) = V_{pulse}\left[1 - e^{-t/\tau}\right]$$

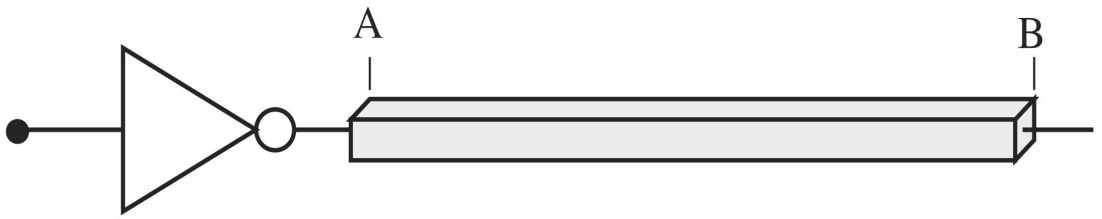
Lumped vs. Distributed RC model

- In reality the resistance and capacitance of the line is distributed along its entire length

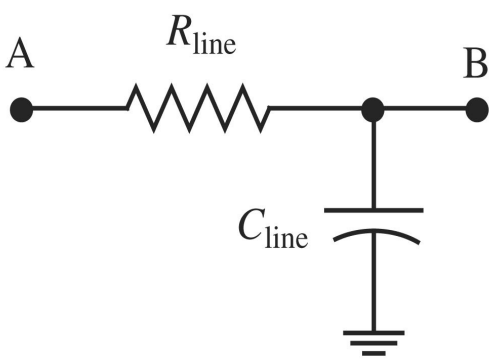


Improving the lumped-element RC model

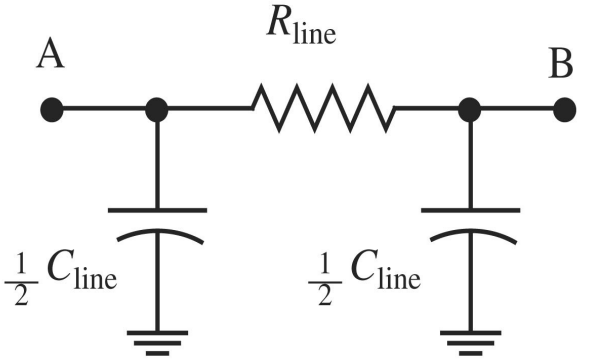
- Placing the capacitance at the end overestimate its effect



(a)



(b) Simple model



(c) Better model

$$\tau = RC$$

$$\tau = \frac{1}{2} RC$$

Lumped vs. Distributed Delay

Vin(t) = u(t)

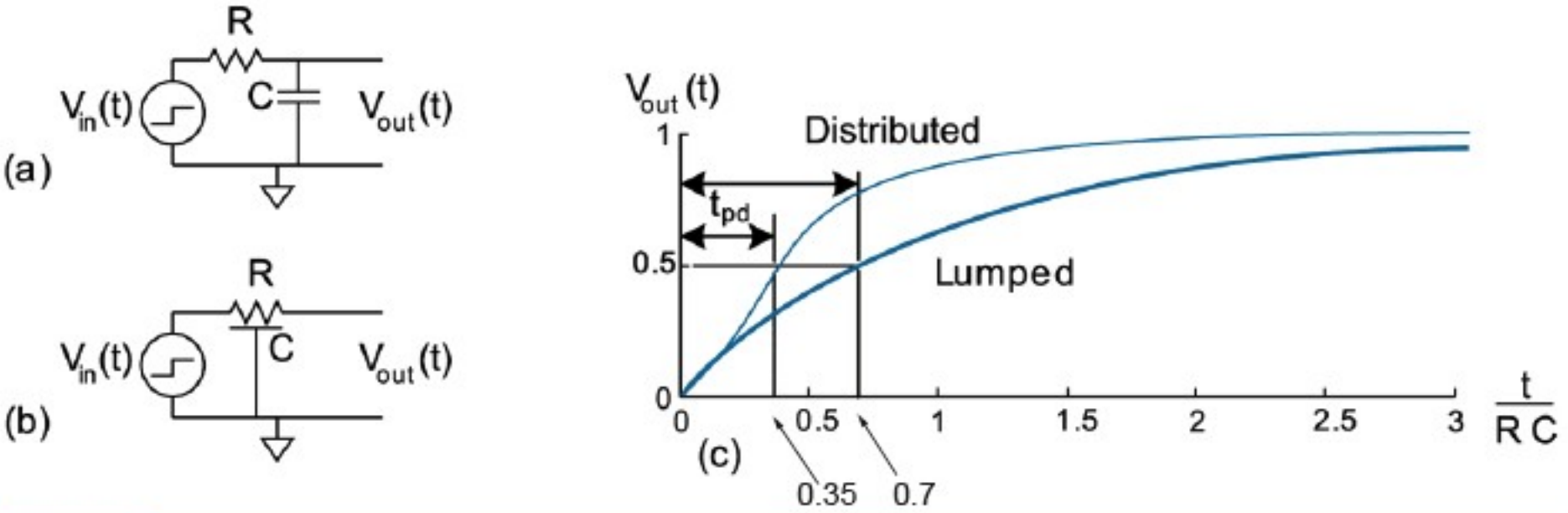


FIG 4.48 Lumped and distributed RC circuit response

Lumped approximations

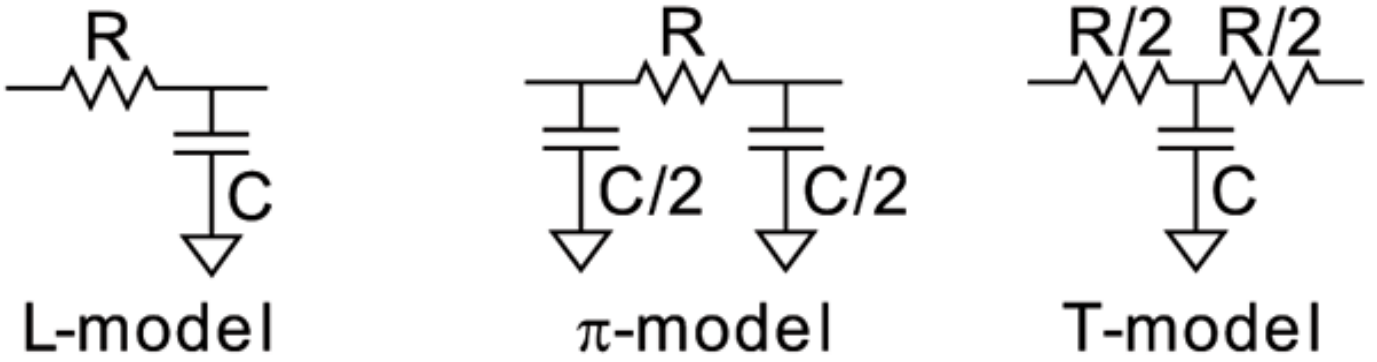
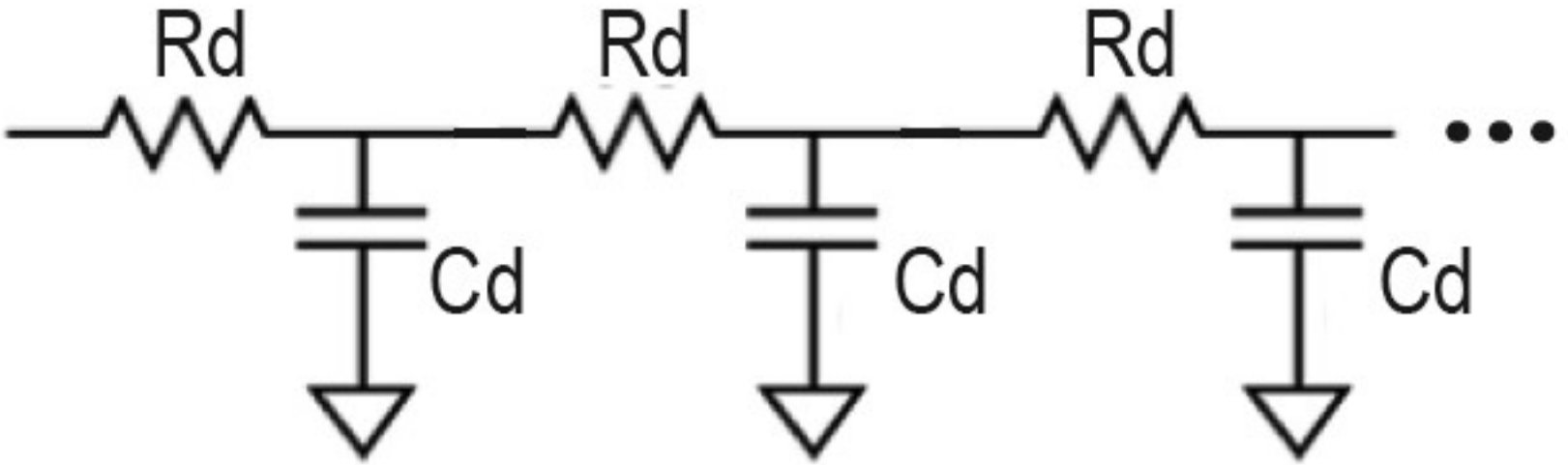


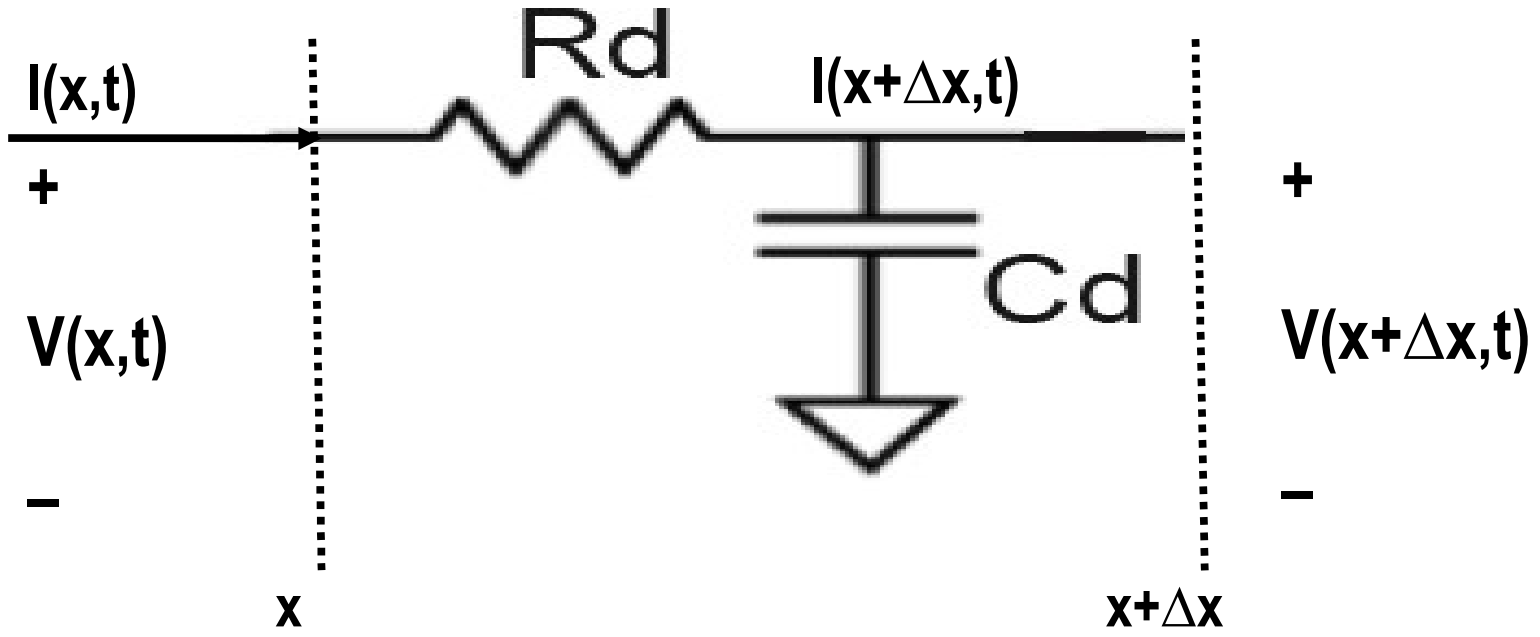
FIG 4.38 Lumped approximation to distributed RC circuit

- The L model is a very poor choice
- The π and T model are equivalent
- It is common practice to model long wires with 3- or 4- π segments

Delay through a distributed RC



Distributed RC: analytical approach (1)



$$\begin{cases} V(x,t) - V(x+\Delta x,t) = R_d I(x,t) \\ I(x,t) - I(x+\Delta x,t) = C_d \dfrac{\partial V(x+\Delta x,t)}{\partial t} \end{cases}$$

Distributed RC: analytical approach (2)

$C_d, R_d ????$ ← Capacitance and resistance of a single distributed cell

Capacitance and resistance per unit length → $C_u = \frac{C}{l}$, $R_u = \frac{R}{l}$ → $C_d = C_u \cdot \Delta x$, $R_d = R_u \Delta x$

$$\begin{cases} V(x,t) - V(x+\Delta x, t) = R_u \Delta x \, I(x,t) \\ I(x,t) - I(x+\Delta x, t) = C_u \Delta x \dfrac{\partial V(x+\Delta x, t)}{\partial t} \end{cases}$$

$$\begin{cases} \dfrac{V(x,t) - V(x+\Delta x, t)}{\Delta x} = R_u I(x,t) \\ \dfrac{I(x,t) - I(x+\Delta x, t)}{\Delta x} = C_u \dfrac{\partial V(x+\Delta x, t)}{\partial t} \end{cases}$$

Distributed RC: analytical approach (3)

$$\begin{cases} \dfrac{V(x,t)-V(x+\Delta x)}{\Delta x} = R_u I(x,t) \\ \dfrac{I(x,t)-I(x+\Delta x)}{\Delta x} = C_u \dfrac{\partial V(x+\Delta x)}{\partial t} \end{cases}$$

- If we let $\Delta x \longrightarrow 0$ (and recall that): $$f'(x) = \lim_{h \to 0} \frac{f(x+h)-f(x)}{h}$$

$$\begin{cases} \dfrac{\partial V(x,t)}{\partial x} = -R_u I(x,t) \\ \dfrac{\partial I(x,t)}{\partial x} = -C_u \dfrac{\partial V(x,t)}{\partial t} \end{cases} \longrightarrow \frac{\partial}{\partial x}\left(\frac{\partial V}{\partial x}\right) = -R_u \frac{\partial I}{\partial x}$$

$$\frac{\partial^2 V}{\partial x^2} = R_u C_u \frac{\partial V}{\partial t}$$

Distributed RC: analytical approach (4)

$$\frac{\partial^2 V(x,t)}{\partial x^2} = \frac{RC}{l^2}\frac{\partial V(x,t)}{\partial t}$$

Diffusion Equation
Does not have a closed form solution !!!

The input voltage is applied at x=0

Using an input of V(0,t) = $V_p u(t)$ the solution at any point x is:

$$V(x,t) = V_P \cdot erfc\left(\frac{x}{2}\sqrt{\frac{RC}{l^2 t}}\right)u(t)$$

With:

$$erfc(\eta) = 1 - erf(\eta) = \frac{2}{\sqrt{\pi}}\int_{\eta}^{\infty} e^{-\alpha^2} d\alpha$$

$$\frac{d}{d\eta} erfc(\eta) = \frac{-2e^{-\eta^2}}{\sqrt{\pi}}$$

$$erf(\eta) = \frac{2}{\sqrt{\pi}}\int_{0}^{\eta} e^{-\alpha^2} d\alpha$$

$$erf(0) = 0$$
$$erf(\infty) = 1$$
$$erf(-\eta) = -erf(\eta)$$

Practical interconnect modeling

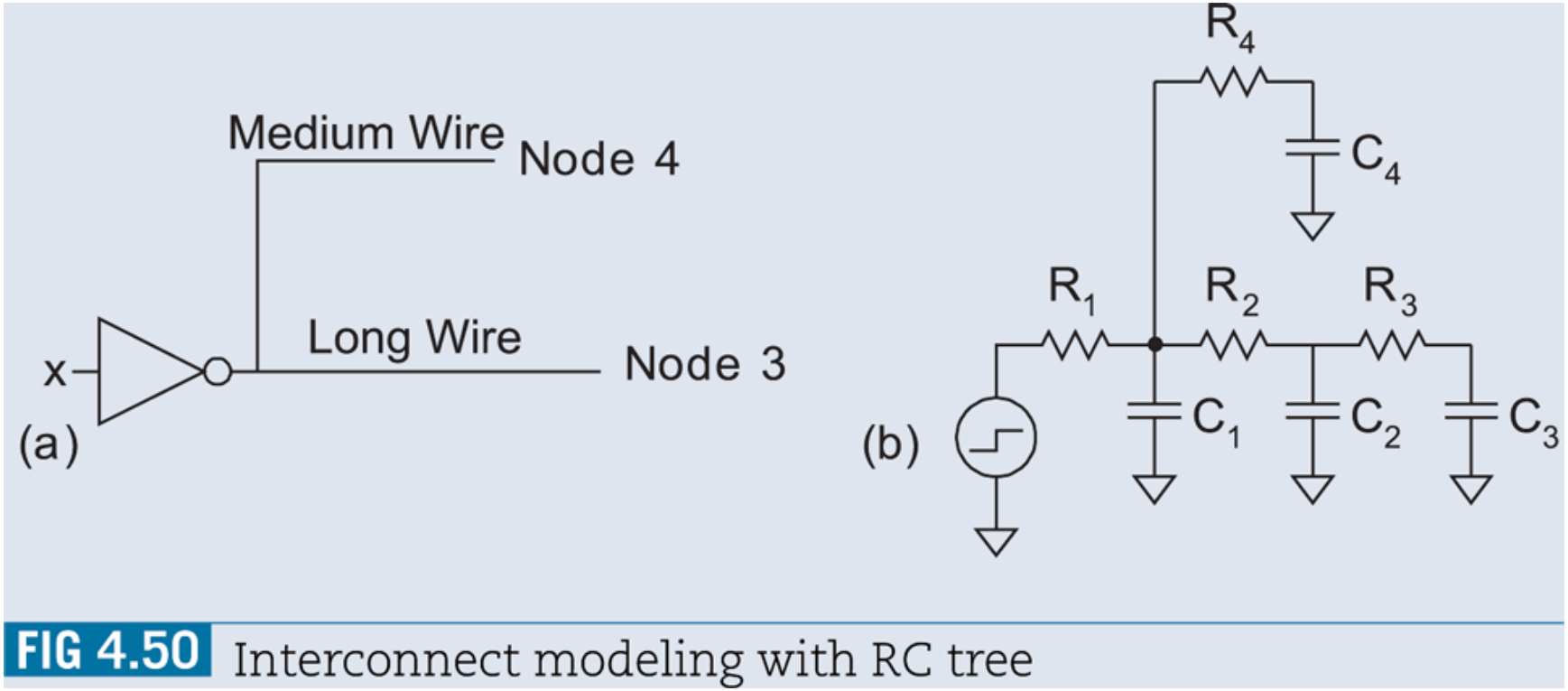


FIG 4.50 Interconnect modeling with RC tree

- The driver is modeled by a voltage source and its source resistance R1
- The medium wire is modeled by a single segment
- The long wire is modeled by two π-segments

Elmore Delay approximation

- For a general RC network we compute the Elmore delay as:

$$\tau_i = \sum_k C_k \times R_{ik}$$

- where:
  - the node of interest is node i
  - C_k is the capacitance at node k
  - R_{ik} is the sum of all resistances in common from the source to node i and the source to node k

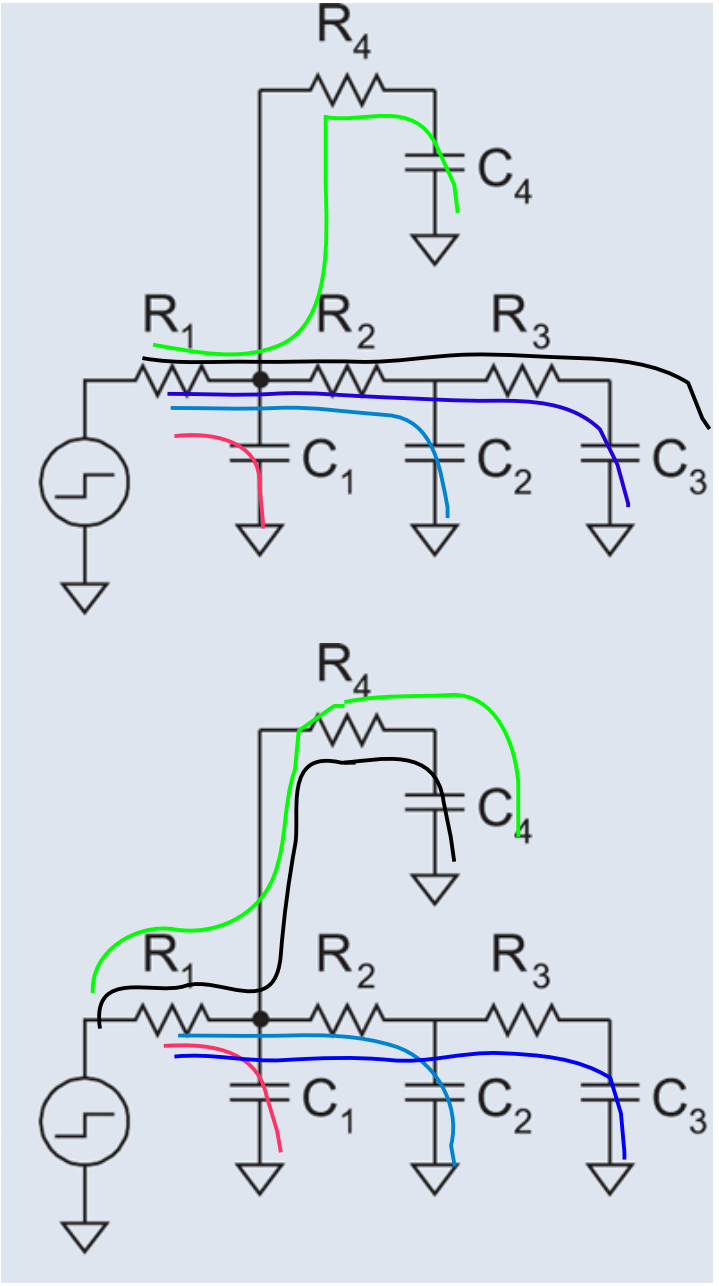
Example of Elmore Delay Calculation

T_{D3} =

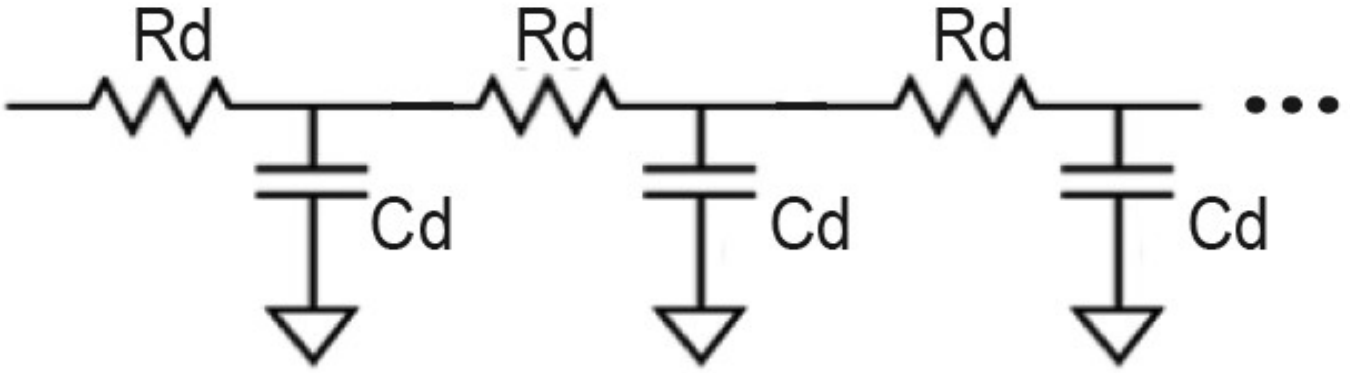
C1 R1 +
C2 (R1+R2) +
C3 (R1+R2+R3) +
C4 R1

T_{D4} =

C1 R1 +
C2 R1 +
C3 R1 +
C4 (R4 + R1)



Distributed RC: approximated approach



- Assume the line has N sections and use Elmore approximation:

$$\tau = \frac{C}{N}\frac{R}{N} + \frac{C}{N}\left(\frac{R}{N} + \frac{R}{N}\right) + \frac{C}{N}\left(\frac{R}{N} + \frac{R}{N} + \frac{R}{N}\right) + \ldots (N\ terms)$$

$$\tau = \frac{CR}{N^2}(1 + 2 + \ldots + N) = \frac{CR}{N^2}\sum_{i=1}^{N} i = \frac{CR}{N^2}\frac{N(N+1)}{2} \underset{N\to\infty}{\rightarrow} \frac{RC}{2}$$

Improving interconnect delay through repeaters

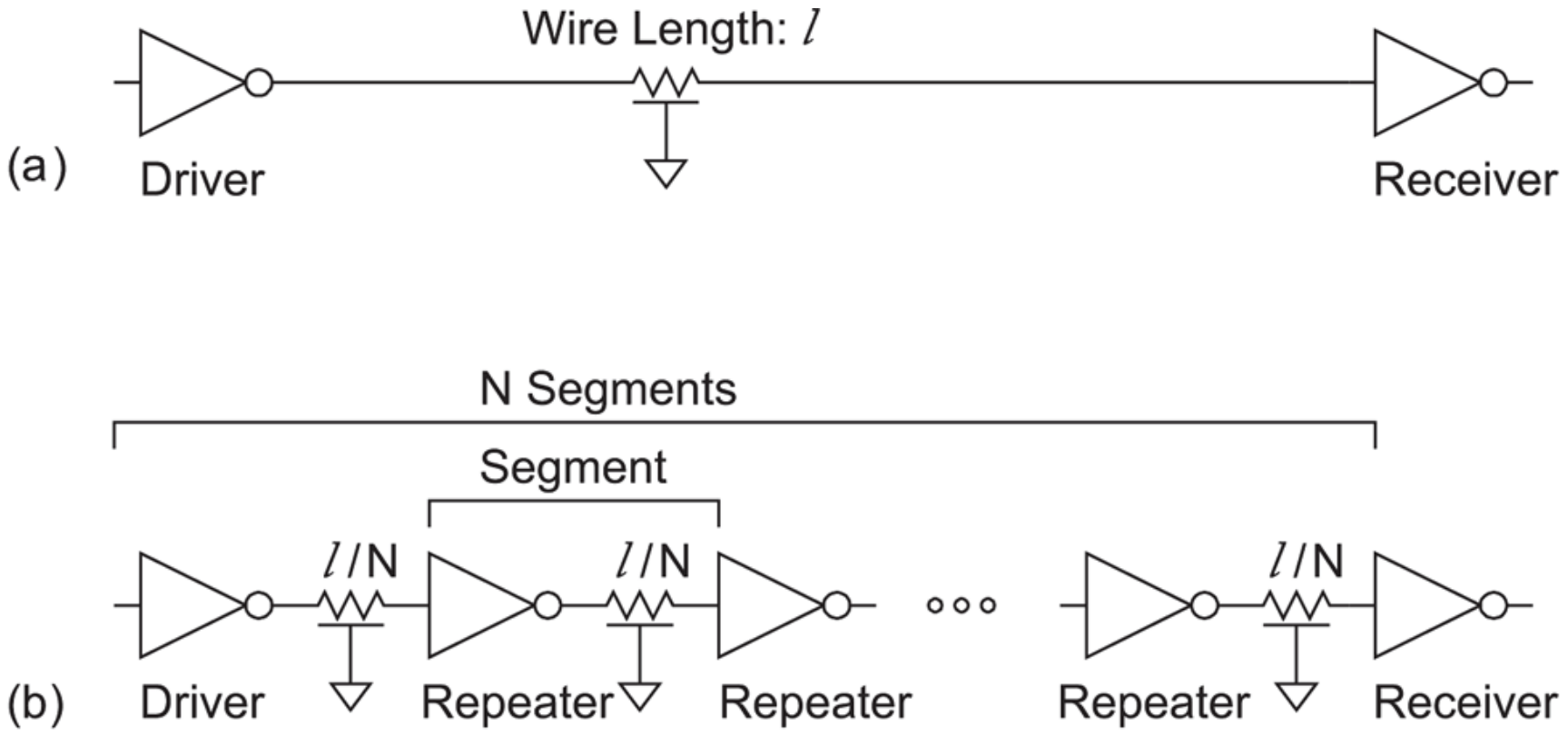


FIG 4.53 Wire with and without repeaters

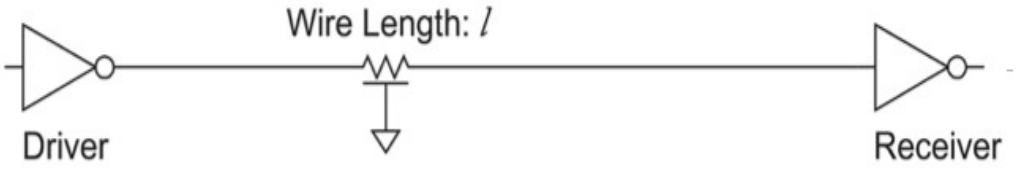
Example of repeaters

$$r = 20\ \Omega/\mu m \text{ with } r = R/\ell$$

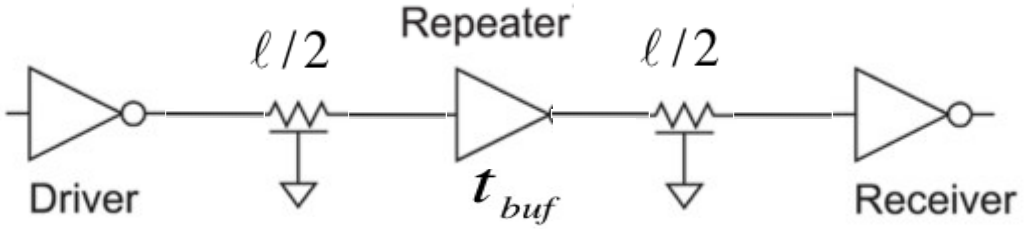
$$c = 4 \times 10^{-4}\ pF/\mu m \text{ with } c = C/\ell$$

$$\ell = 2mm$$

without repeater :



$$tp \approx \frac{0.7}{2} rc\ell^2 = 11.2ns$$



with repeater :

$$tp = 2.8ns + t_{buf} + 2.8ns = 5.6ns + t_{buf}$$

Summary: important results

- **Step Response of lumped and distributed RC networks**

Voltage Range	Lumped RC	Distributed RC
0→50% (tp)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (tr)	2.2 RC	0.9 RC
0→90%	2.3 RC	1.0 RC

Design Rules of Thumbs

- w.r.t. propagation delay
  - RC effects should be considered only when the propagation delay of the interconnect is comparable or larger than the propagation delay of the driving gate

$$L_{crit} = \sqrt{\frac{t_{pgate}}{0.38\,RC/l^2}}$$

RC delays become dominant for interconnect wires longer than L_{crit}

- w.r.t. rise (fall) time
  - RC effects should be considered only when the rise (fall) time at the line's input is smaller than the rise (fall) time of the line (≈0.9 RC)

$$t_{rise} < 0.9\,RC$$

If this condition occurs the RC delay is such that the line cannot keep up with the rate of change of the signal applied to it