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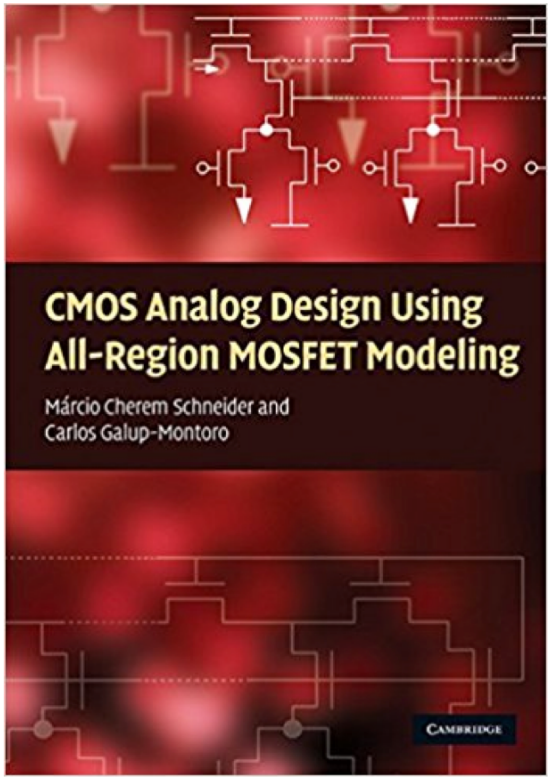
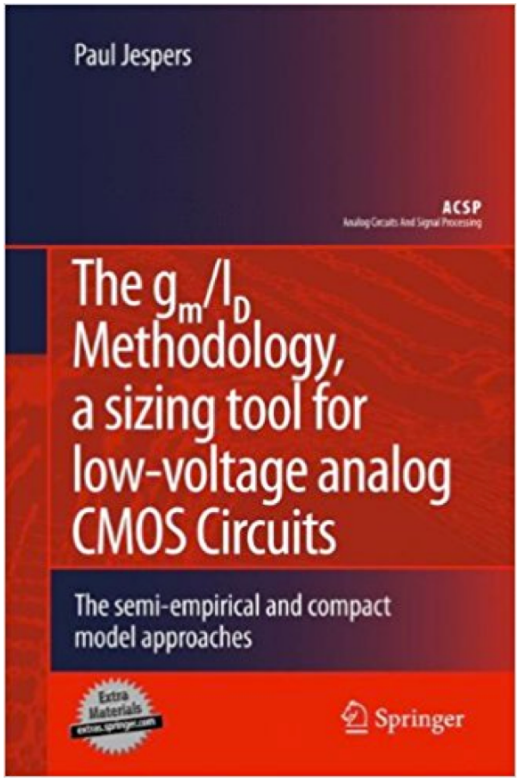
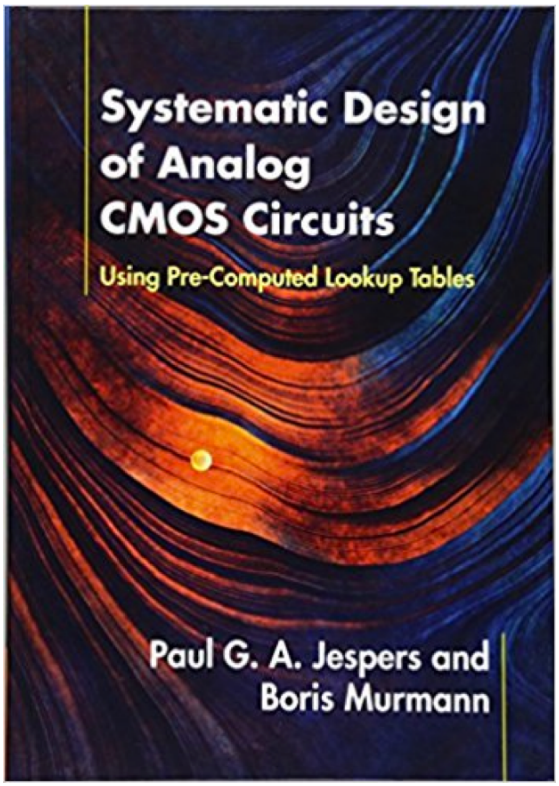
# Systematic Design of Analog CMOS Circuits Using $g_m/I_D$-Based Lookup Tables

Claudio TALARICO

# Systematic Design of Analog CMOS Circuits Using $g_m/I_D$-based Lookup Tables



# Research Projects: TIA

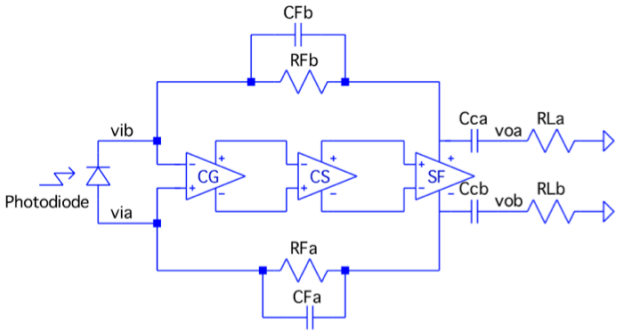
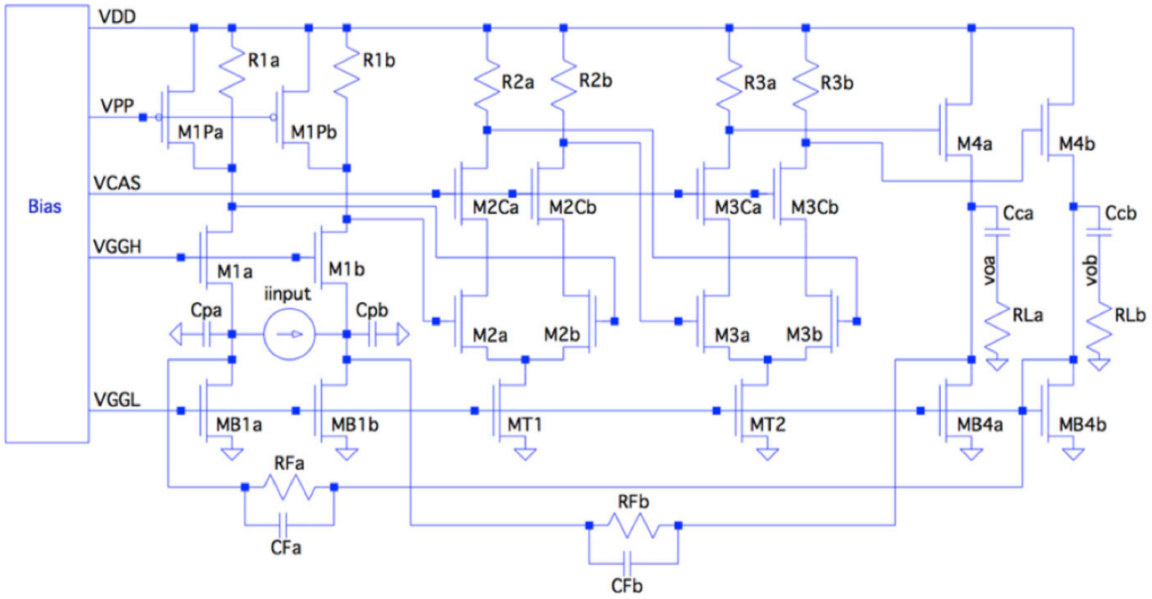



**Table 4** Performance comparison of state-of-the-art CMOS TIAs

| Spec. | [3] | [4] | [9] | [14] | [2] | This work |
|---|---|---|---|---|---|---|
| Gain (dBΩ) | 66 | 66.02 | 94.96 | 69.8 | 72 | 78.34 |
| BW (GHz) | 2.1 | 22 | 0.0018 | 1 | 2.4 | 2.21 |
| Cin (pF) | 0.5 | 0.5 | 2 | 0.5 | 0.5 | 0.5 |
| Input ref. noise (pA/$\sqrt{}$Hz) | 10 | 22 | 0.065 | 4.5 | 18.12 | 11.91 |
| $P_{DISS}$(mW) | 7.2 | 75 | 0.436 | 4.62 | 20.57 | 13.5 |
| FOM (Ω*GHz/mW) | 581.95 | 586.7 | 231.19 | 668.9 | 464.4 | 1352 |
| Process (μm) | 0.18 | 0.09 | 0.18 | 0.18 | 0.18 | 0.18 |
| Supply voltage (V) | 1.8 | 1.2 | 1.8 | 3.3 | 1.8 | 1.8 |



# Research Projects: Mixer

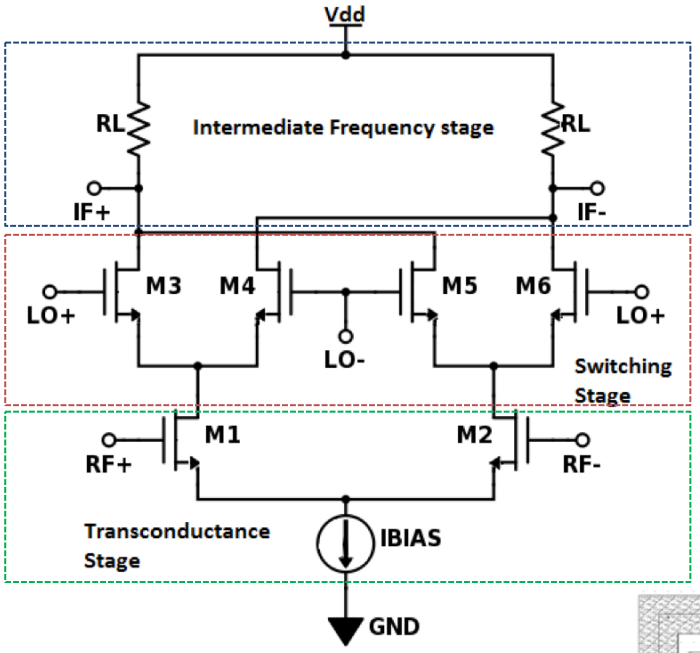
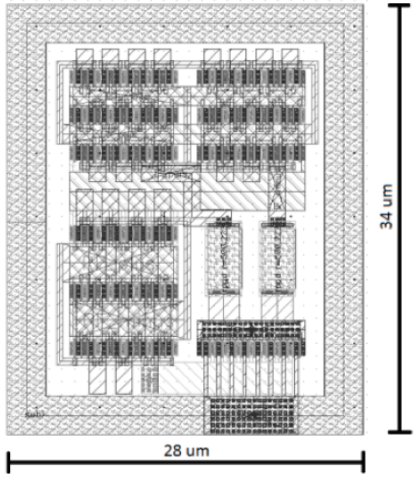



TABLE I. REPORTED PERFORMANCE OF CMOS GILBERT MIXERS

| *Ref.* | *CMOS Tech.* | *Gain [dB]* | *IIP3 [dBm]* | *NF Av. [dB]* | *$P_{DC}$ [mW]* | *FOM* |
|---|---|---|---|---|---|---|
| [4] | 0.13 um | 8 | -3 | 11.2 | 5.57 | 0.12 |
| [9] | 0.18 um | 10 | 4 | 10 | 10 | 0.16 |
| [10] | 0.13 um | 8.95 | -2.2 | 11.4 | 3.7 | 0.16 |
| [11] | 0.13 um | 21 | -1.8 | 15.7 | 18.3 | 0.06 |
| [12] | 0.18 um | 13.5 | -3.25 | 21.22 | 7.2 | 0.06 |
| This Work | 0.13 um | 11.24 | -3.1 | 11.6 | 2.1 | 0.32 |

The performance metrics indicated refers to the core of the mixer




$$FOM = \frac{CG_{[dB]} \cdot IIP3_{[mW]}}{NF_{[dB]} P_{DC[mW]}]}$$

# Research Projects: Distributed LNA for UWB

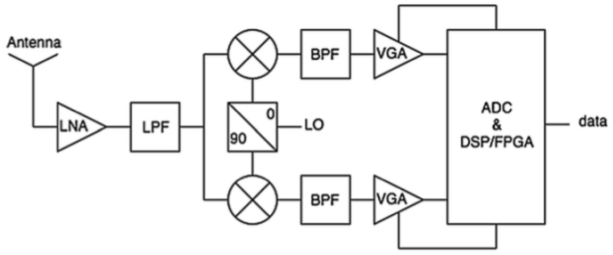



**Fig. 1** Architecture of a UWB system

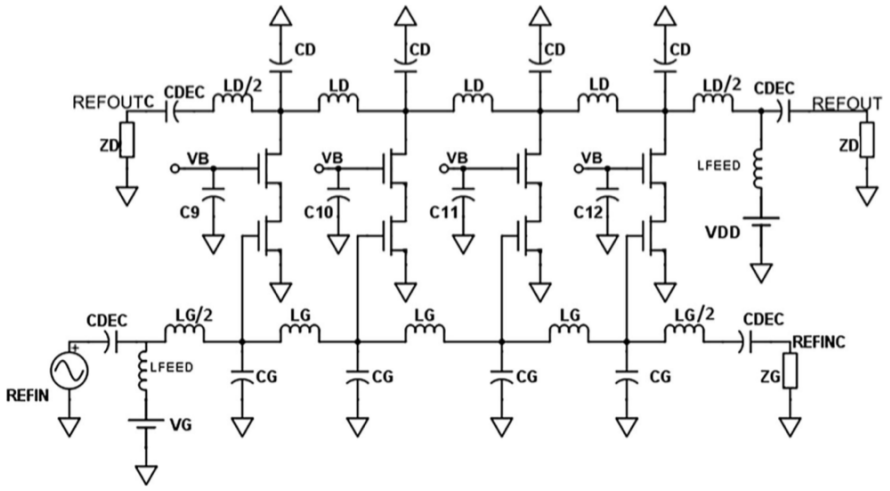


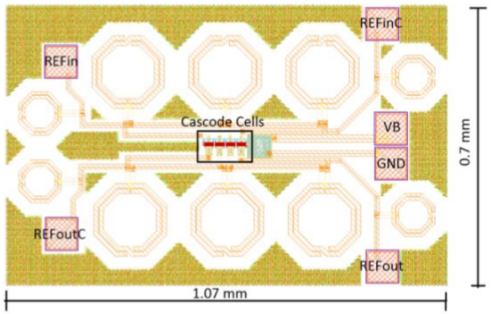

**Fig. 2** Architecture of a conventional four stages distributed amplifier

$$FOM_{\left[GHz/_{mW\cdot mm^2}\right]} = \frac{\alpha_{[dB]} \cdot BW_{[GHz]}}{NF_{[dB]} P_{DC[mW]} Area[mm^2]}$$

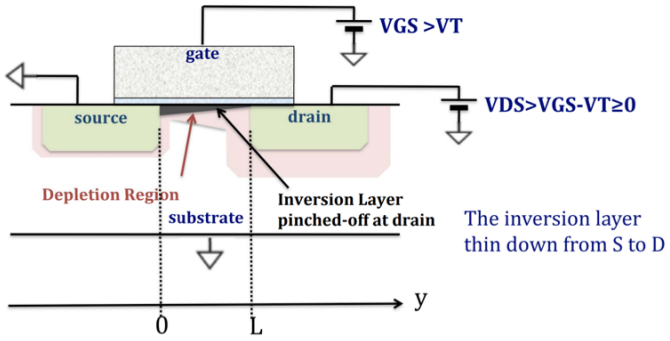
$$\alpha_{[dB]} = 10 \cdot \log_{10}\{|S_{21}|^2 \cdot [(1-|S_{11}|^2)\cdot(1-|S_{22}|^2)]\}$$

TABLE II. REPORTED PERFORMANCE OF CMOS DAS FOR UWB SYSTEMS

| *Reference* | *Technology* | *BW [GHz]* | *Gain [dB]* | *S11/S22 [dB]* | *NF average [dB]* | *Power [mW]* | *Area ($mm^2$)* | *FOM [GHz/mW·$mm^2$]* |
|---|---|---|---|---|---|---|---|---|
| [2] | 0.13 um CMOS | 3-9.4 | 12 | <-7 / <-8 | 3.3 | 30 | 0.82 | 0.28 |
| [8] (HG mode) | 0.13 um CMOS | 3-10 | 20.4 | <-10/<-10 | 3.29 | 37.8 | 0.88 | 1.26 |
| [8] (LG mode) | 0.13 um CMOS | 3-10 | 11 | <-10/<-10 | 4.25 | 6.86 | 0.88 | 1.71 |
| [9] | 0.13 um CMOS | 3-10 | 15 | <-12/<-15 | 3.34 | 26 | 0.43 | 2.89 |
| [10] | 0.13 um CMOS | 2.2-9 | 9.8 | <-10/<-9.2 | 4.25 | 30 | 0.68 | 0.28 |
| [11] | 0.18 um CMOS | 3-10 | 18 | <-10/<-9 | 6 | 54 | 2.2 | 0.15 |
| This Work | 0.13 um CMOS | 3-10 | 11 | <-16/<-18 | 2.65 | 26 | 0.75 | 1.61 |



# Motivation



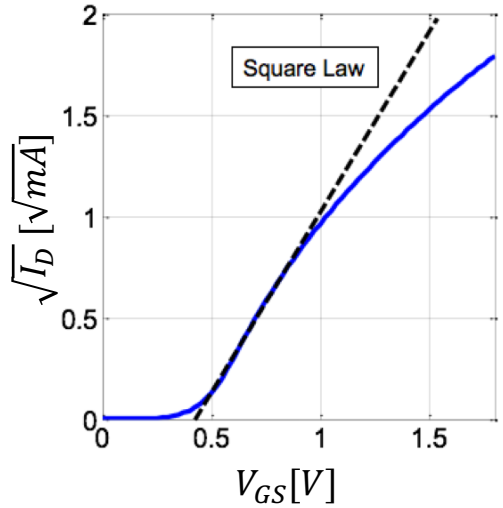

- The square-law MOS model is plagued by several limitations

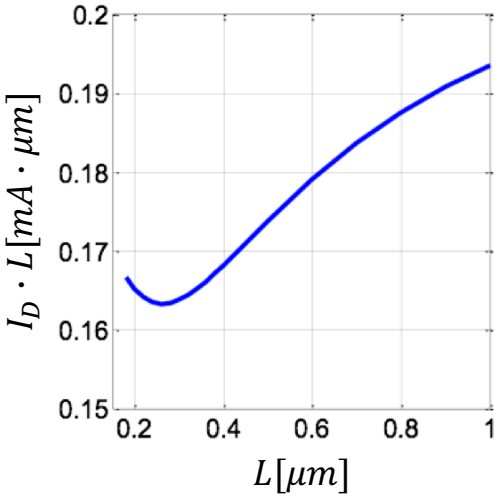
$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

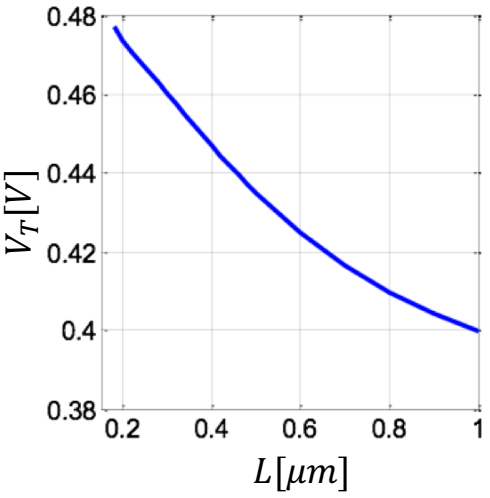
  - Modern MOSFETs are impaired by mobility degradation effects
  - In moderate inversion with gate overdrive voltages below 150mV, the square law model is grossly inaccurate
  - In weak inversion, the current flows by diffusion (like in a BJT) and the square-law model must be replaced with an exponential relationship

# Simulations (nMOS, 5 μm/0.18 μm, $V_{DS}$=1.8V)

- The transistor does not abruptly turn off at $V_T$
- The current is not perfectly quadratic with $V_{OV}$ (=$V_{GS}$–$V_T$)
- The current does not scale perfectly with 1/L
- The threshold voltage $V_T$ of the device changes with L



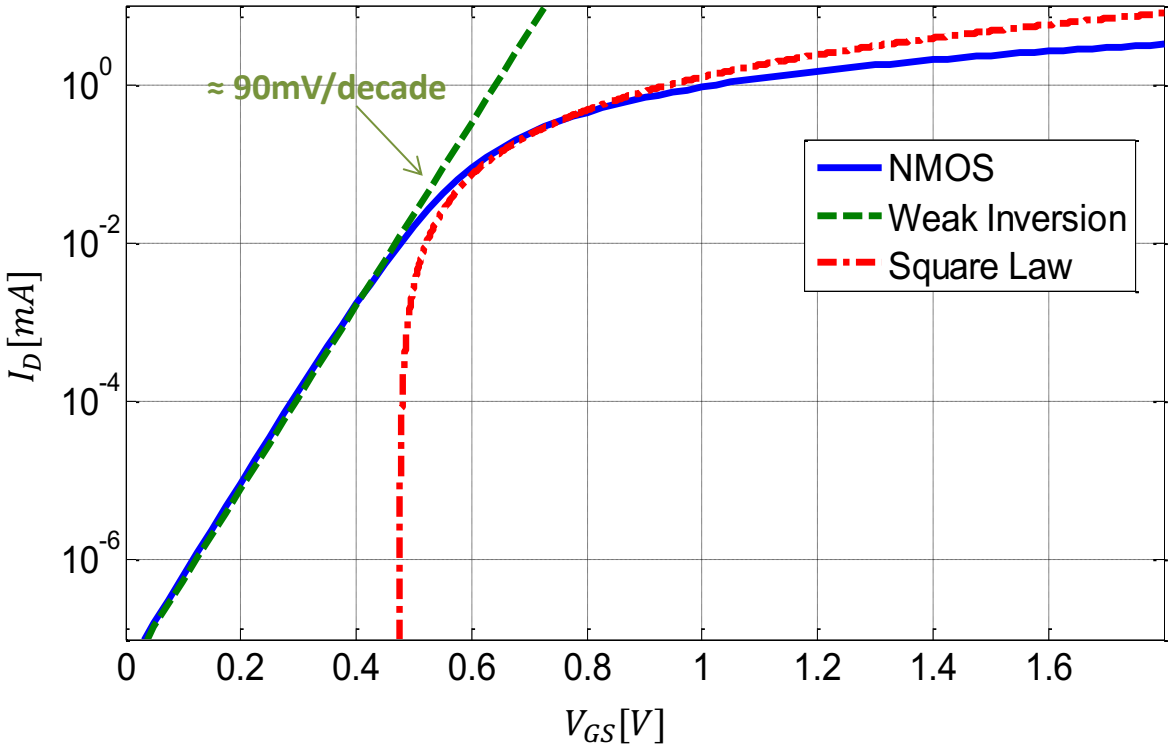



# The square law model fails miserably for low $V_{GS}$

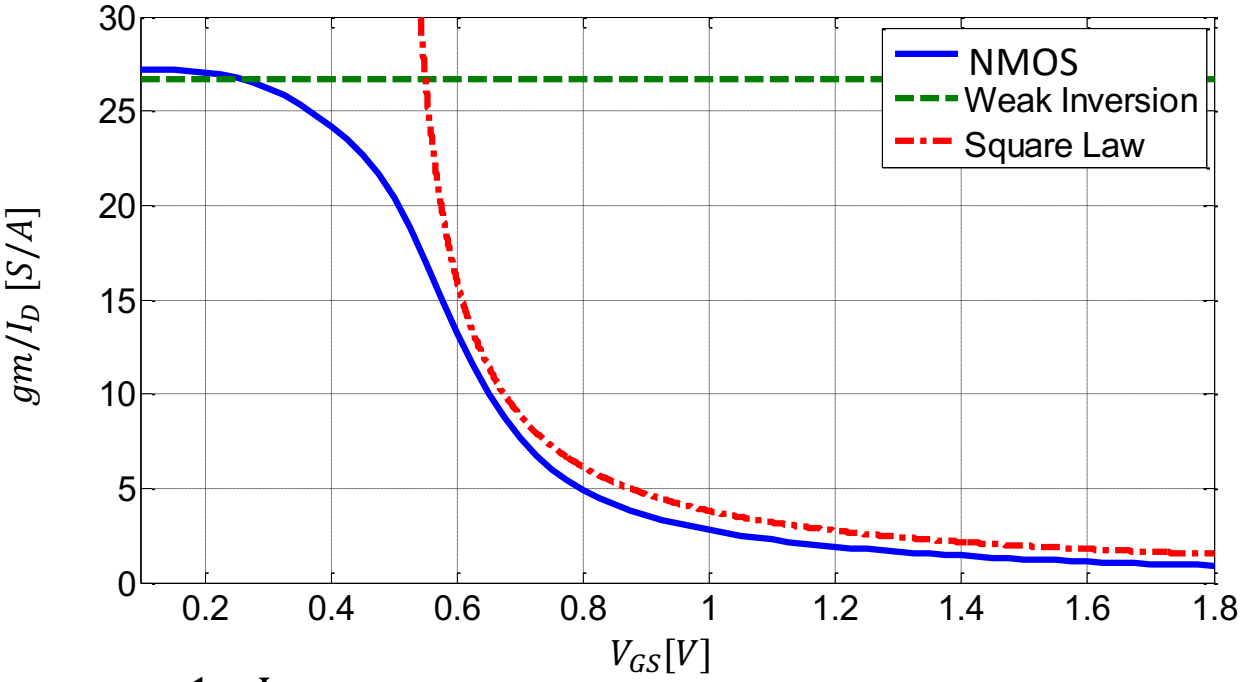
- The square law equation is adequate only for "strongly inverted" devices (that is for moderately-large $V_{OV}$)

*Currents on a Log Scale*



# A more design friendly perspective

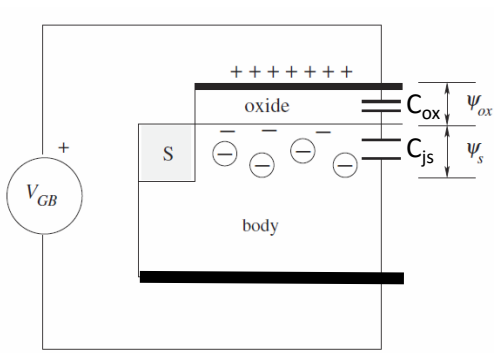
Transconductance Efficiency

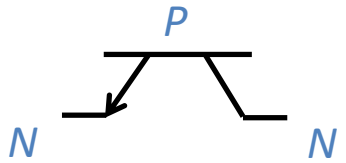



In weak inversion: $g_m = \frac{1}{n} \cdot \frac{I_D}{V_{th}}$

In moderate inversion: ???

In strong inversion: $g_m = \frac{2I_D}{V_{OV}}$

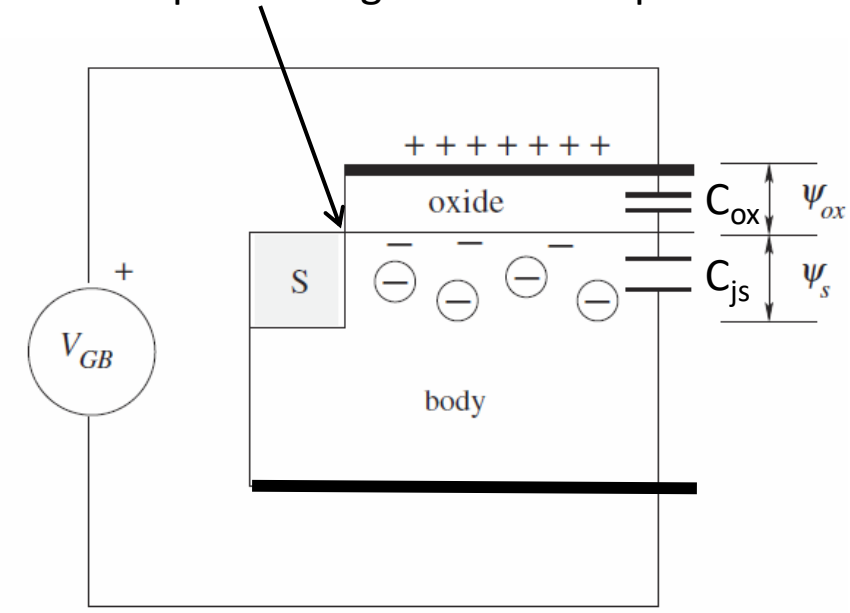


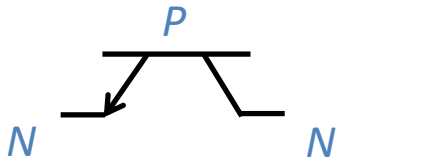
# Weak Inversion (Subthreshold) Operation

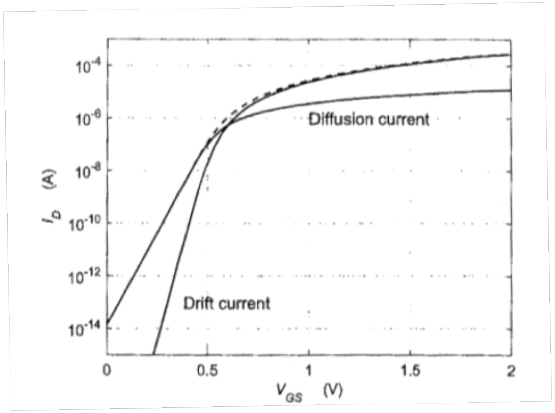
- Physics governed by a "gated diode" model
- The amount of electrons injected into a given point of the body depends on the potential present at that given point

Potential at this point is higher than the potential at any other body/source point



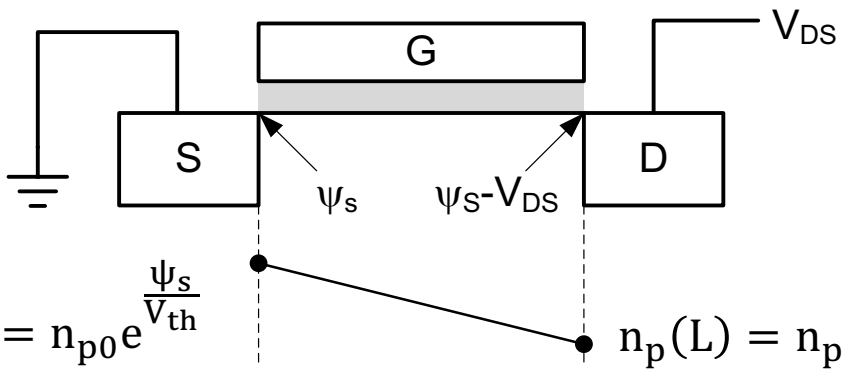

D.L. Pulfrey, Understanding Modern Transistors and Diodes, Cambridge University Press, 2010.




Total drain current dashed line

# Resulting Diffusion Current




$$I_D = qAD_n \frac{n_p(0) - n_p(L)}{L}$$

$$I_D = \frac{1}{L} qAD_n n_{p0} e^{\frac{\psi_s}{V_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)$$

- The current grows exponentially with $\psi_s$
- The current becomes independent of $V_{DS}$ for $V_{DS} > 3V_{th}$ (78mV)

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# Capacitive Divider

$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_{js} + C_{ox}} = \frac{1}{n}$$

- n is called “subthreshold factor” or “nonideality factor”
- n ≅ 1.45 for an NMOS device in our technology
- After including this relationship between $\psi_s$ and $V_{GS}$ and after a few additional manipulations, the final expression for the drain current becomes:

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}-V_t}{nV_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)$$

where $I_{D0}$ depends on technology ($I_{D0} \cong 0.43\mu A$ for an NMOS device in our technology)

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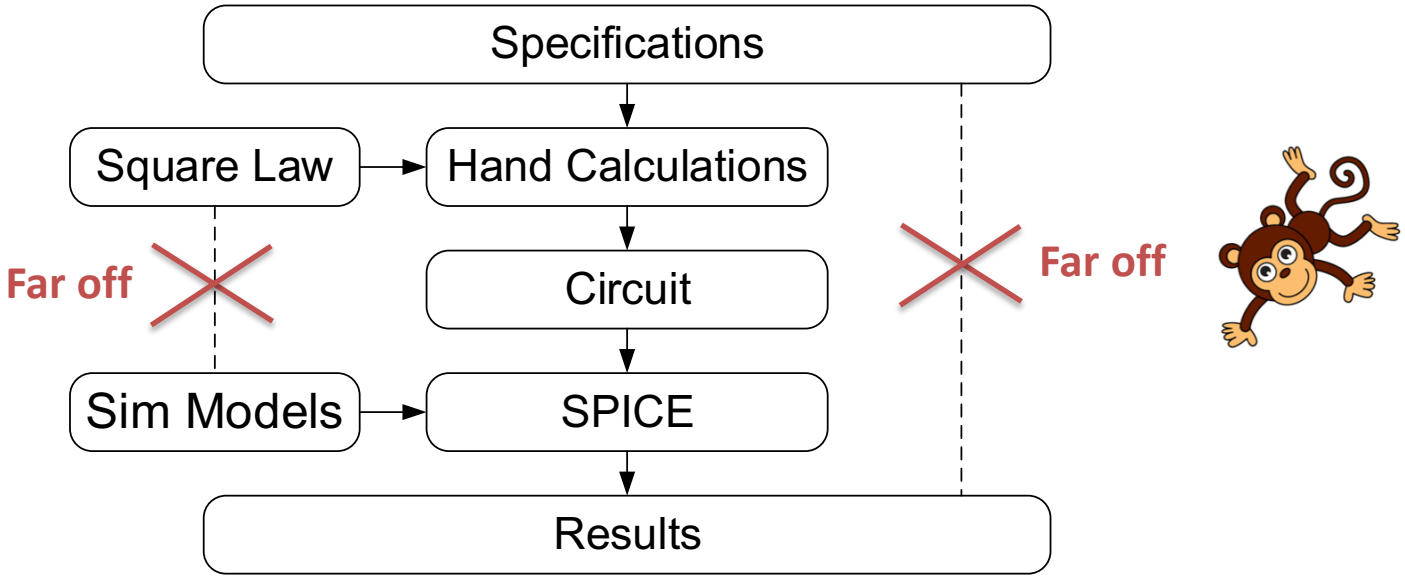
# In summary …

- Modern MOSFETs are complicated !
- The behavior of a MOS in saturation can be roughly categorized according to the channel's inversion level: weak, moderate and strong inversion
- The bottom line is that there is no modeling expression that is simple enough for hand analysis and sufficiently accurate to match real world device behavior

# Typical Analog circuits design flow based on square law hand calculations and SPICE simulation




- The complexity of the transistor model preclude the derivation of simple closed form analytical expressions
- Design process takes multiple iterations and “hand” tweaking of the transistor sizing before converging toward a working circuit

# Technology centric vs. Design centric FOMs

- Most of the he parameters in the square-law model are technology centric

$$I_D = \frac{1}{2}\boldsymbol{\mu C_{ox}}\frac{W}{L}(V_{OV})^2(1+\boldsymbol{\lambda} V_{DS})$$

$$V_{OV} \therefore V_{GS} - \boldsymbol{V_T}$$

- It is hard to link technology parameters to the design requirements (gain, bandwidth, input and output impedances, noise)

# By the way what are $\mu C_{ox}$, lambda and $V_T$ for our technology ?

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```
* 0.18um CMOS models (nominal process)
.MODEL nmos nmos (
+acm     = 3              hdif    = 0.32e-6        LEVEL   = 49
+ CAPOP = 39
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3618397
+K1      = 0.5916053      K2      = 3.225139E-3    K3      = 1E-3
+K3B     = 2.3938862      W0      = 1E-7           NLX     = 1.776268E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.3127368      DVT1    = 0.3876801      DVT2    = 0.0238708
+U0      = 256.74093      UA      = -1.585658E-9   UB      = 2.528203E-18
+UC      = 5.182125E-11   VSAT    = 1.003268E5     A0      = 1.981392
+AGS     = 0.4347252      B0      = 4.989266E-7    B1      = 5E-6
+KETA    = -9.888408E-3   A1      = 6.164533E-4    A2      = 0.9388917
+PRWG    = 0.5            PRWB    = -0.2
+WR      = 1              WINT    = 0              LINT    = 1.617316E-8
+XL      = 0              XW      = -1E-8          DWG     = -5.383413E-9
+DWB     = 9.111767E-9    VOFF    = -0.0854824     NFACTOR = 2.2420572
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.981159E-3    ETAB    = 9.289544E-6
+DSUB    = 0.0159753      PCLM    = 0.7245546      PDIBLC1 = 0.1568183
+PDIBLC2 = 2.543351E-3    PDIBLCB = -0.1           DROUT   = 0.7445011
+PSCBE1  = 8E10           PSCBE2  = 1.876443E-9    PVAG    = 7.200284E-3
+DELTA   = 0.01           MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 1
+CGDO    = 4.91E-10       CGSO    = 4.91E-10       CGBO    = 1E-12
+CJ      = 9.652028E-4    PB      = 0.8            MJ      = 0.3836899
+CJSW    = 2.326465E-10   PBSW    = 0.8            MJSW    = 0.1253131
+CF      = 0              PVTH0   = -7.714081E-4   PRDSW   = -2.5827257
+PK2     = 9.619963E-4    WKETA   = -1.060423E-4   LKETA   = -5.373522E-3
+PU0     = 4.5760891      PUA     = 1.469028E-14   PUB     = 1.783193E-23
+PVSAT   = 1.19774E3      PETA0   = 9.968409E-5    PKETA   = -2.51194E-3
+nlev    = 3              kf      = 0.5e-25)
```

This is a 110-parameter BSIM3v3 SPICE model: $\mu$Cox $\triangleq$ KP and lambda are nowhere to be found

# Transistor Figures of Merit for Design

- Transconductance efficiency
  - Want large $g_m$, for as little current as possible

$$\frac{g_m}{I_D}$$

**Square Law**

$$= \frac{2}{V_{OV}}$$

- Transit frequency
  - Want large $g_m$, without large $C_{gg}$

$$\frac{g_m}{C_{gg}}$$

$$\cong \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

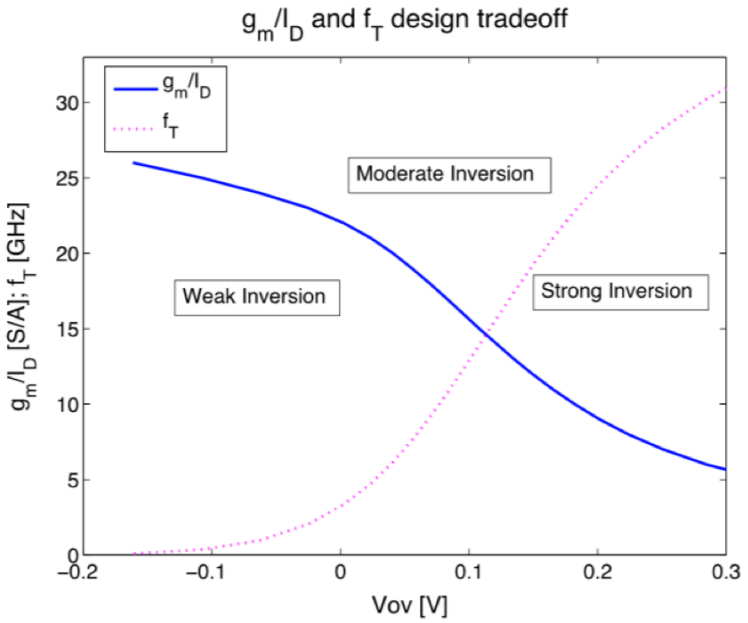
- Intrinsic gain
  - Want large $g_m$, but no $g_{ds}$

$$\frac{g_m}{g_{ds}}$$

$$\cong \frac{2}{\lambda V_{OV}}$$

# Design Tradeoffs

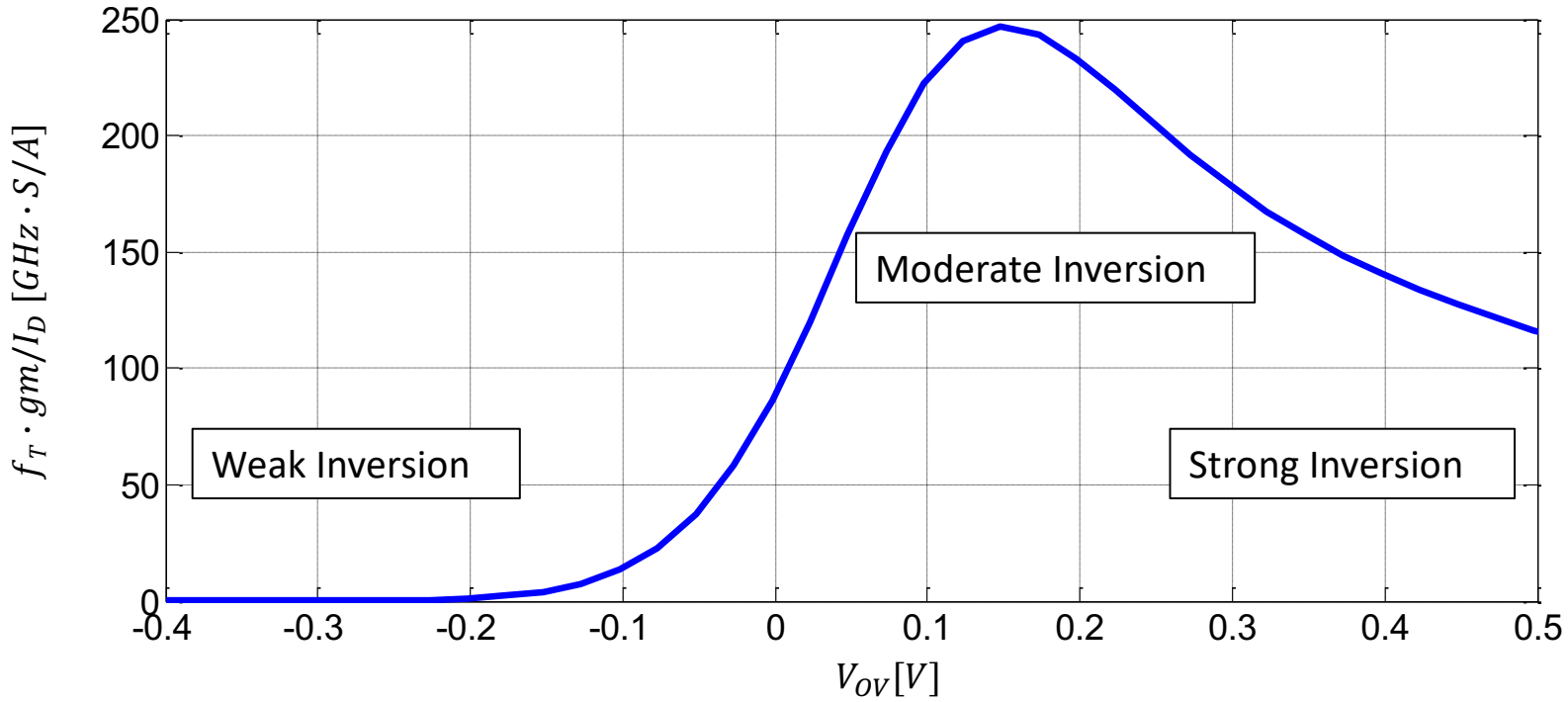
Plot of $g_m/I_D$ and $f_T$ at different levels of inversion Vov for an nMOS transistor with channel length $L = 0.18\ \mu m$




| Transconductance efficiency | |
|---|---|
| Low $g_m/I_D$ | High $g_m/I_D$ |
| Strong inversion | Weak inversion |
| Poor power efficiency | Good power efficiency |
| Low output voltage range | High output voltage range |
| High transient frequency | Low transient frequency |
| Small transistor | Large transistor |

**Table 1** Transistor's properties at different levels of transconductance efficiency

# Product of $g_m/I_D$ and $f_T$




- Interestingly, the product of $g_m/I_D$ and $f_T$ peaks in moderate inversion
  - For our 0.18 μm technology it peaks at around $g_m/I_D \approx 13$ S/A
- Operating the transistor in moderate inversion makes sense when we value speed and power efficiency equally
  - Not always the case, it depends on the application

# Product of $g_m/I_D$ and $f_T$ for varying L

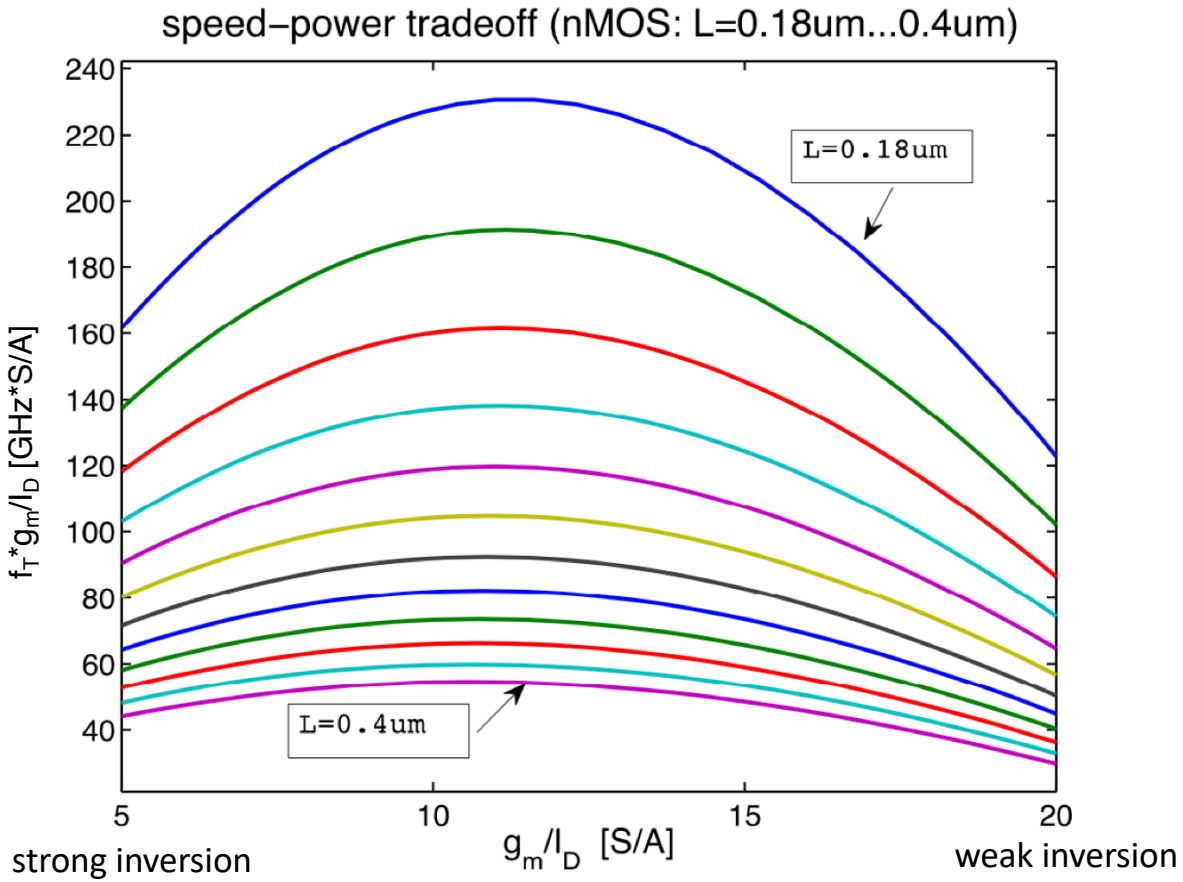



**Fig. 1** Relationship between $f_T g_m/I_D$ and $g_m/I_D$ for nMOS transistors with channel length $L$ varying from 0.18 to 0.4 μm

# Systematic Design of Analog CMOS Circuits Using $g_m/I_D$-based Methodology

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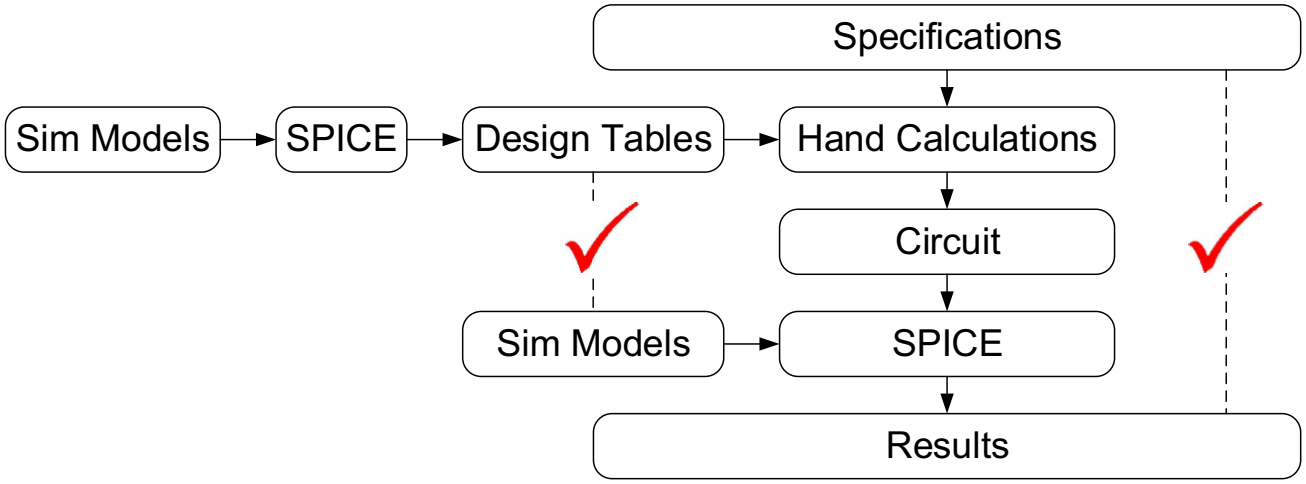
- Goal
  - Maintain a systematic design methodology in the absence of a set of useful compact MOS equations
- Strategy
  - Design using look-up tables or charts




- Use pre-computed SPICE data in hand calculations

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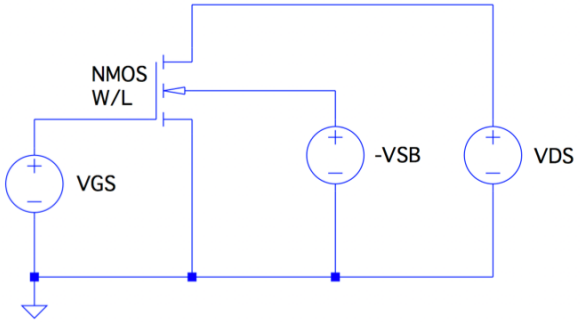
# Starting Point: $g_m/I_D$-Centric Technology Characterization

- Tabulate the figures of merit considering $g_m/I_D$ as an index, over a reasonable range of $g_m/I_D$ and channel lengths
  - Transit frequency ($f_T$)
  - Intrinsic gain ($g_m/g_{ds}$)
- Also tabulate relative estimates of capacitances
  $C_{gd}/C_{gg}$ and $C_{dd}/C_{gg}$
- Note, that all the FOMs are (to first order) independent of device width
- So, in order to compute device widths, we need one more table that links $g_m/I_D$ and current density $I_D/W$

# $g_m/I_D$-Centric Technology Characterization

- Obtain tables of device characteristics through a DC sweep of the transistor
  - Measure transistor .op parameters at each point of the sweep
    - $g_m$, $I_D$, $C_{gg}$, $g_{ds}$, etc.
  - Repeat the sweep for different lengths
    - 180nm, 200nm, ….. 3µm
- Simple version: sweep $V_{GS}$ with $V_{DS}$ held fixed at $V_{DS} = V_{DD}/2$
  - The figures of merit and $I_D/W$ don't vary too much with $V_{DS}$
- Advanced version: sweep also $V_{DS}$ and $V_{BS}$
  - Captures the back-gate effect due to $V_{BS}$
    - Threshold Voltage shift
  - Often using "low/medium/high" $V_{DS}$ charts is good enough



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# Simulation Data in MATLAB

```
% data stored in /home/ee406/matlab
>> load 180nch.mat
>> nch
nch =
        ID: [4-D double]
        VT: [4-D double]
        GM: [4-D double]
       GMB: [4-D double]
       GDS: [4-D double]
       CGG: [4-D double]
       CGS: [4-D double]
       CGD: [4-D double]
       CGB: [4-D double]
       CDD: [4-D double]
       CSS: [4-D double]
      INFO: 'GU ee406 models, 180nm CMOS, BSIM3'
       VGS: [73x1 double]
       VDS: [73x1 double]
       VSB: [11x1 double]
         L: [32x1 double]
         W: 5.0000e-06
     NFING: 1
>> size(nch.ID)
ans =
    32    73    73    11
```

Four-dimensional arrays

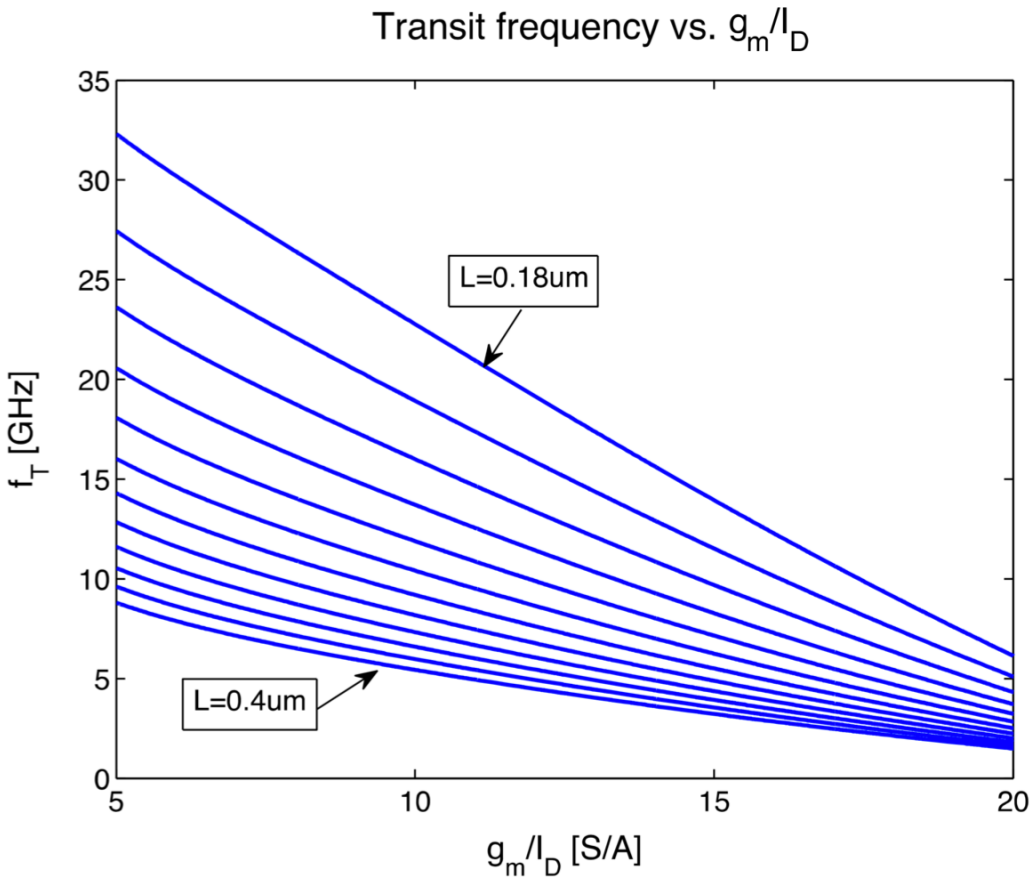
$$I_D(L, V_{GS}, V_{DS}, V_S)$$

$$V_t(L, V_{GS}, V_{DS}, V_S)$$

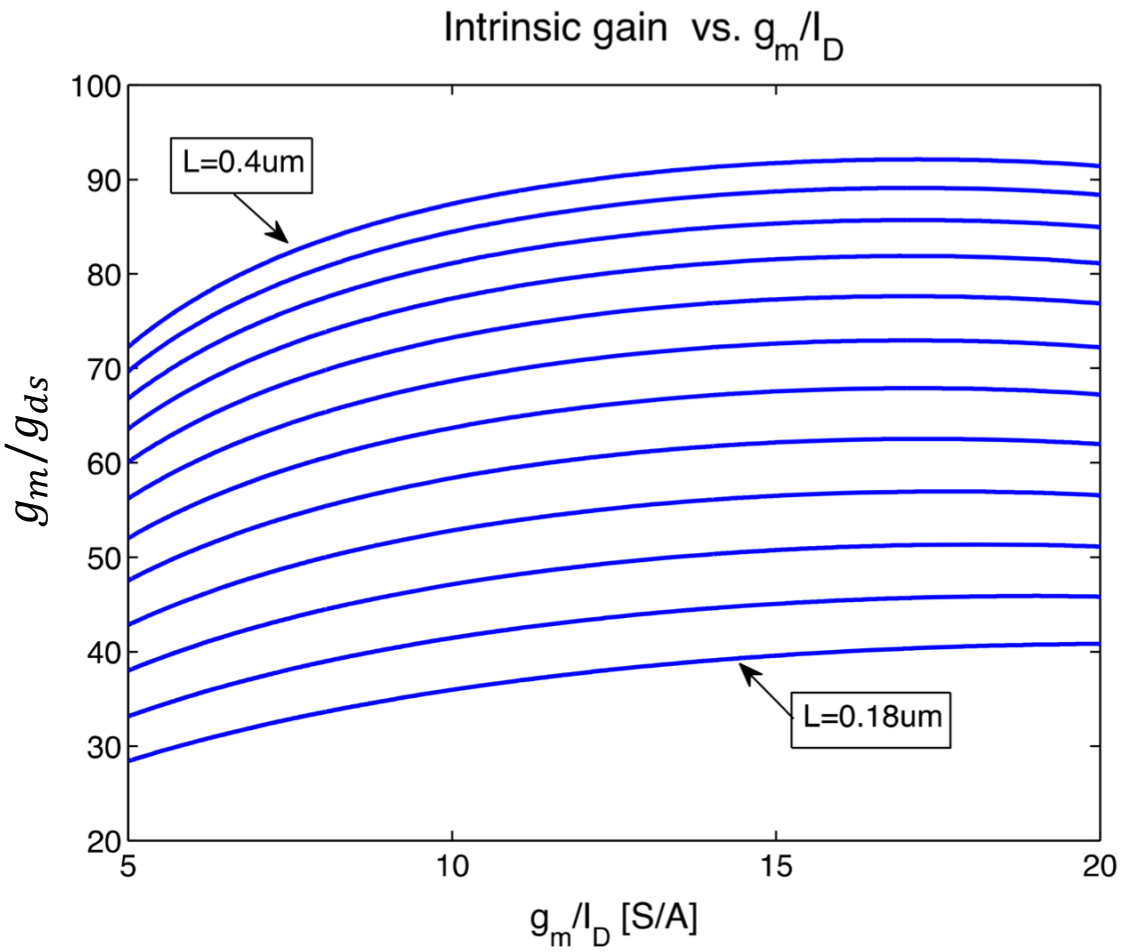
$$g_m(L, V_{GS}, V_{DS}, V_S)$$

...

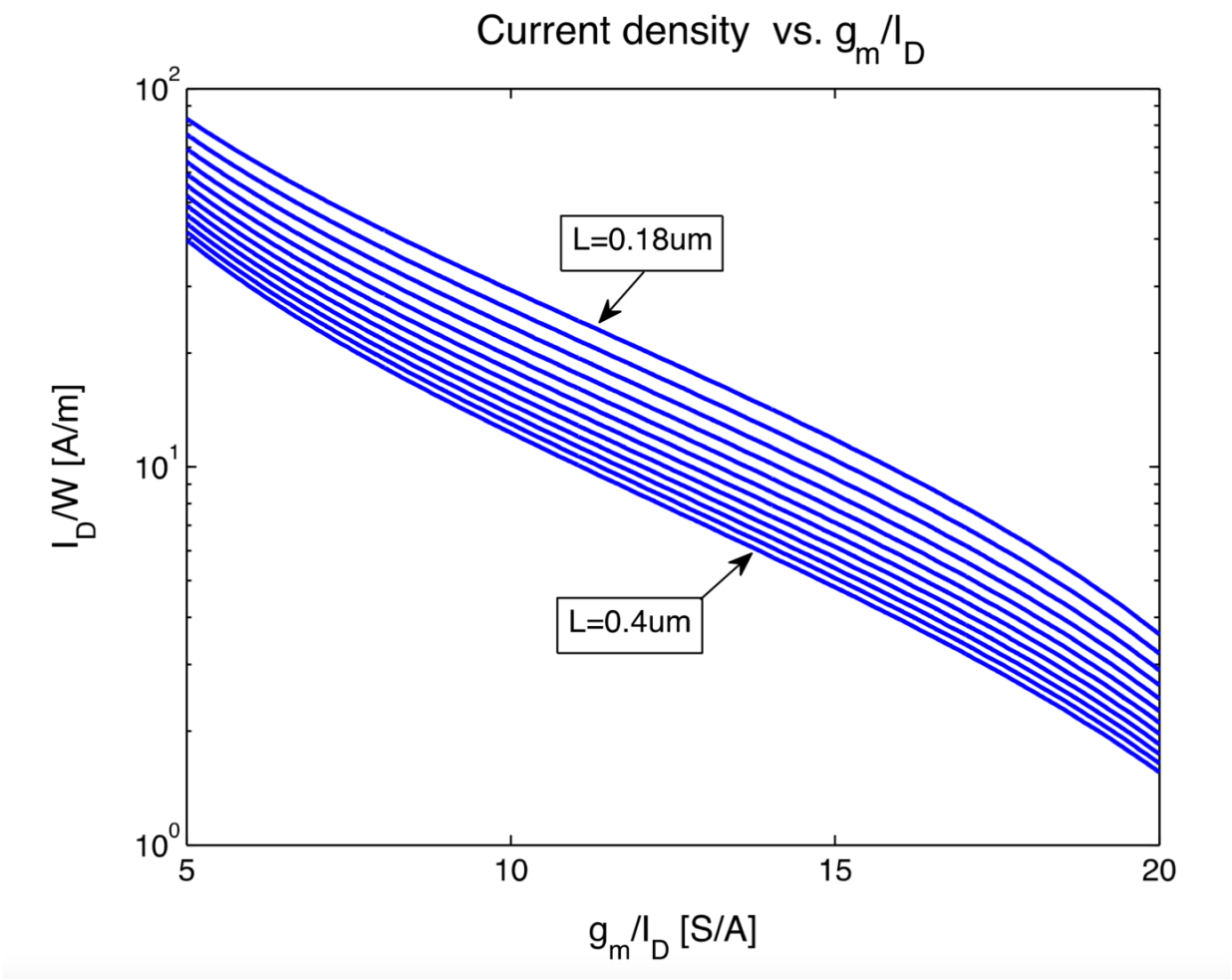
# Transit Frequency ($f_T=g_m/C_{gg}$)



# Intrinsic Gain ($g_m/g_{ds}$)



# Current Density ($J_D=I_D/W$)



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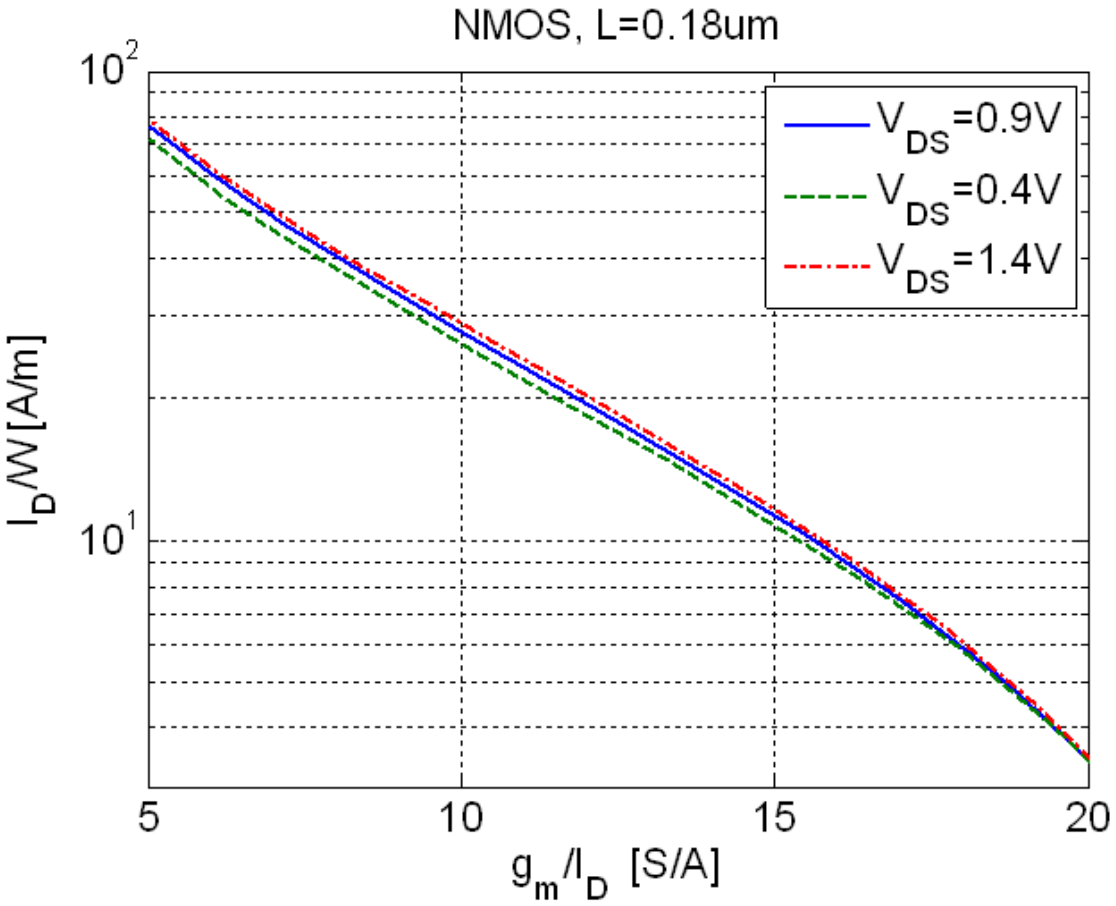
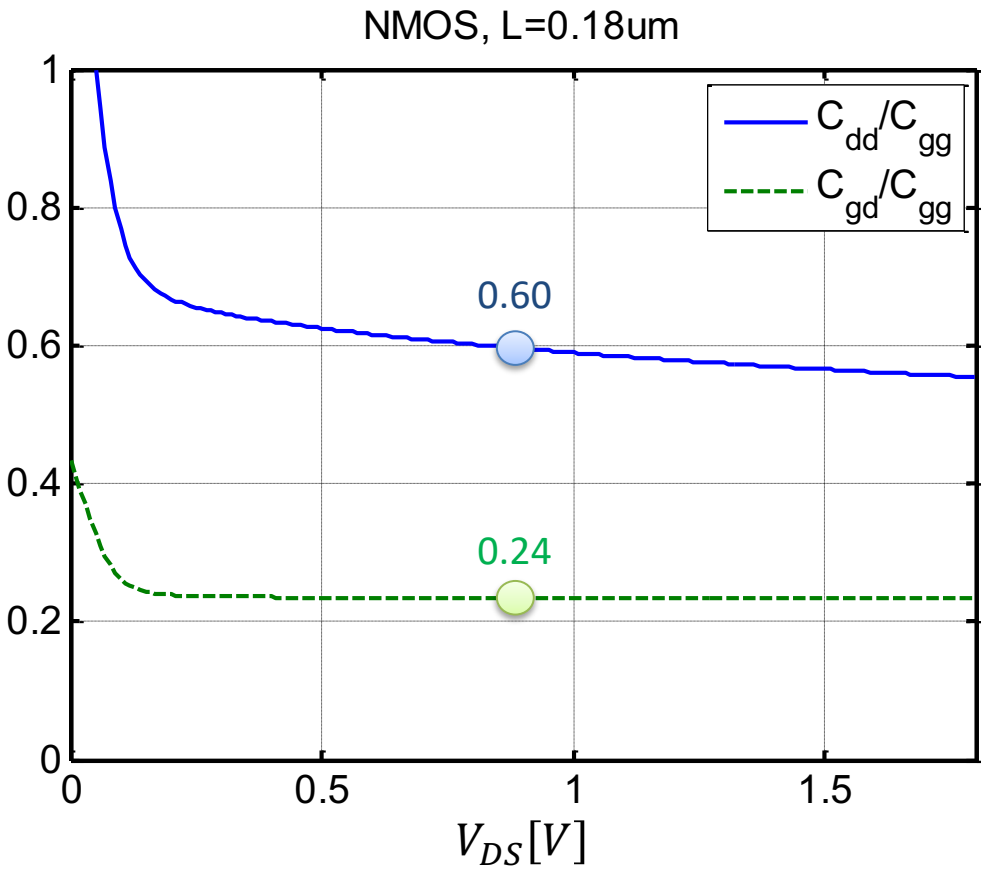
# $V_{DS}$ Dependence




- $V_{DS}$ dependence is relatively weak
- Typically it is OK to work with data generated for $V_{DD}/2$

# Capacitances



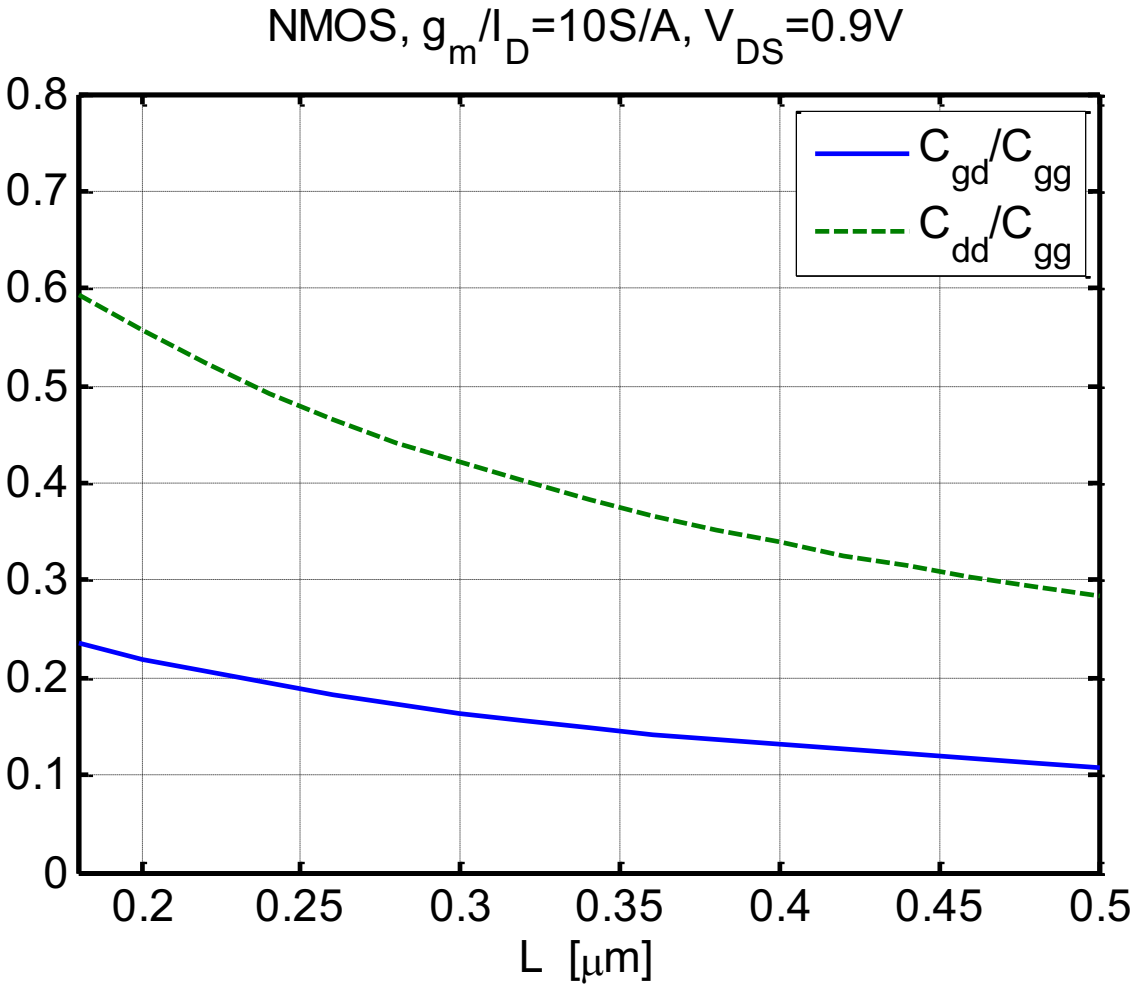

- Again, it's usually OK to work with estimates taken at $V_{DS}=V_{DD}/2$

$$C_{gg} = C_{gs} + C_{gd} + C_{gb}$$

$$C_{dd} = C_{gd} + C_{db}$$

$$C_{ss} = C_{gs} + C_{sb}$$

# Capacitances – Length Dependence



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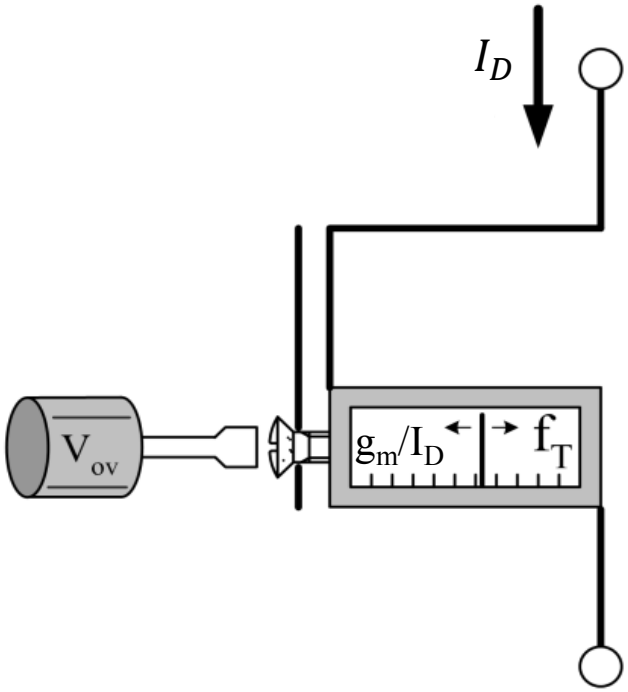
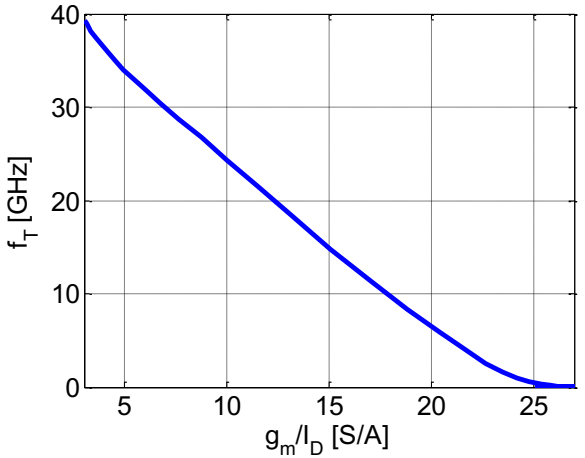
# Design in a Nutshell



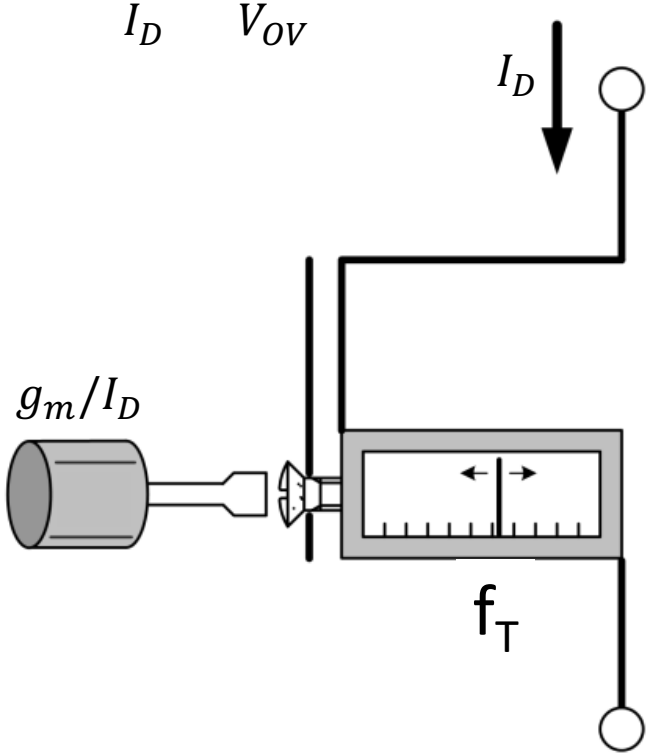




- Choose length L such that the circuit has 'enough' gain
- Choose the inversion level according to the proper tradeoff between speed ($f_T$) and transconductance efficiency ($g_m/I_D$) for the given circuit
- The inversion level is fully determined by the gate overdrive $V_{OV}$
  - But, $V_{OV}$ is not a very interesting parameter outside the square law framework; not much can be computed from $V_{OV}$

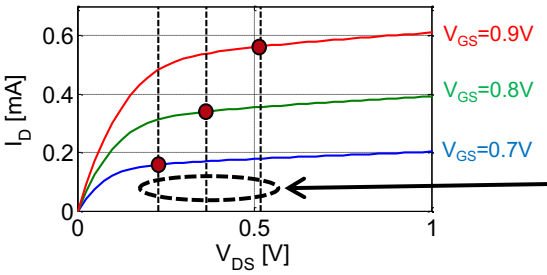
# Eliminating $V_{OV}$

- But, … the inversion level is also fully defined by $g_m/I_D$ so there is no need to know $V_{OV}$

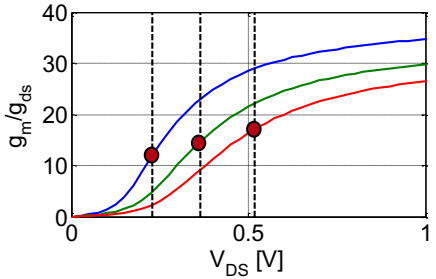
$$\frac{g_m}{I_D} = \frac{2}{V_{OV}}$$




**Reality Check**




computed as $2/(g_m/I_D)$ values




The SPICE model data confirms that $2/(g_m/I_D)$ is a good estimate for the minimum reasonable $V_{DS}$

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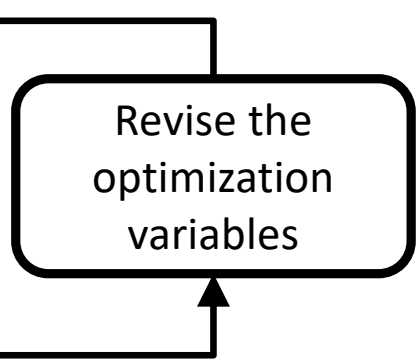
# A Generic Design Optimization Flow

Complicated circuits have *many* degrees of freedom and objectives

- Usually we must make some heuristic choices up front
- Charts and lookup tables help you iterate through possible designs rapidly

1) Pick transistor lengths
2) Pick $g_m/I_D$ bias points
3) Determine gm (from design objective)
4) Determine bias currents (from $g_m$ and $g_m/I_D$)
5) Total power consumption = ???
   - Room for improvement?
   - Ready to verify?




6) Determine W (from $I_D/W$)
7) Simulate the circuit: meets specs and estimated performance?
   - If yes, then you're done!
   - If not, revise the design flow: correct mistakes, improve estimates, etc.

# TIA for Fiber Optic Receiver

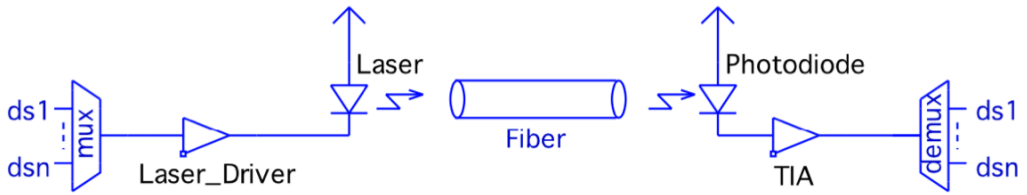



**Fig. 2** Typical optical communication (OC) system

TIA specifications:

- 0.18µm CMOS technology,
- closed-loop transimpedance gain of 73 dBΩ
- 0.5 pF photodiode
- 250 Ω-load,
- Total current budget up to 16mA
- input referred current noise PSD up to $160 \times 10^{-24}$ $A^2/Hz$
- Optimize for gain, speed and power consumption

$$\text{FOM} = \frac{\text{GBW}}{P_{\text{DISS}}}$$

| Performance metric | Analysis | Simulation | \|% Relative error\| |
|---|---|---|---|
| Gain (dBΩ) | 73.06 | 78.34 | 6.74 |
| $f$3 db (GHz) | 2.4 | 2.21 | 8.6 |
| Input ref. noise (pA/$\sqrt{}$Hz) | 11.99 | 11.91 | 0.67 |
| Power dissipated (mW) | 14.40 | 13.5 | 6.67 |
| Phase margin (degrees) | 47.48 | 45.19 | 5.07 |

# TIA for Fiber Optic Receiver

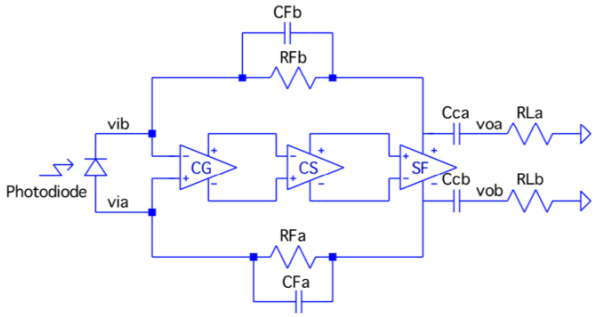



**Fig. 4** TIA topology (CG = common gate, CS = common source, SF = source follower)

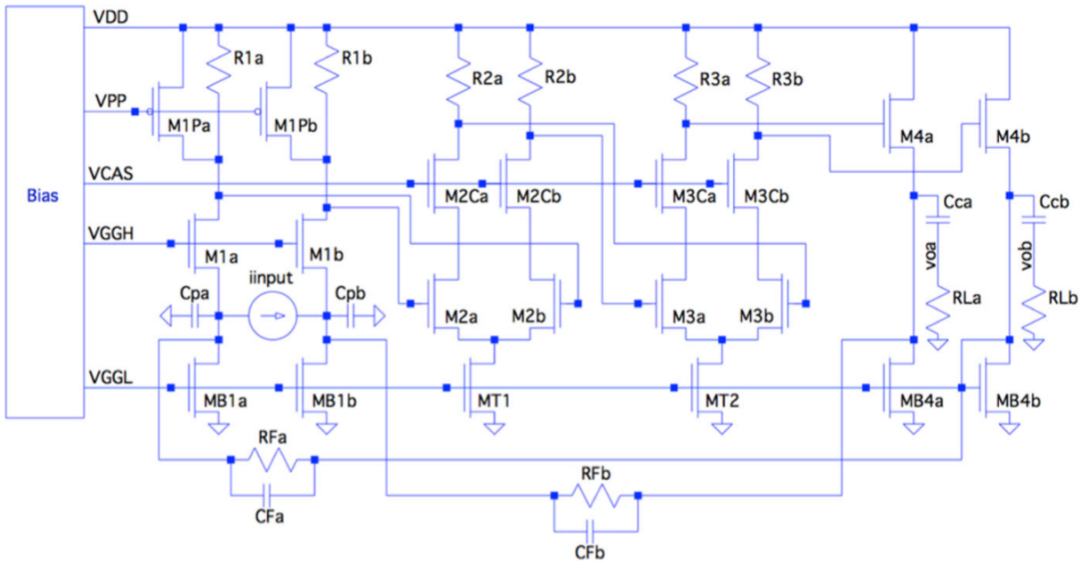
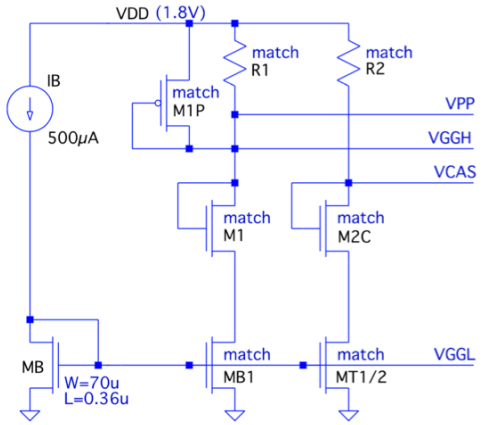



**Fig. 5** TIA schematic

**Fig. 6** TIA's biasing circuit



# TIA for Fiber Optic Receiver

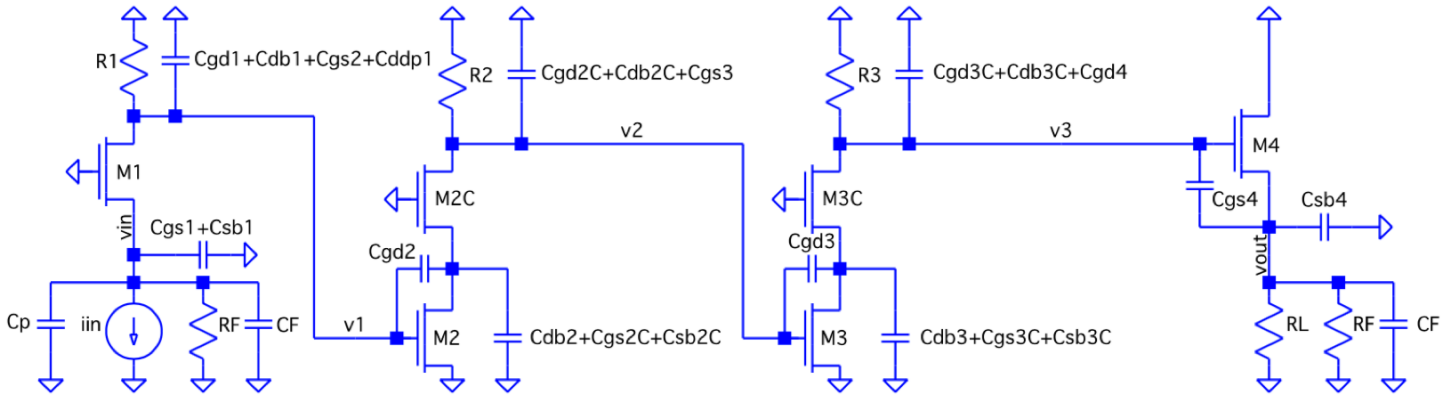



**Fig. 7** TIA AC half circuit with feedback loading and relevant capacitances

*Loop gain:* $T_0 = a_0 f_0$

*Closed Loop Trans-impedance gain:* $A_0 = \dfrac{v_{\text{out,diff}}}{i_{\text{input}}} \approx \dfrac{2a_0}{1+T_0}$ $\quad i_{\text{input}} = i_{\text{in}}/2$ and $v_{\text{out,diff}} = v_{\text{oa}} - v_{\text{ob}}$

*Bandwidth (ZVTC):* $f_{-3\,\text{dB}} \approx \dfrac{1+T_0}{2\pi \cdot \sum_{\forall i} \tau_i}$

*Input referred current noise PSD:* $\dfrac{\overline{i^2_{\text{noise}}}}{\Delta f} \approx \dfrac{1}{2} \cdot \left( \dfrac{4KT}{R_{\text{F}}} + 4KT\gamma_n g_{\text{mB1}} + \dfrac{4KTR_1}{A^2_{\text{CG}}} + 4KT\gamma_p g_{\text{m1P}} \dfrac{R_1^2}{A^2_{\text{CG}}} \right)$

# TIA for Fiber Optic Receiver

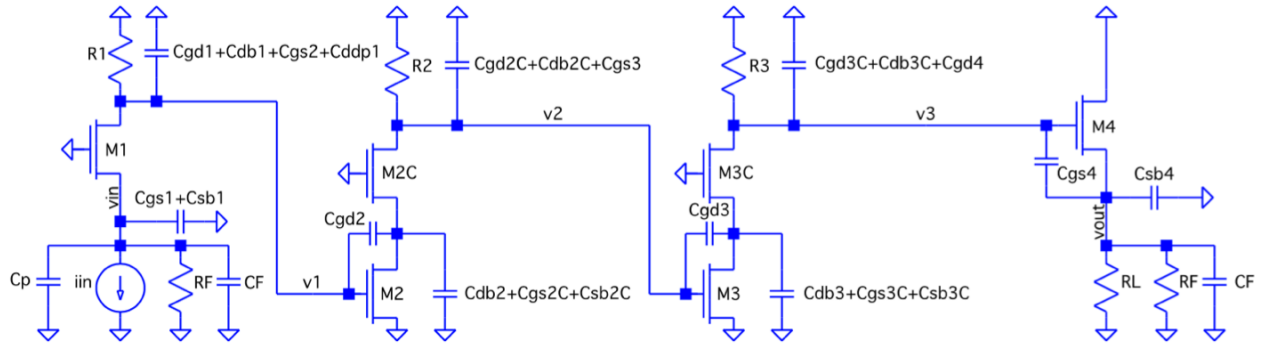



**Fig. 7** TIA AC half circuit with feedback loading and relevant capacitances

*TC at the CG input:* $\tau_{in} \approx C_{in} \cdot \left( R_F || \frac{1}{g^*_{m1}} \right)$ where $C_{in} = C_P + C_F + C_{gs1} + C_{sb1} + C_{ddp1}$ and $C_{ddp1} = C_{gdp1} + C_{dbp1}$

*TC at the CG output:* $\tau_2 \approx R_1 C_2$ where $C_2 = C_{gd1} + C_{db1} + C_{gs2} + C_{gd2}(1 + g_{m2}/g^*_{m2C})$

*TC at the source of M2C:* $\tau_{2C} \approx \frac{1}{g^*_{m2C}} C_{2C}$ where $C_{2C} = C_{db2} + C_{gs2C} + C_{sb2C}$

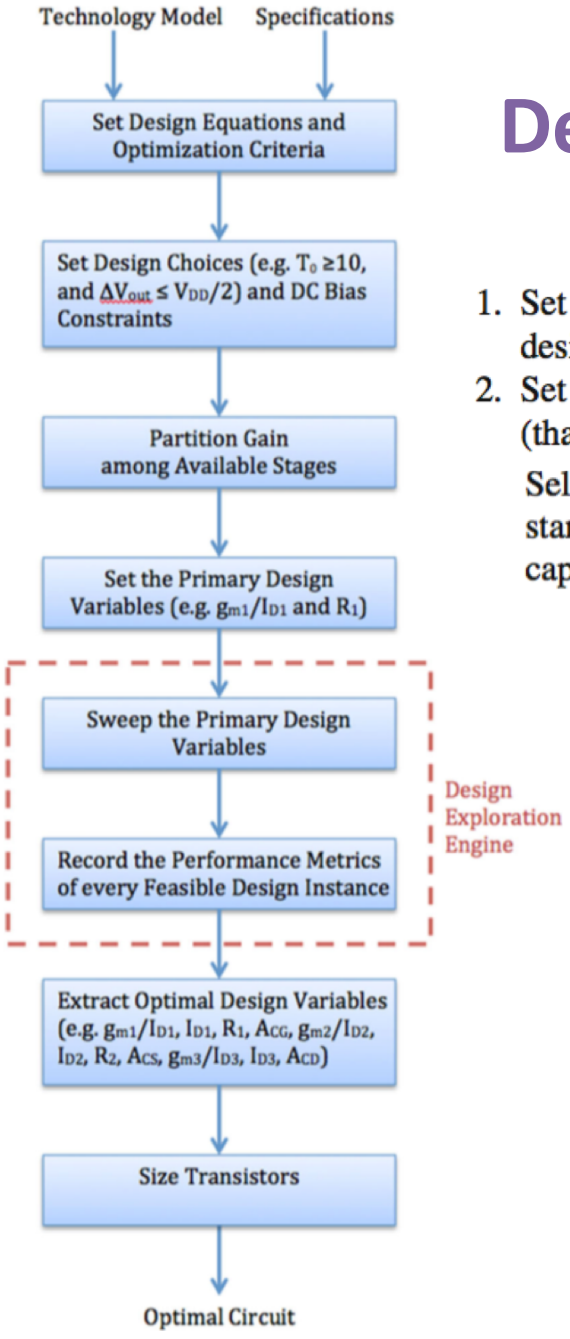
*TCs at the first CS output:* $\tau_3 \approx R_2 C_3$ and $\tau_{3m} \approx C_{gd3} \cdot \left( R_2 + \frac{1}{g^*_{m3C}} + g_{m3} \frac{R_2}{g^*_{m3C}} \right)$

*TC at the source of M3C:* $\tau_{3C} \approx \frac{1}{g^*_{m3C}} C_{3C}$ where $C_{3C} = C_{db3} + C_{gs3} + C_{sb3C}$

*TC at the CD input:* $\tau_{4in} \approx R_2 C_{4in}$ and $\tau_{4m} \approx C_{gs4} \frac{R_3 + R_{Lp}}{g_{m4} R_{Lp} + 1}$ where $C_{4in} = C_{db2C} + C_{gd2C} + C_{gs3}$

*TC at the CD output:* $\tau_{4out} \approx R_{Lp} \cdot (C_F + C_{sb4})$

# Design Optimization Framework




1. Set the loop gain $T_0$ to an appropriate value ($T_0 \geq 10$) and derive $R_F$ based on the design objectives ($A_0 \geq 73$ dBΩ).
2. Set $g_m/I_D$ for the transistor $M_4$ (source follower) to allow max output signal swing (that is $V_{IN4} = V_{DD}/2$) and compute the corresponding transient frequency $f_T$. Select an appropriate value of bias current based on $C_{gg4}$ such that the time constants associated with the source follower are not dominant. Estimate the parasitic capacitances and compute the resulting gain $A_{CD}$ of the source follower.

$$C_{gg4} = \frac{g_{m4}}{2\pi f_{T4}}$$

$$I_{D4} = \frac{g_{m4}}{g_{m4}/I_{D4}}$$

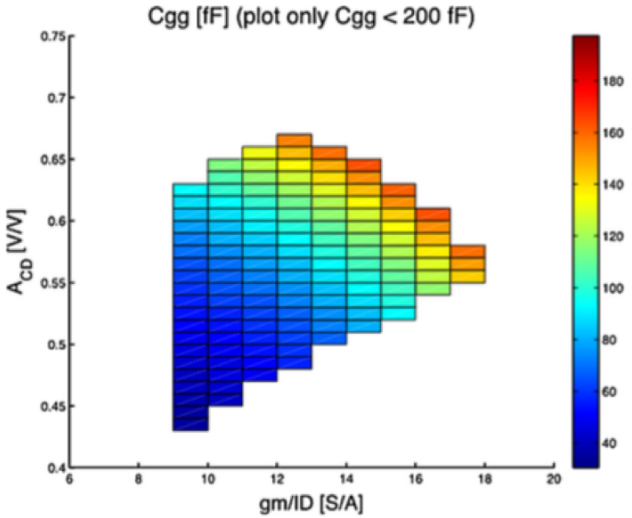
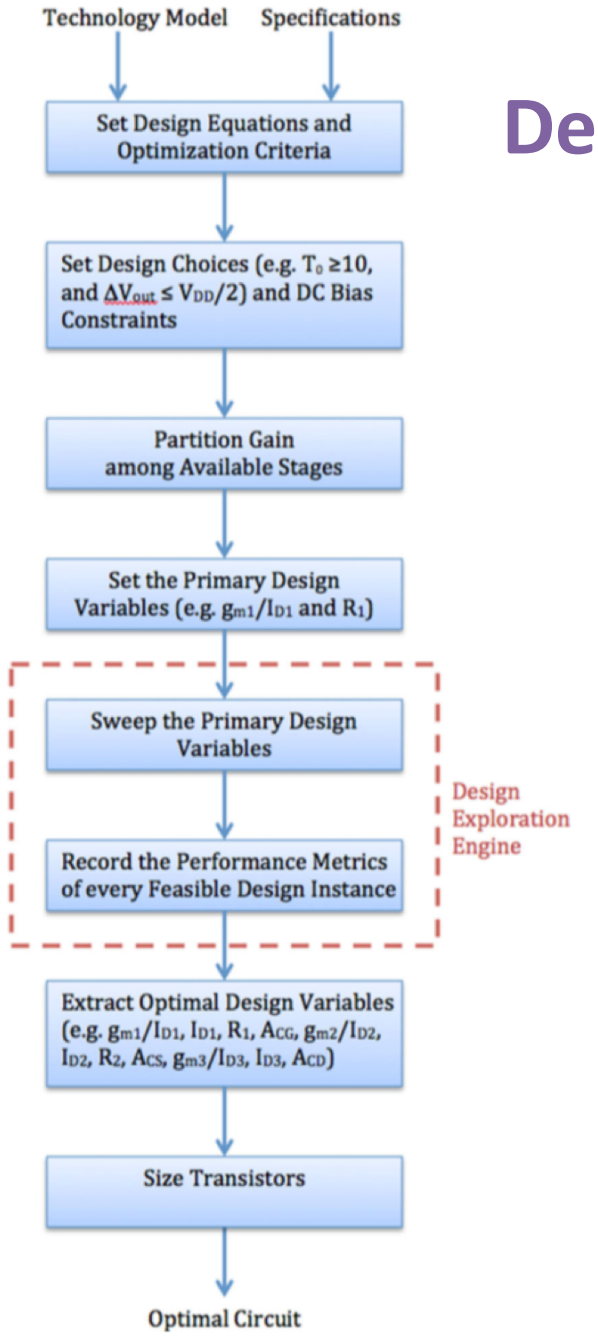



**Fig. 10** Source follower design optimization: $C_{gg}$ capacitance versus $g_m/I_D$ and gain $A_{CD}$




# Design Optimization Framework

3. Partition the amount of gain needed to meet specification between the common source and the common gate:

$$A_{CS}A_{CG} = \frac{a_0}{A_{CD}} \tag{16}$$

An excessive value of $A_{CS}$ causes a strong miller effect at the intermediate node between the transistors $M_2$ and $M_{2C}$ and results in a non optimal value of the dominant time constant $\tau_2$. Similarly, an excessive value of $A_{CG}$ implies an excessive value of $R_1$ and results in a suboptimal value of the dominant time constant $\tau_2$. Appropriate values of $A_{CS}$ and $A_{CG}$ are in the following ranges:

$$1 \leq A_{CS} \leq 50 \text{ and } \frac{a_0}{A_{CD}A_{CSmax}} \leq A_{CG} \leq \frac{a_0}{A_{CD}} \tag{17}$$

4. Set $g_m/I_D$ of transistor $M_1$ and the value of $R_1$ as the primary design variables. The values of $g_{m1}/I_{D1}$ and $R_1$ set the value of $A_{CG}$. The value of $A_{CG}$ set the value of $A_{CS}$ and therefore the value of $g_{m2}/I_{D2}$, $R_2$, $g_{m3}/I_{D3}$ and $R_3$.
5. Sweep $g_{m1}/I_{D1}$ from weak inversion region ($g_m/I_D = 25$ S/A) to strong inversion region ($g_m/I_D = 5$ S/A) and $R_1$ from $A_{CG\_min}$ to $A_{CG\_max}$. Register the performance metrics of every feasible design in the explored space. Design feasibility and the current bias for the CG and CS are determined by the bias constrains.
6. Determine $g_{m1}/I_{D1}$, $I_{D1}$, $R_1$, $A_{CG}$, $g_{m2}/I_{D2}$, $I_{D2}$, $R_2$, $R_3$, $g_{m3}/I_{D3}$, $I_{D3}$, $A_{CS}$, and $A_{CD}$ for the TIA design that achieves the best bandwidth.
7. Finally, determine transistor widths from $g_m/I_D$, the calculated $I_D$, and the current density ($I_D$/W) look-up tables

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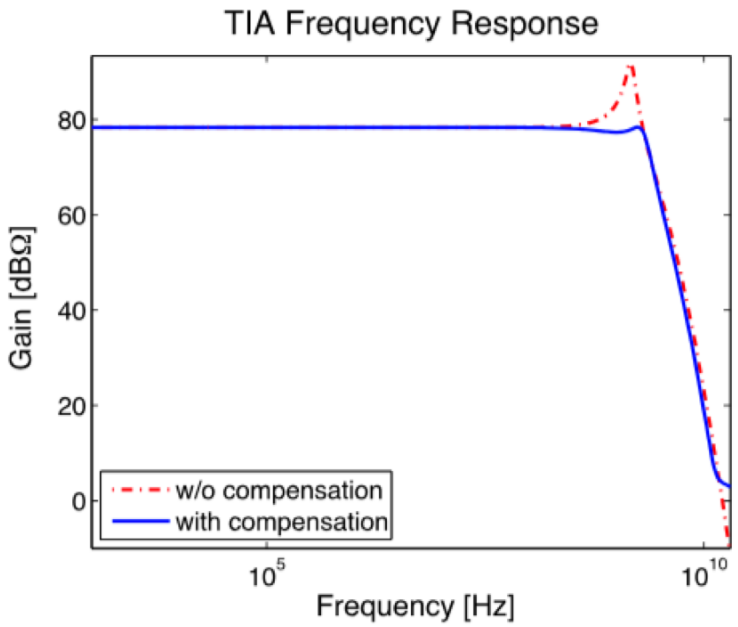
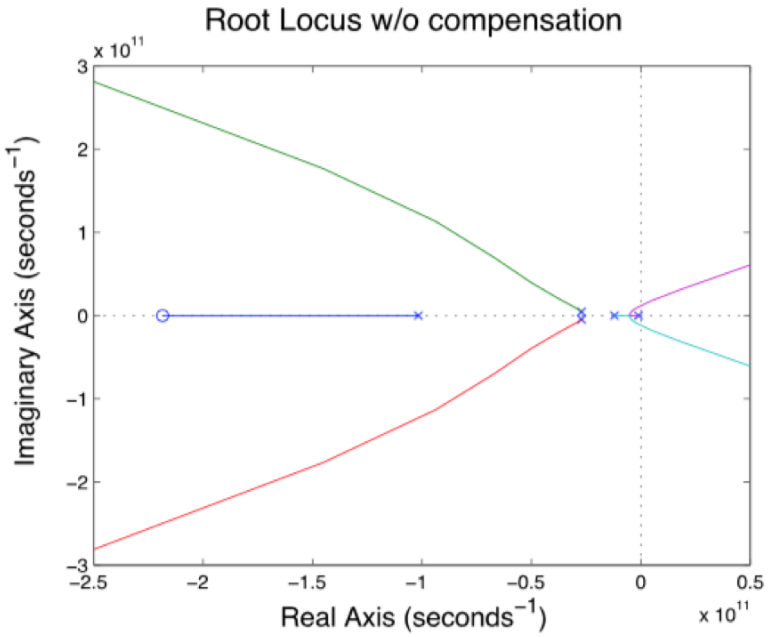
# Results

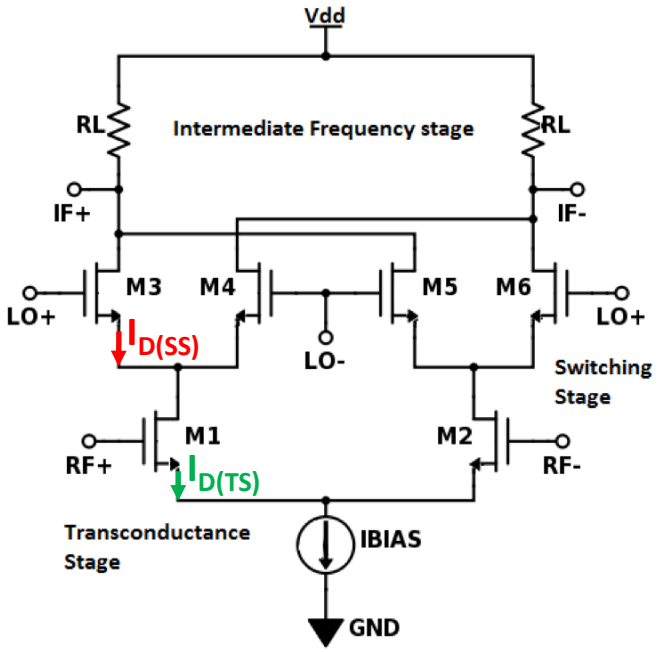
**Table 4** Performance comparison of state-of-the-art CMOS TIAs

| Spec. | [3] | [4] | [9] | [14] | [2] | This work |
|---|---|---|---|---|---|---|
| Gain (dBΩ) | 66 | 66.02 | 94.96 | 69.8 | 72 | 78.34 |
| BW (GHz) | 2.1 | 22 | 0.0018 | 1 | 2.4 | 2.21 |
| Cin (pF) | 0.5 | 0.5 | 2 | 0.5 | 0.5 | 0.5 |
| Input ref. noise (pA/$\sqrt{Hz}$) | 10 | 22 | 0.065 | 4.5 | 18.12 | 11.91 |
| $P_{DISS}$(mW) | 7.2 | 75 | 0.436 | 4.62 | 20.57 | 13.5 |
| FOM (Ω*GHz/mW) | 581.95 | 586.7 | 231.19 | 668.9 | 464.4 | 1352 |
| Process (μm) | 0.18 | 0.09 | 0.18 | 0.18 | 0.18 | 0.18 |
| Supply voltage (V) | 1.8 | 1.2 | 1.8 | 3.3 | 1.8 | 1.8 |



# Gilbert Cell Mixer




***Specifications***:

- A conversion gain greater than 10 dB
- DC-power consumption lower than 3 mW
- A resistive load of 500 Ω
- A target third-order intercept (IIP3) > -5 dBm

***Topology Main Benefits:***

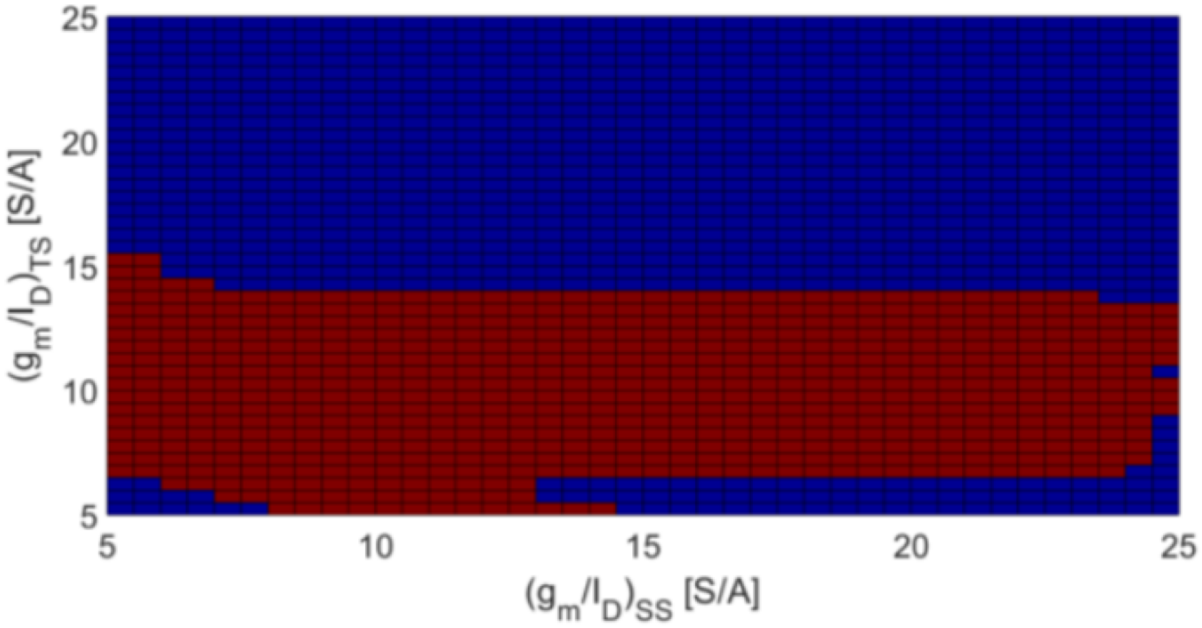
- Simple
- Good port-to-port isolation
- Low even-order harmonic distortion

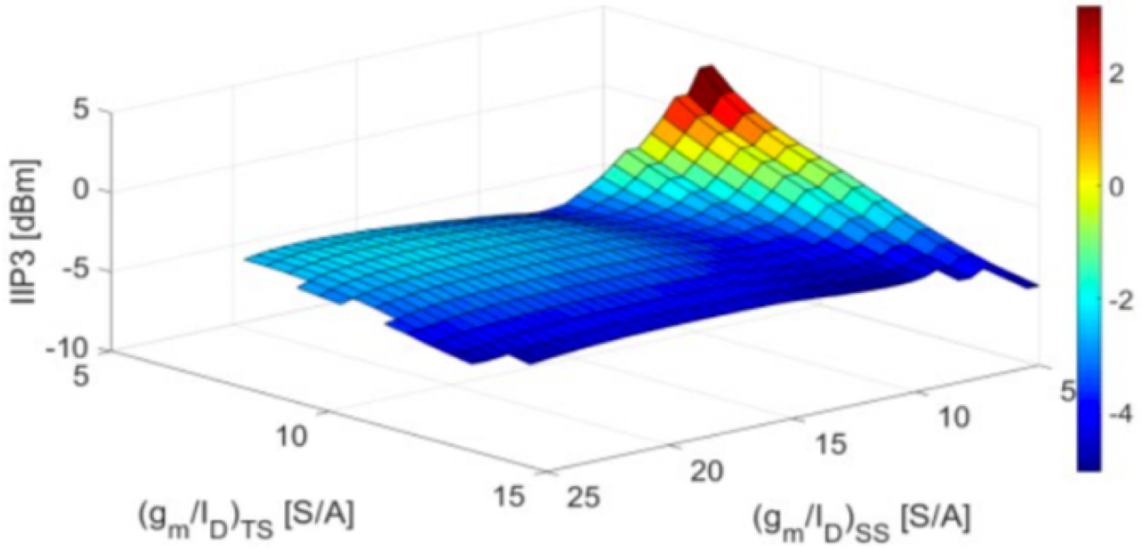
$$A_v \cong \left(\frac{2}{\pi}\right) g_m R_L \qquad g_m = \sqrt{\frac{2KP_n W I_D}{L}}$$

$$I_{BIAS} = 2 \times I_{D(TS)} \qquad I_{D(SS)} = 2 \times I_{D(TS)}$$

***Topology Drawback:***

The cell is composed of a stack of three MOS transistors, so it requires large voltage headroom to keep the transistors biased in saturation, and it results in a large DC-power consumption




# Optimization Framework

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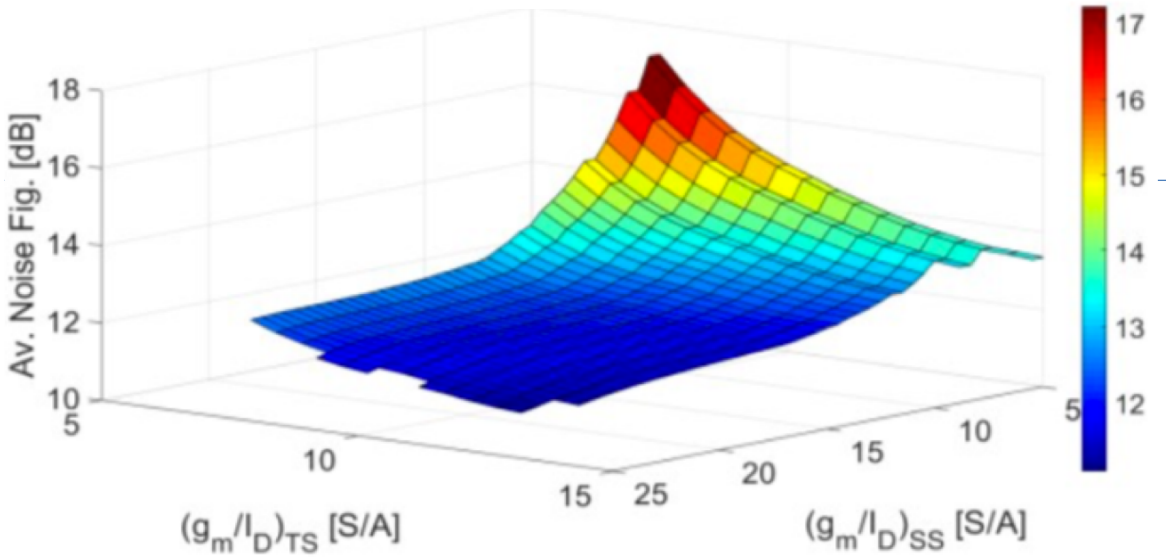
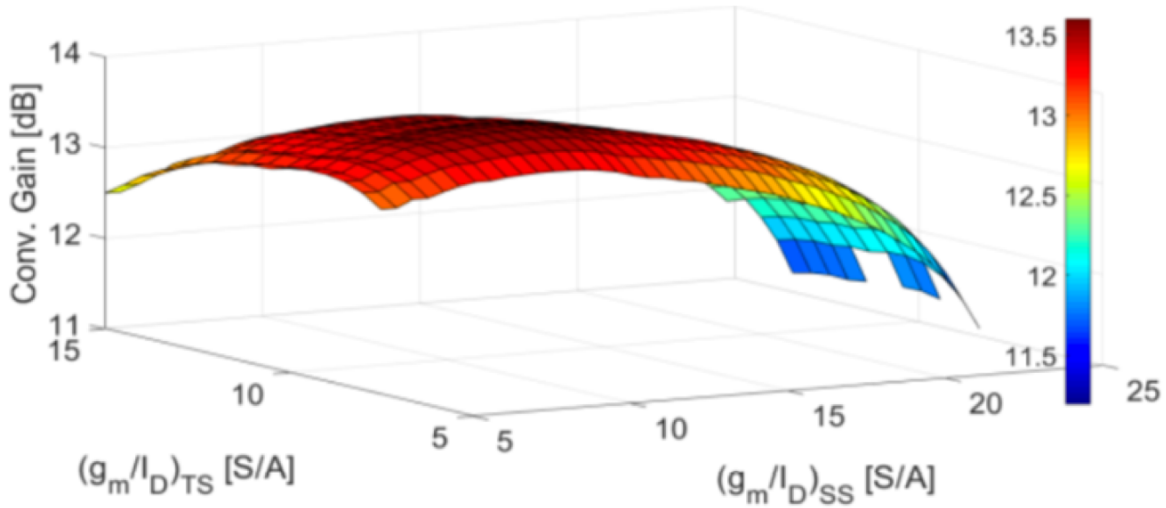



# Optimization Framework

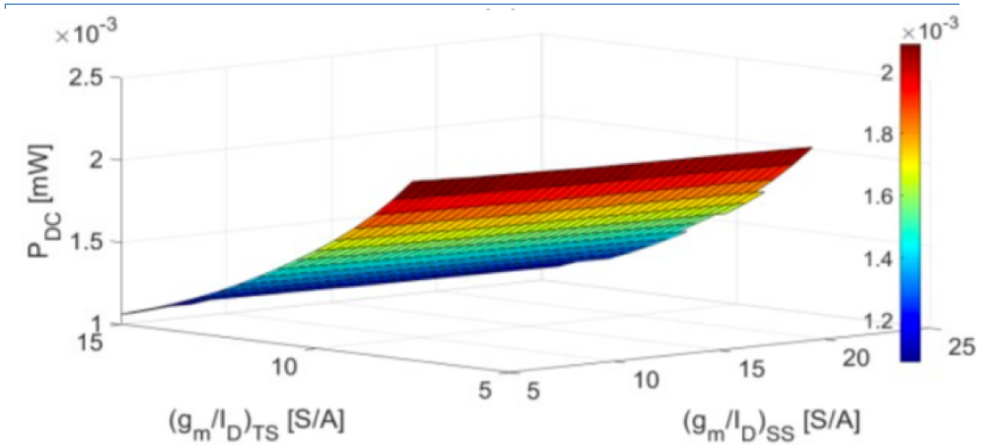
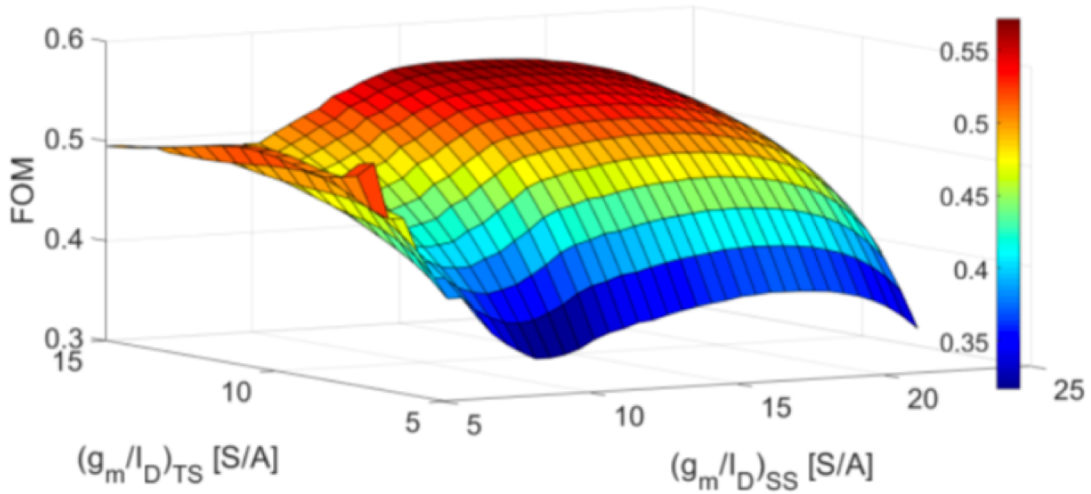



TABLE I. REPORTED PERFORMANCE OF CMOS GILBERT MIXERS

| *Ref.* | *CMOS Tech.* | *Gain [dB]* | *IIP3 [dBm]* | *NF Av. [dB]* | *$P_{DC}$ [mW]* | *FOM* |
|---|---|---|---|---|---|---|
| [4] | 0.13 um | 8 | -3 | 11.2 | 5.57 | 0.12 |
| [9] | 0.18 um | 10 | 4 | 10 | 10 | 0.16 |
| [10] | 0.13 um | 8.95 | -2.2 | 11.4 | 3.7 | 0.16 |
| [11] | 0.13 um | 21 | -1.8 | 15.7 | 18.3 | 0.06 |
| [12] | 0.18 um | 13.5 | -3.25 | 21.22 | 7.2 | 0.06 |
| This Work | 0.13 um | 11.24 | -3.1 | 11.6 | 2.1 | 0.32 |

The performance metrics indicated refers to the core of the mixer

# Optimization Framework




$$FOM = \frac{CG_{[dB]} \cdot IIP3_{[mW]}}{NF_{[dB]} P_{DC[mW]}]}$$

# Gilbert Cell: Framework

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1. Given the target gain and the load resistance specifications, use (1) to derive the value of $g_m$;
2. Once the value of $g_m$ has been set, sweep $g_m/I_D$ (that is the inversion level of the transistors) in the range 5÷25, and let the framework computes the corresponding current levels $I_{D(SS)}$ and $I_{D(TS)}$;
3. Exploiting the lookup table of the current density ($I_D/W$), computes the values of $W_{(SS)}$ and $W_{(TS)}$ for all inversion levels explored. Set the channel length L to the minimum value of 130nm to maximize speed[5];
4. Perform systematic DC analysis of the mixer by independently varying the $g_m/I_D$ ratio for the TS and SS. For each bias point computes the DC-power consumption of the mixer.
5. For each solution checks that the circuit is correctly biased (that is all transistors operates in saturation) and compares the DC-power consumption with the design specification. Discard any unfeasible solution.
6. For each solution left from the previous step, compute the conversion gain of the mixer. Discard any further solution that exhibit a conversion gain lower than the design specifications.
7. Repeat the previous step for the noise figure and the third-order intercept of the system.
8. Explores the pruned solutions space and extract the optimal bias point, that is the bias point that allows to achieve the best tradeoff among the performance metrics of the mixer.

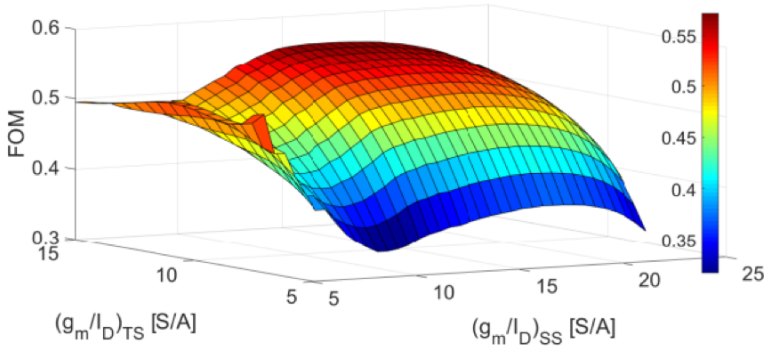
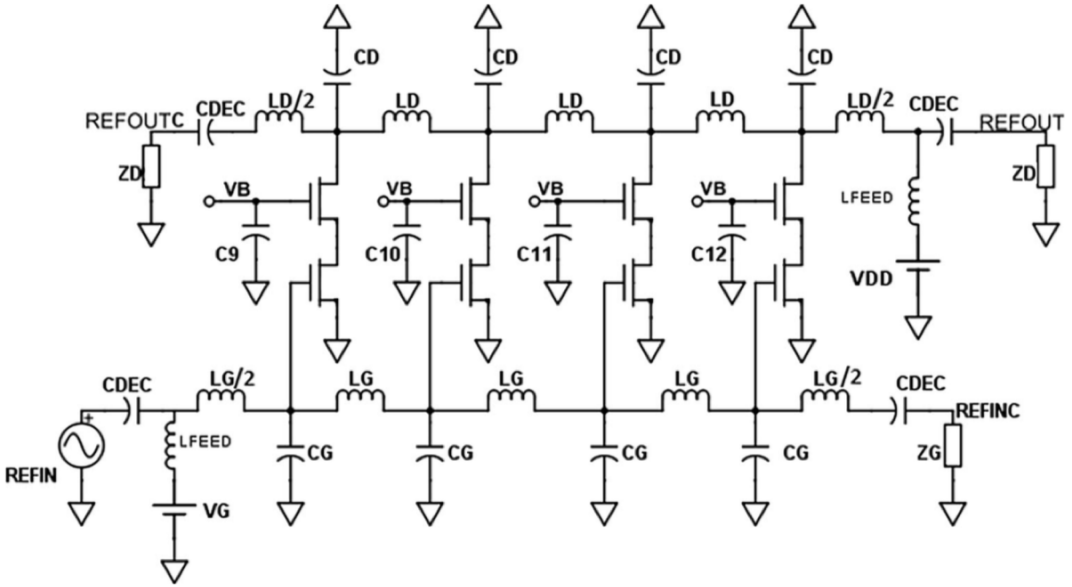



Fig. 4 FOM versus $g_m/I_{D(TS)}$ and $g_m/I_{D(SS)}$ ratios.

$$FOM = \frac{CG_{[dB]} \cdot IIP3_{[mW]}}{NF_{[dB]}P_{DC[mW]}]}$$

# UWB LNA Distributed Amplifier




**Theoretical Gain:**

$$G = \frac{N g_m Z_0}{2}$$

**Upper Bound:**

$$N_{opt} = \frac{\ln\left(A_D/A_G\right)}{A_D - A_G}$$

**Synchronism of propagation:**

$$L_G C_{GG} \approx L_D C_{DD}$$

**Symmetry of characteristic impedance**

$$Z_G = \sqrt{\frac{L_G}{C_G}} = Z_D = \sqrt{\frac{L_D}{C_D}}$$

**Bandwidth:**

$$BW \cong \min\left(\frac{1}{\pi}\sqrt{\frac{1}{C_{GG}L_G}}, \frac{1}{\pi}\sqrt{\frac{1}{C_{DD}L_D}}\right)$$

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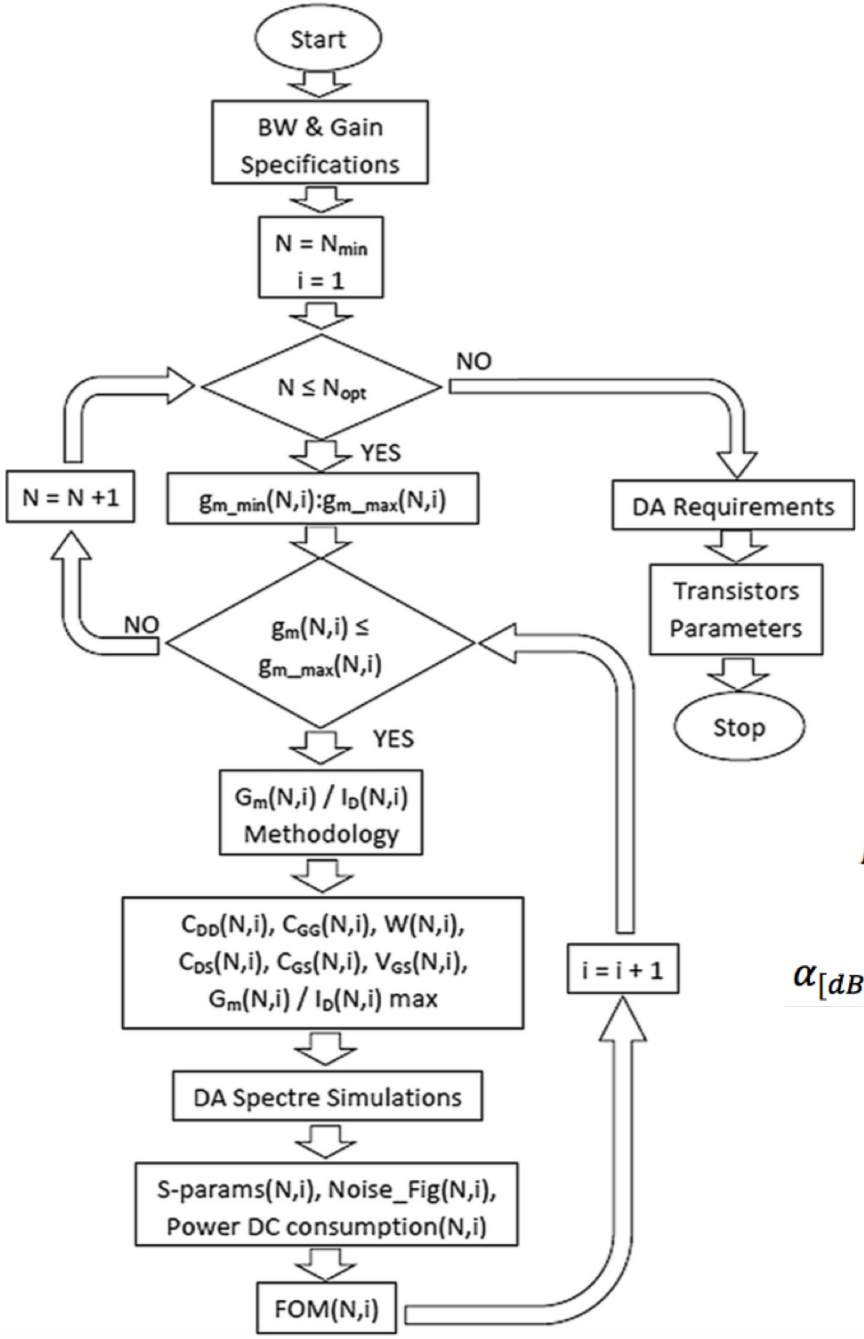
# UWB Framework




$$FOM_{\left[GHz/_{mW\cdot mm^2}\right]} = \frac{\alpha_{[dB]} \cdot BW_{[GHz]}}{NF_{[dB]} P_{DC[mW]} Area[mm^2]}$$

$$\alpha_{[dB]} = 10 \cdot \log_{10}\{|S_{21}|^2 \cdot [(1 - |S_{11}|^2) \cdot (1 - |S_{22}|^2)]\}$$