

## Problem Set

### Problem

Assume you got a new technology file for SPICE, so you need to do some hand calculations and related SPICE simulations to confirm what to expect from the technology at hand.

1. Assume a  $W=40\mu\text{m}$  and  $L=1.6\mu\text{m}$  NMOS device, with  $KP=50\mu\text{A}/\text{V}^2$ ,  $V_{T0}=0.5\text{V}$  and  $\text{COX}=2.3\text{mF}/\text{m}^2$  and use the following lambda scaling rule:

$$\lambda(L) = \frac{0.1 \mu\text{m} \cdot \text{V}^{-1}}{L}$$

For a bias current of 0.25mA and assumed  $V_{ds}=2.5\text{V}$ , compute (by hand) the required  $V_{gs}$  and resulting  $C_{gs}$  as well as small-signal  $g_m$  and  $g_{ds}$  (ignoring all extrinsic capacitances).

2. Now compute by hand all extrinsic capacitances. Assume that  $\text{CGSO}=0.5\text{nF}/\text{m}$  and  $\text{CGDO}=0.5\text{nF}/\text{m}$ . The junction capacitances are specified by the formulae given in Table 1. Table 1 also provides all needed HSPICE parameters. Compute the resulting  $C_{gd}$ ,  $C_{gs}$ ,  $C_{jdb}$ ,  $C_{jsb}$  values (use  $L_{diff}=3\mu\text{m}$ ).
3. Construct an HSPICE deck, to be used for finding out the dc operating point and ".op" output for the circuit of figure 1. Use  $R=10\text{K}\Omega$ ,  $R_i=20\text{K}\Omega$ ,  $V_{DD}=5\text{V}$ ,  $V_B=2.5\text{V}$ ,  $I_B=250\mu\text{A}$  and the model formulation shown in table 2. Run the simulations and confirm your hand calculations in part 1. and 2. (These should be virtually identical to your hand calculations). State exactly how you arrive at the total nodal values provided by SPICE, starting from your results in 1. and 2. Your homework solution must include both your input and output files (Make sure to correctly specify VI to get  $V_{ds}=2.5\text{V}$ ).

Capacitance	Value	
<b>cdtot</b>	<b>cgd+cdb</b>	<b>cdb = cjdb</b>
<b>cgtot</b>	<b>cgs+cgd+cgb</b>	
<b>cstot</b>	<b>cgs+csb</b>	<b>csb = cjsb</b>
<b>cgs</b>	<b>cgs* + cgso*W</b>	<b>cgs_ov = cgso*W</b>
<b>cgd</b>	<b>cgd* + cgdo*W</b>	<b>cgd_ov = cgdo*W</b>

**Triode region:**  $\text{cgd}^* = \text{cgs}^* = (1/2) \cdot \text{cox} \cdot W \cdot L$

**Saturation region:**  $\text{cgd}^* = 0$  ;  $\text{cgs}^* = (2/3) \cdot \text{cox} \cdot W \cdot L$

$$V_{th} = V_{T0} + \text{GAMMA} (\text{PHI} + V_{SB})^{0.5} - \text{GAMMA} (\text{PHI})^{0.5}$$

Table 1.

Parameter	Purpose	nMOS
KP	$\mu_{Cox}$	50uA/V <sup>2</sup>
COX	$\epsilon_{ox}/t_{ox}$	2.3fF/um <sup>2</sup>
VTO	Threshold Voltage	0.5V
LAMBDA	Channel Length Modulation	0.1V <sup>-1</sup> um/L
CGDO,CGSO	Gate-drain, gate-source overlap capacitance	0.5fF/um
CJ	Zero Bias area capacitance	0.1fF/um <sup>2</sup>
CJSW	Zero bias sidewall capacitance	0.5fF/um
PB	Junction potential	0.95V
MJ	Area junction grading coefficient	0.5
MJSW	Sidewall junction grading coefficient	0.33
HDIF	Half length of S/D diffusion (Ldiff/2)	1.5um
GAMMA	Bulk threshold voltage	0.6 V <sup>1/2</sup>
PHI	Surface Potential	0.8V

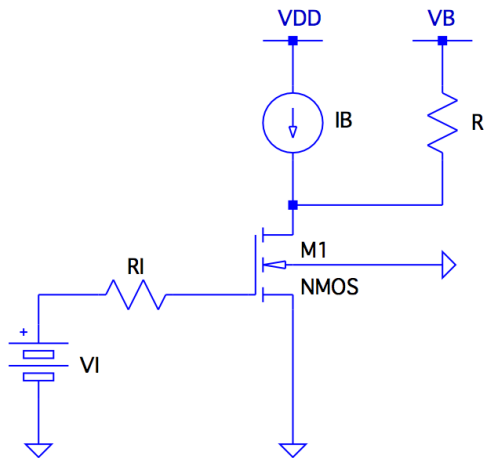
$$C_{jdb} = \frac{AD \cdot CJ}{\left(1 + \frac{VDB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VDB}{PBSW}\right)^{MJSW}}$$

$$C_{jsb} = \frac{AS \cdot CJ}{\left(1 + \frac{VSB}{PB}\right)^{MJ}} + \frac{PS \cdot CJSW}{\left(1 + \frac{VSB}{PBSW}\right)^{MJSW}}$$

Table 2.

```
.param lambda=0.1u
.param Ln=1.6u

.model my_nmos nmos kp=50u vto=0.5 lambda='lambda/Ln' cox=2.3e-3 capop=1
+ cgdo=0.5n cgso=0.5n cj=0.1m cjsw=0.5n pb=0.95 mj=0.5 pbsw=0.95
+ mjsw=0.33 gamma=0.6 phi=0.8
+ acm=3 cjgate=0 hdif=1.5u
```



$I_B = 250 \mu\text{A}$   
 $V_B = 2.5\text{V}$   
 $R = 10 \text{ k}\Omega$   
 $R_I = 20 \text{ k}\Omega$

Figure 1.

Write a short report including:

1. Hand calculation (state clearly any assumption you make)
2. SPICE input and output files
3. Table showing hand calculation and SPICE results. Explain any discrepancy.
4. State exactly how you arrive at the total nodal values provided by SPICE, starting from your hand calculation results.