Circuit Simulation with SPICE

SPICE Simulation

- Introduction to SPICE
- DC Analysis
- Transient Analysis
- Subcircuits
- Optimization
- Power Measurement
- Design Corners

Introduction

- **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
  - Developed in 1970's at Berkeley
  - Many versions are available
  - HSPICE is a robust commercial industry standard
    - Has many enhancements that we will use
- Written in FORTRAN for punch-card machines
  - Circuits elements are called *cards*
  - Complete description is called a SPICE *deck*

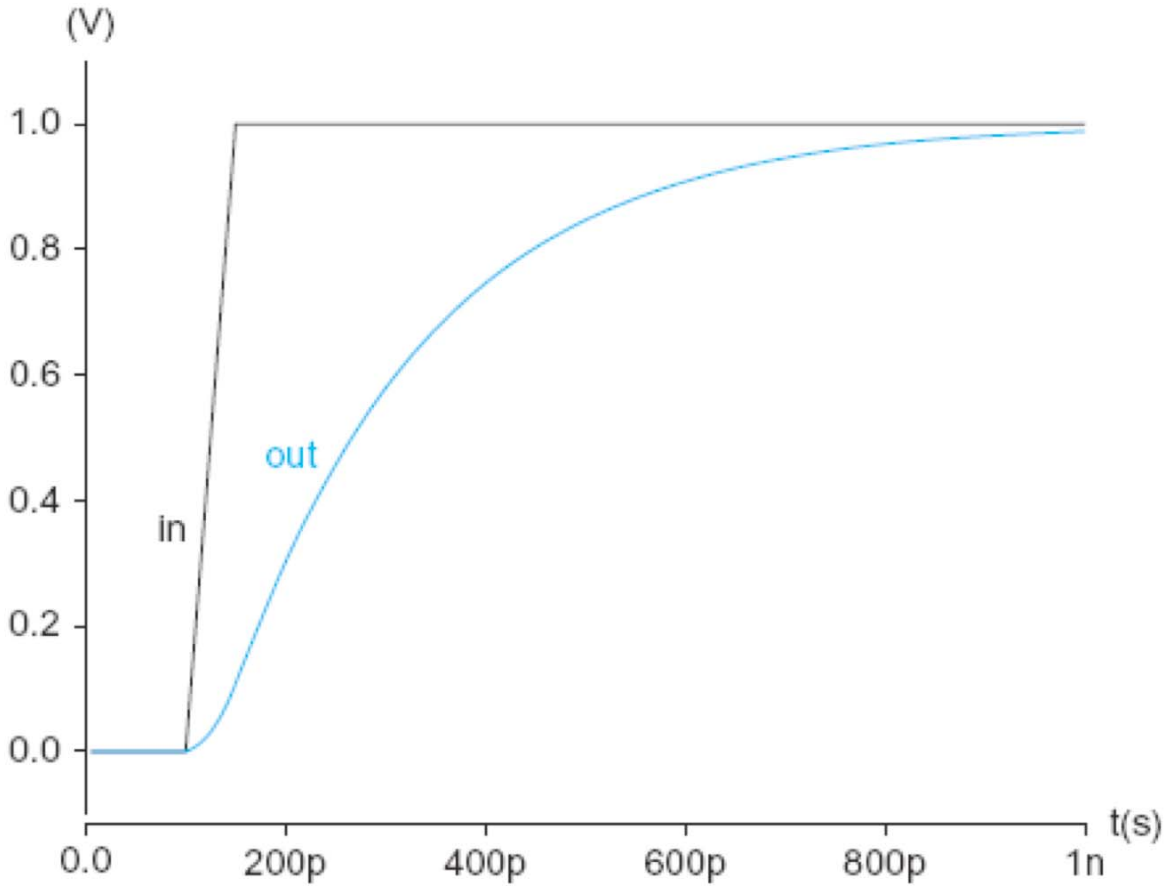
Writing SPICE Decks

- Writing a SPICE deck is like writing a program
  - Plan: sketch schematic on paper or in editor
    - Whenever possible, "modify" existing decks
  - Code: strive for clarity
    - Start with name, date, purpose
    - Comment, comment, comment …
  - Drive the tool (avoid SPICE monkeying):
    - Predict what results should be
    - Compare with actual
    - *Garbage In, Garbage Out!*

Example: A simple RC circuit

```
* rc.sp
* Created  David_Harris@hmc.edu - 2/2/03,
* Modified ctalarico@ewu.edu - 9/17/11
* Find the response of RC circuit to rising input
*-------------------------------------------------
* Parameters and models
*-------------------------------------------------
.option post brief nomod
*-------------------------------------------------
* Simulation netlist
*-------------------------------------------------
Vin in    gnd  pwl  0ps 0 100ps 0 150ps 1.0 1ns 1.0
R1  in    out  2k
C1  out   gnd  100f
*-------------------------------------------------
* Analysis
*-------------------------------------------------
.tran 20ps 1ns
.plot v(in) v(out)
.end
```

Result (Graphical)



Sources (for digital design)

- DC Source

```
Vdd vdd gnd 2.5
```

- Piecewise Linear Source

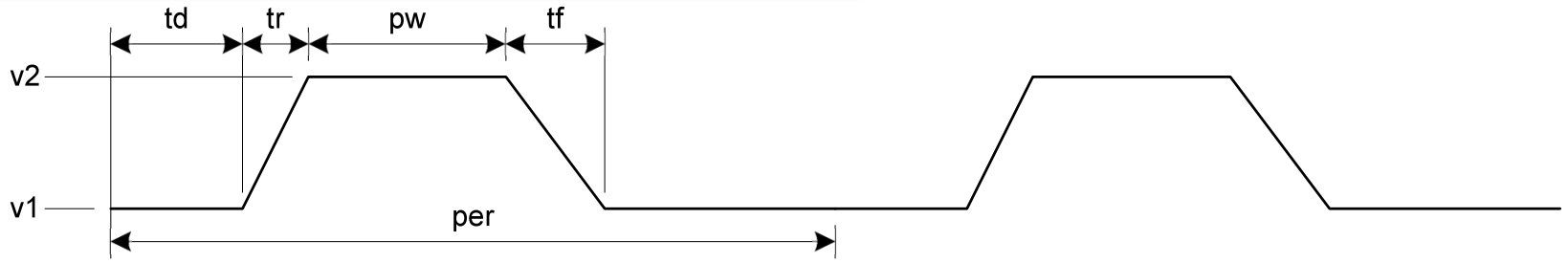
PWL t1 v1 t2 v2 …

```
Vin in gnd pwl 0ps 0 100ps 0 150ps 1.0 1ns 1.0
```

- Pulsed Source

```
Vck clk gnd PULSE 0 1.0 0ps 100ps 100ps 300ps 800ps
```

PULSE v1 v2 td tr tf pw per



SPICE Elements

Letter	Element
R	Resistor
C	Capacitor
L	Inductor
K	Mutual Inductor
V	Independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
W	Lossy transmission line
X	Subcircuit
E	Voltage-controlled voltage source
G	Voltage-controlled current source
H	Current-controlled voltage source
F	Current-controlled current source

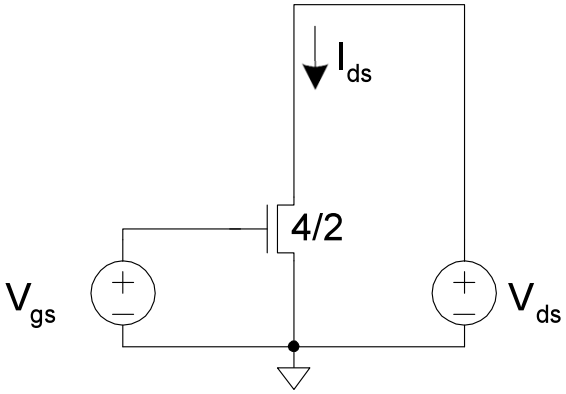
SPICE Units

Letter	Unit	Magnitude
a	atto	10^{-18}
f	fempto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
u	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
x or meg	mega	10^{6}
g	giga	10^{9}

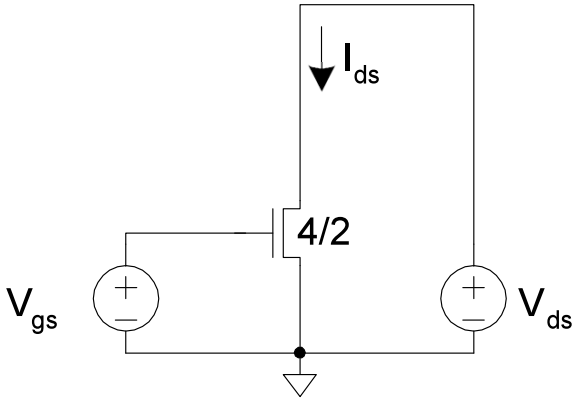
- Example:
  100 femtoFarad capacitor = 100fF = 100f =100e-15

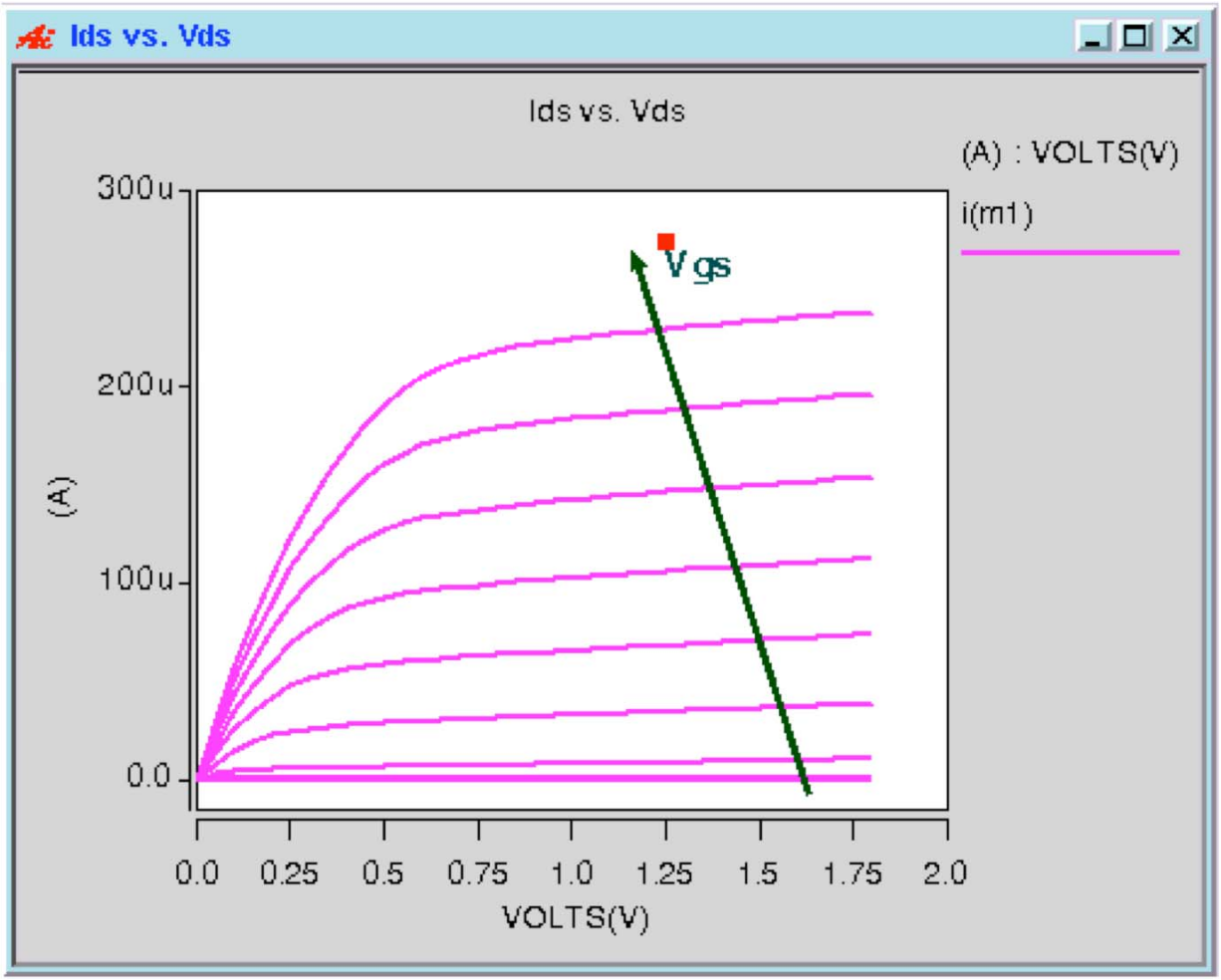
DC Analysis

```
* mosiv.sp
* nMOS I-V Characteristics

*-----------------------------------------------
* Parameters and models
*-----------------------------------------------
.include '../mosistsmc180/mosistsmc180.sp'
.temp 70
.option post brief nomod

*-----------------------------------------------
* Simulation netlist
*-----------------------------------------------
*nmos
Vgs  g gnd 0
Vds  d gnd 0
M1   d g gnd gnd NMOS W=360n L=180n

*-----------------------------------------------
* Analysis
*-----------------------------------------------
.dc Vds 0 1.8 0.05 SWEEP Vgs 0 1.8 0.2
.probe i(m1)
.end
```



nMOS I-V Characteristics (Result)





MOSFET Elements

M element for MOSFET

```
Mname drain gate source body type
+ W=<width> L=<length>
+ AS=<area source> AD = <area drain>
+ PS=<perimeter source> PD=<perimeter drain>
```

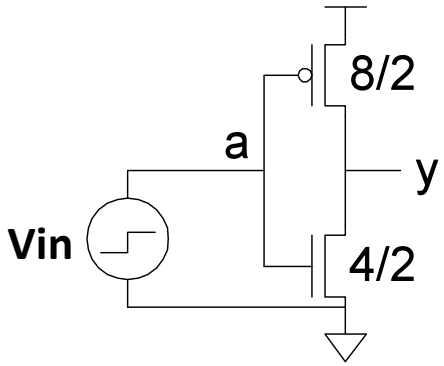
Transient Analysis

```
* inv.sp
*-----------------------------------------------
* Parameters and models
*-----------------------------------------------
.param SUPPLY=1.8
.option scale=90n
.include '../mosistsmc180/mosistsmc180.sp'
.temp 70
.option post brief nomod

*-----------------------------------------------
* Simulation netlist
*-----------------------------------------------
Vdd vdd gnd 'SUPPLY'
Vin a gnd DC 0 PULSE 0 'SUPPLY' 50ps 1ps 1ps 99ps 200ps
M1 y a gnd gnd NMOS W=4 L=2
+ AS=20 PS=18 AD=20 PD=18
M2 y a vdd vdd PMOS W=8 L=2
+ AS=40 PS=26 AD=40 PD=26

*-----------------------------------------------
* Analysis
*-----------------------------------------------
.tran 0.1ps 250ps
.end
```

λ=90n

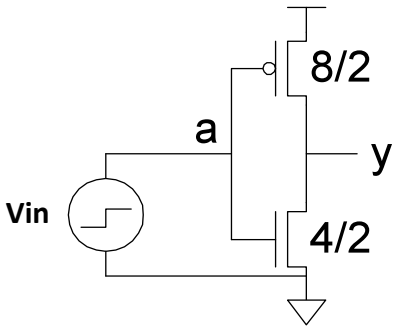
W=360n; L=180n

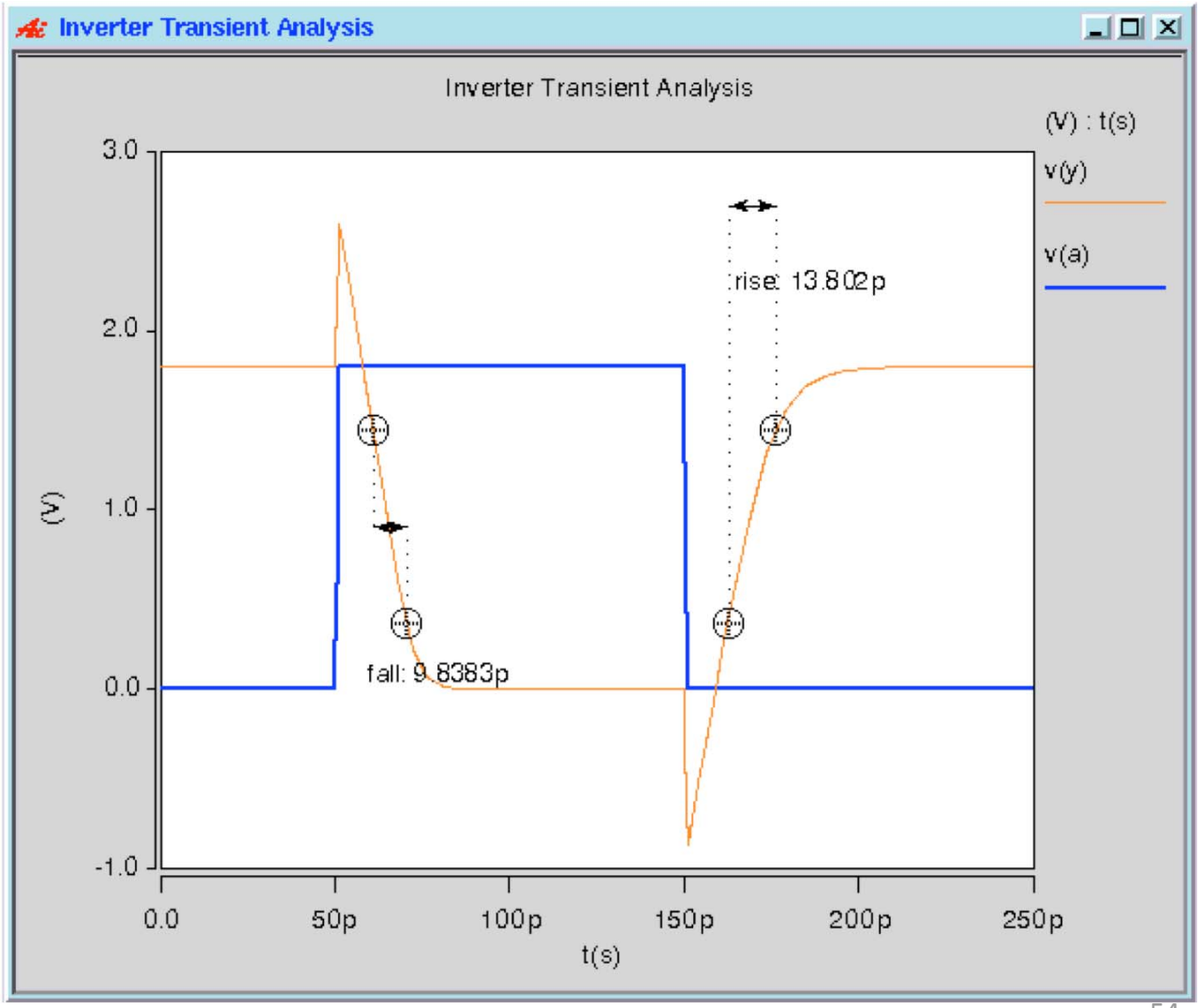
W=720n; L=180n



Transient Analysis Results

- Unloaded inverter with fast edges
  - Overshoot





MOSFET Junction Capacitances

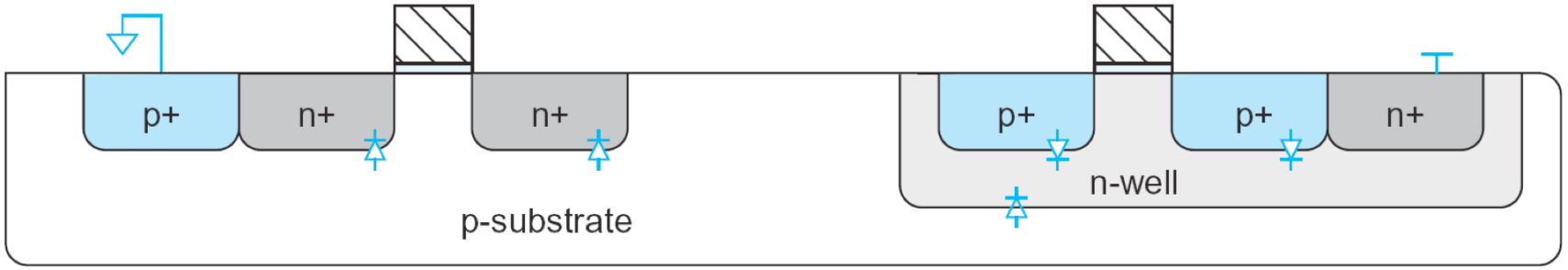
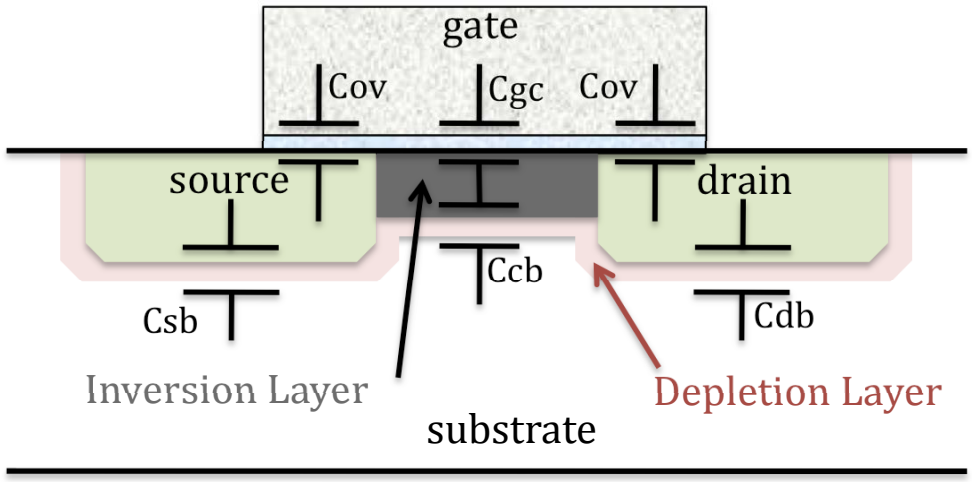
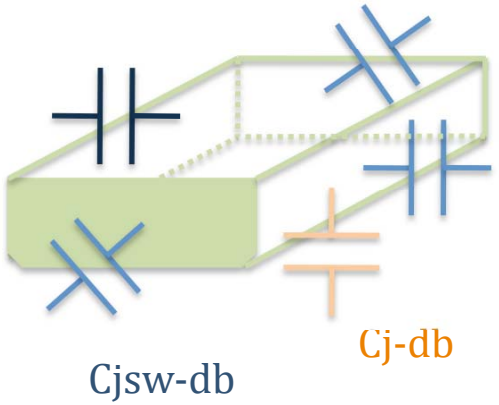


FIGURE 2.22 Substrate to diffusion diodes in CMOS circuits



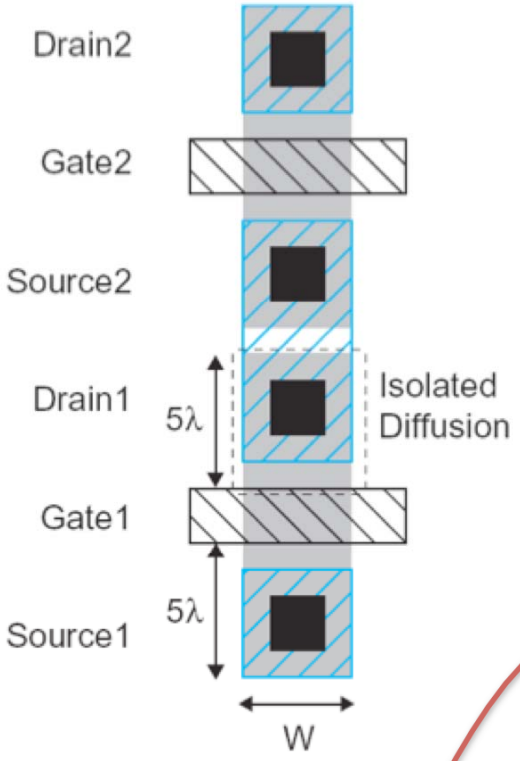


$$Cdb = AD \times Cj\text{-}db + PD \times Cjsw\text{-}db$$

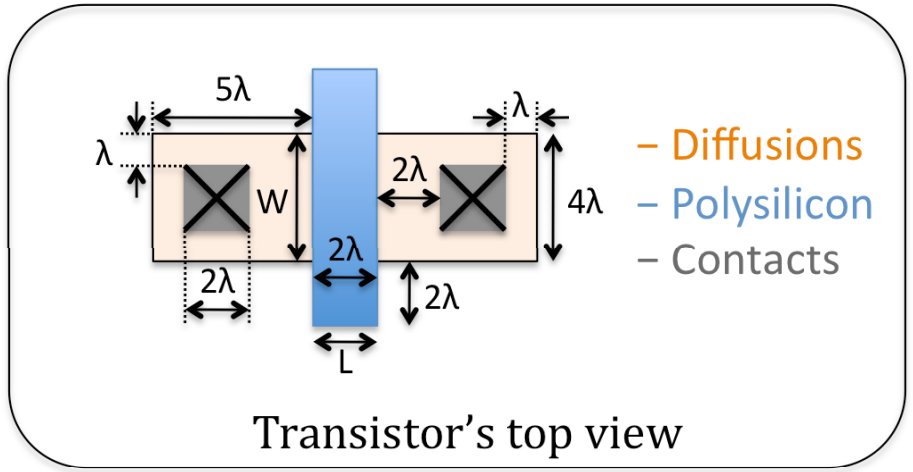
bottom junction cap. per area

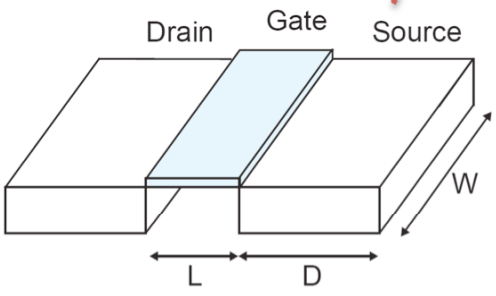
Side wall junction cap. per perimeter

Area and Side Wall Perimeter of the diffusion regions




```
M1 y a gnd gnd NMOS W='N' L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2 y a vdd vdd PMOS W='P' L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends.subckt inv a y N=4 P=8
```





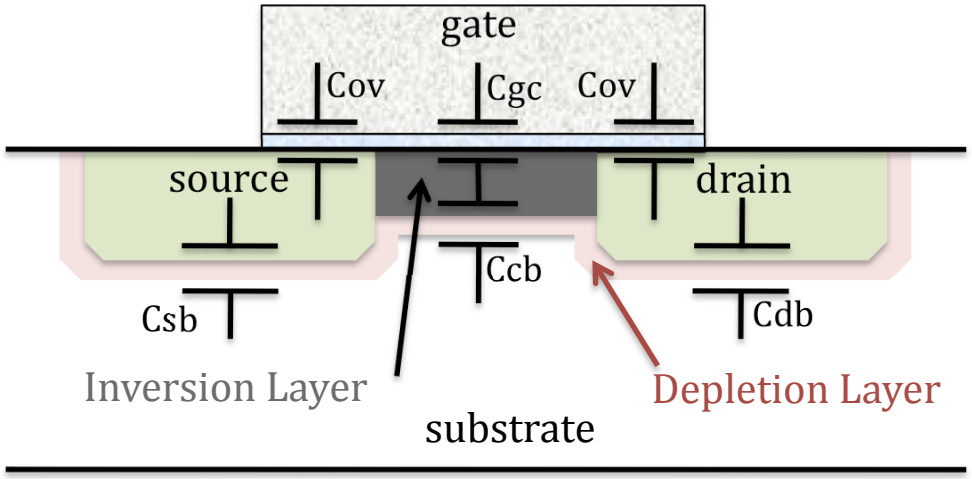
Make sure to check MOS model LEVEL and ACM

AD=AS = W×D; PD=PS = 2W+2D

AD=AS=5$W\lambda^2$; PD=PS=(2W+10)λ

Don't forget we are using .SCALE

MOSFET Capacitances



Cgc modeled through Cgs and Cgd

Ccb modedel through Cgb

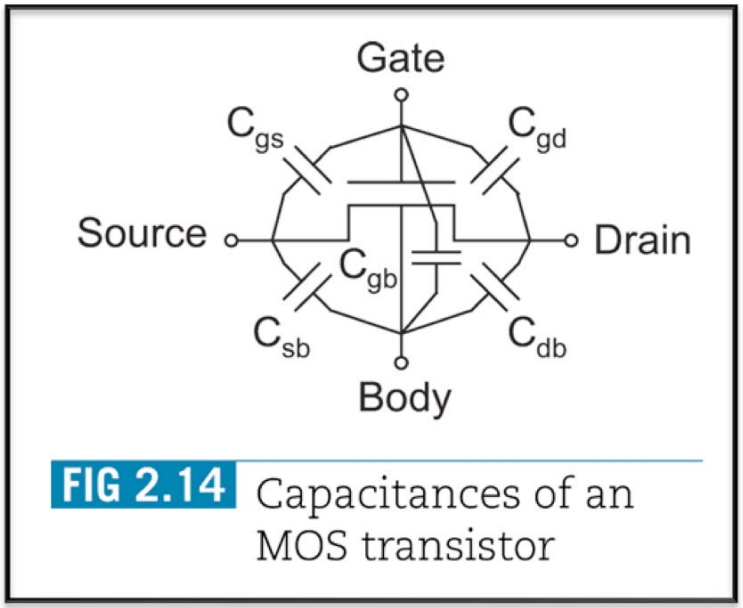
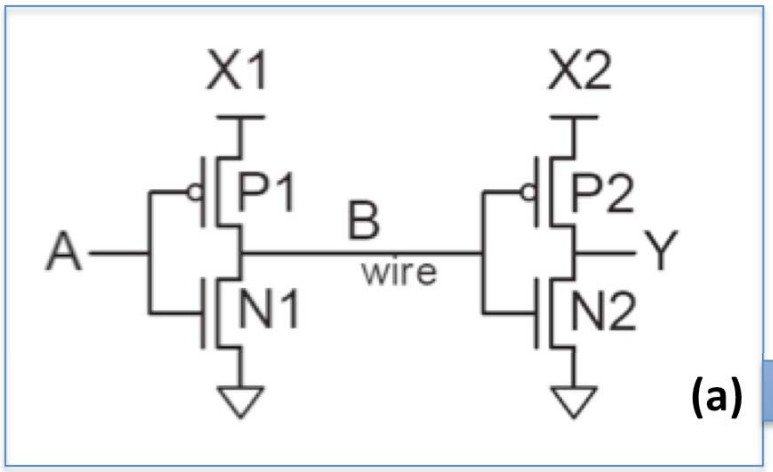
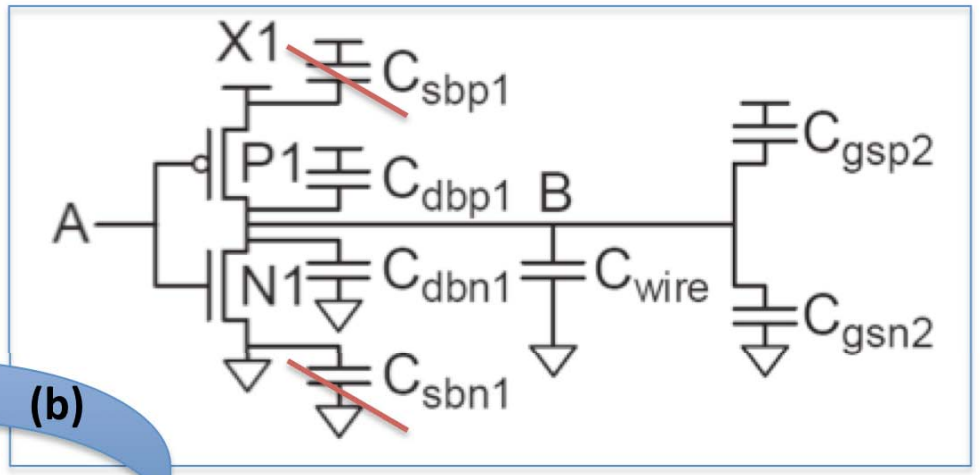
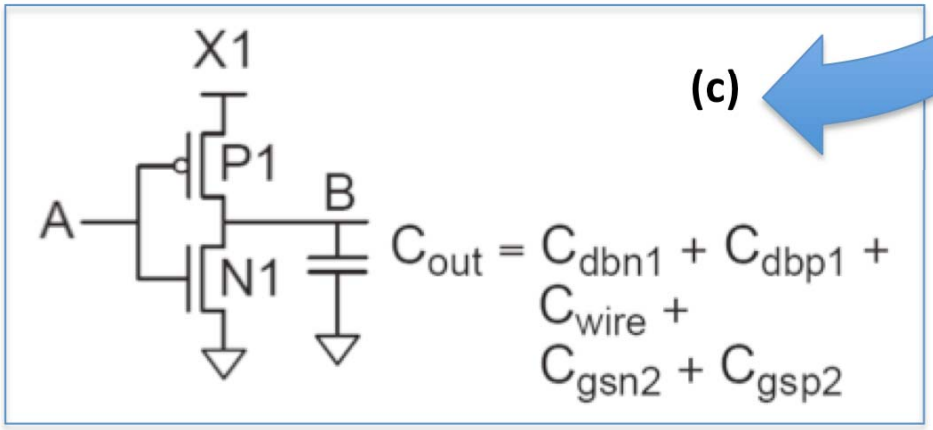


FIG 2.14 Capacitances of an MOS transistor

Inverter Delay Calculation (1/3)







Csb shorted, Cgb negligible
What about Cgd ?

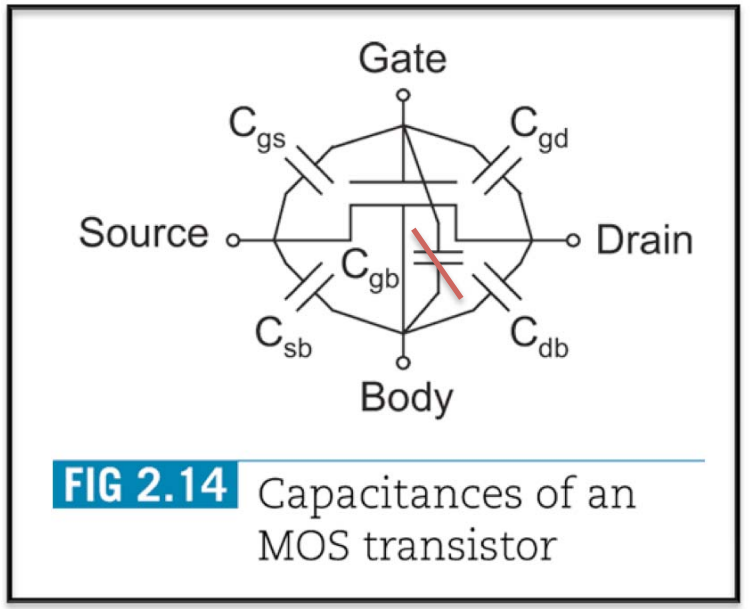
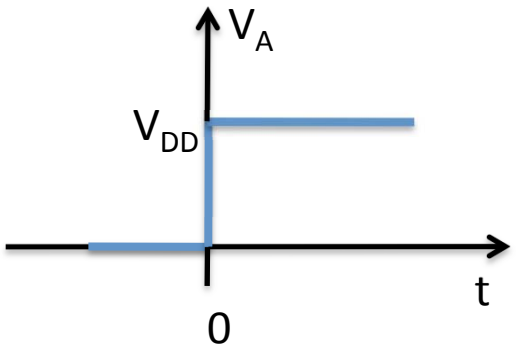
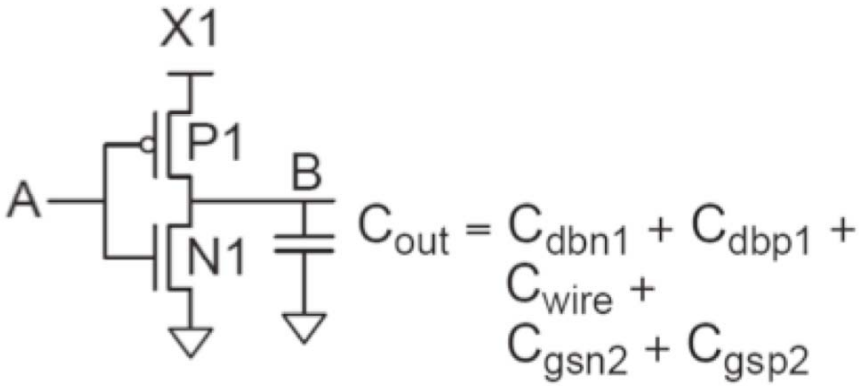


FIG 2.14 Capacitances of an MOS transistor

Inverter Delay Calculation (2/3)

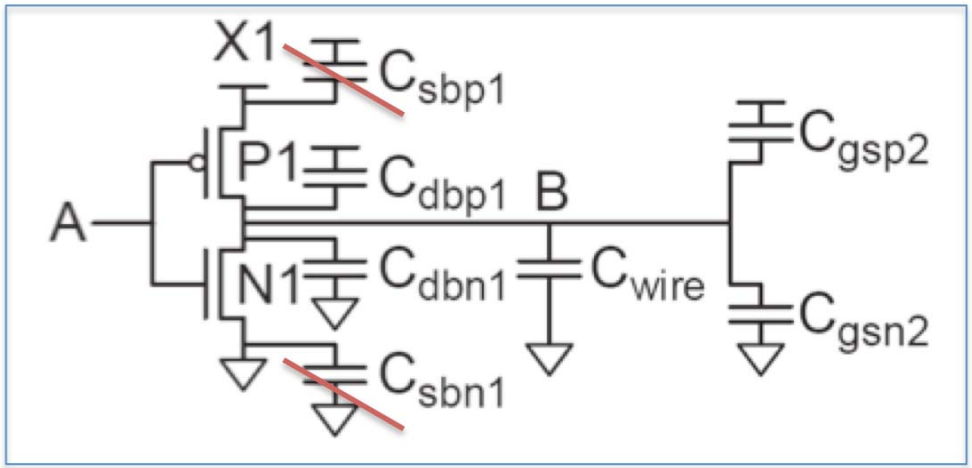




Before the step voltage is applied, V_A=0, N_1 is OFF, P_1 is ON and V_B=V_{DD}.
After the step, N_1 turns ON and it is initially in saturation (V_{ds1} =V_{DD} > V_{gs1}-V_t=V_{DD}-V_t) and later as V_B drops below V_{DD}-V_t it enters linear region.

$$-I_{dn1} = C_{out}\frac{dV_B}{dt}$$

Delay Calculations (3/3)



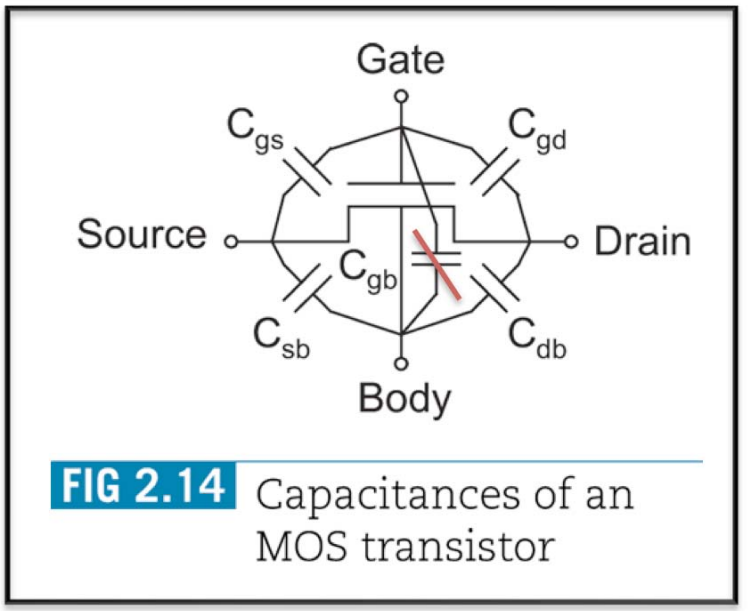
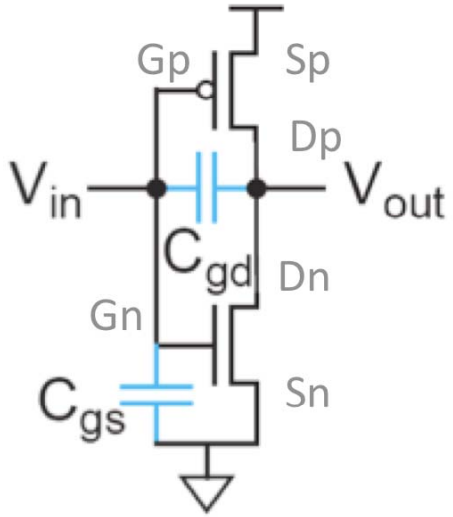
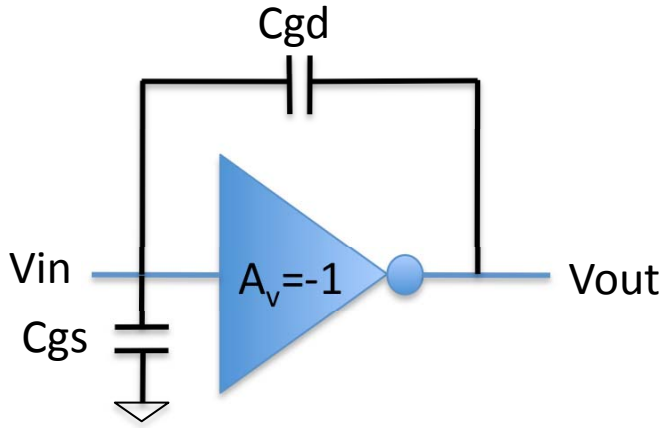


FIG 2.14 Capacitances of an MOS transistor

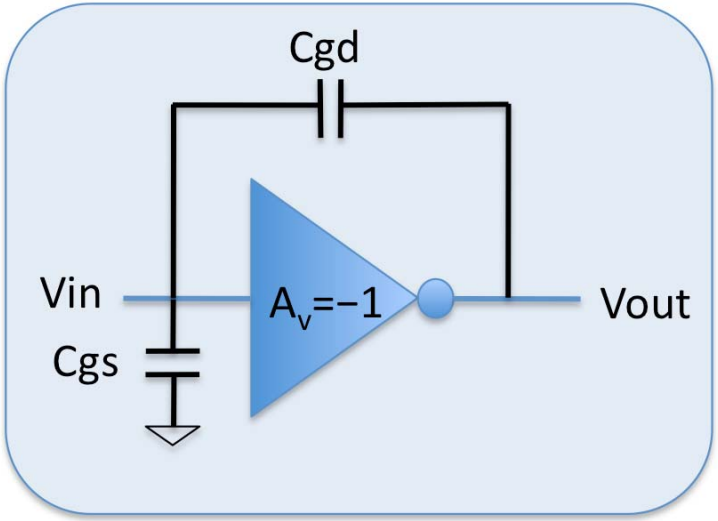
Csb shorted, Cgb negligible.
What about Cgd ?

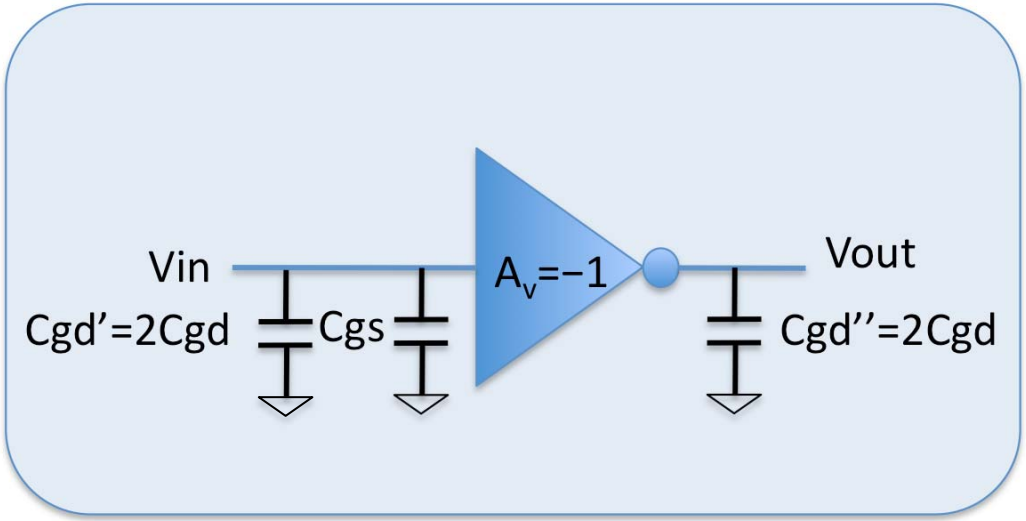
Cgd = Cgdp1+Cgdn1
Cgs= Cgsp1+Cgsn1





Bootstrapping (Miller Effect)





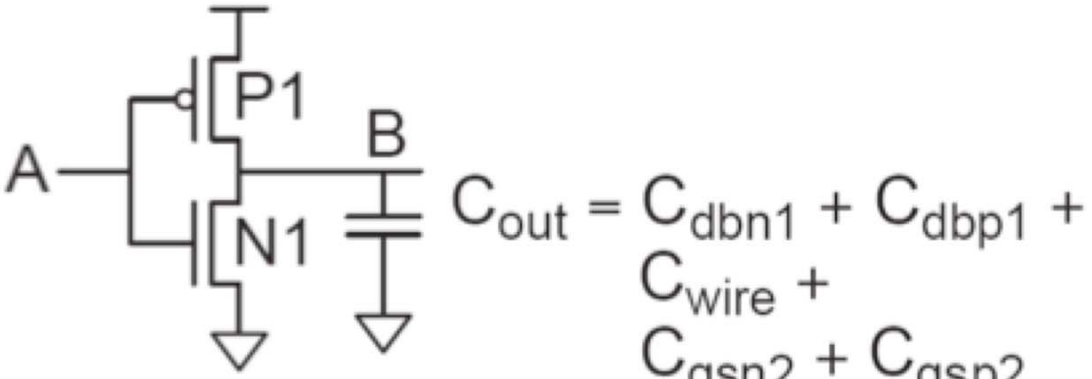
$$A_V = \frac{Vout}{Vin}$$

$$C_{gd}^{'} = C_{gd}\left(1 - A_V\right)$$

$$C_{gd}^{''} = C_{gd}\left(1 - \frac{1}{A_V}\right)$$

Factors affecting delay ? (1/3)

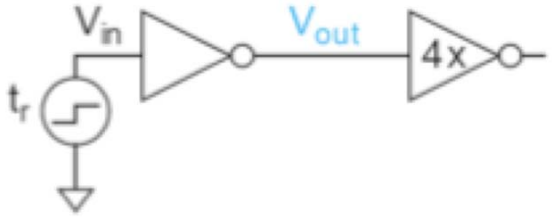
- Output capacitance

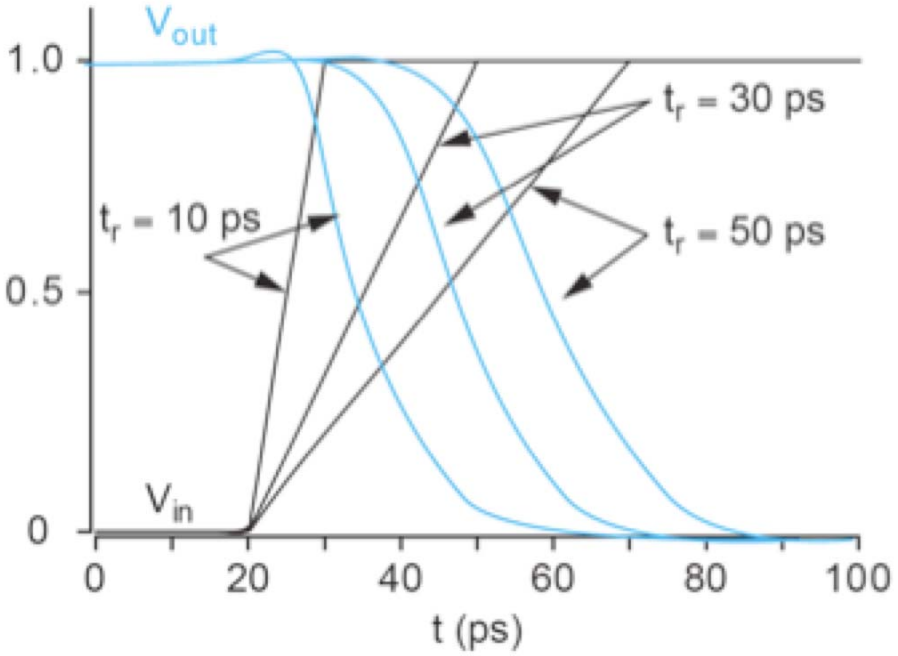


Factors affecting delay ? (2/3)

- Slope of the input waveform (a.k.a. input slew rate)

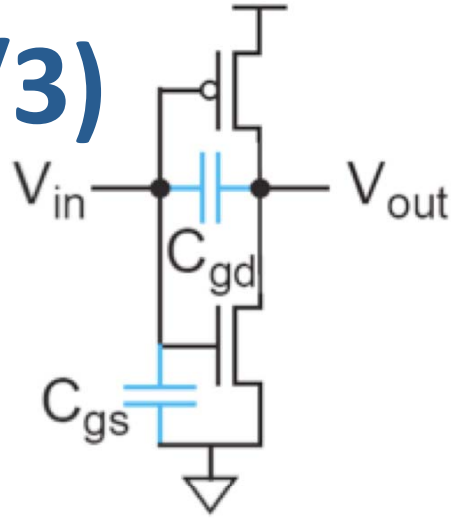
  As the gate voltage changes so does the capacitance (the transistors go through different operating modes, before turning fully ON or OFF)

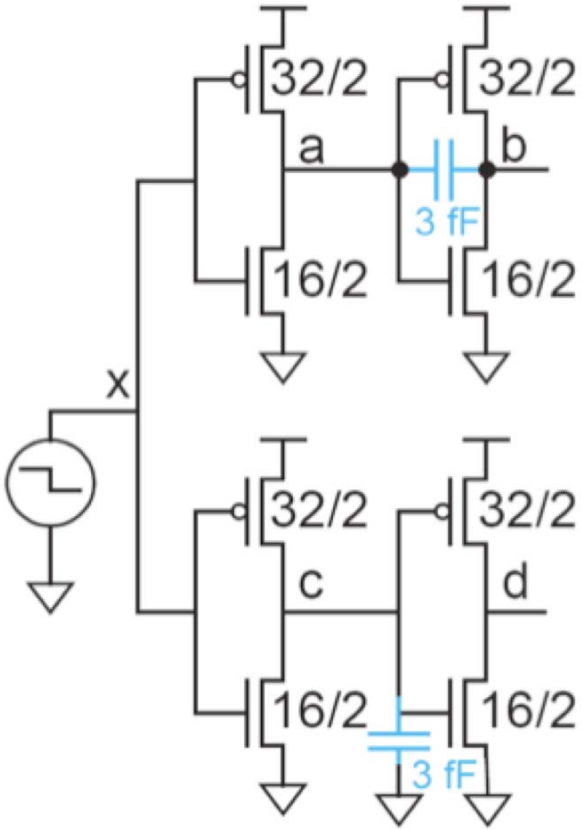




Factors affecting delay ? (3/3)

- Bootstrapping
  the effect of Cgd on gate capacitance is effectively doubled





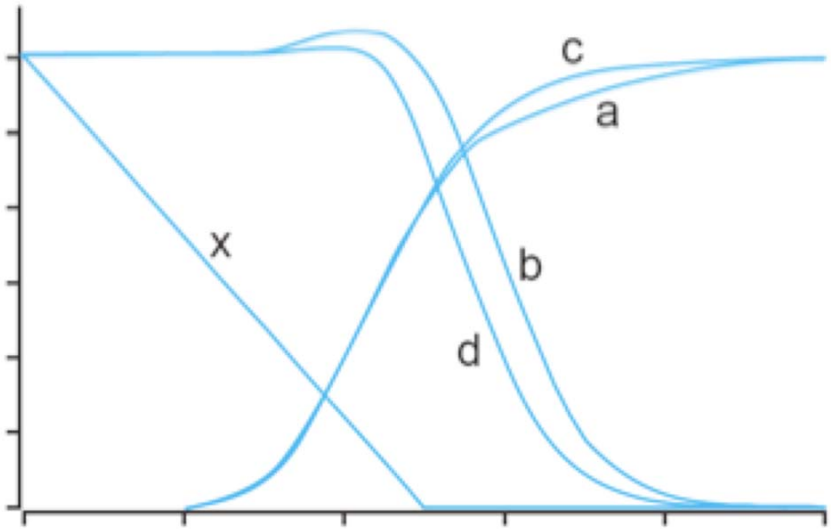


FIGURE 4.28 The effect of bootstrapping on inverter delay and waveform shape

more on Bootstrapping …

- The extra capacitance has greater effect when connected between input and output (feedback) as compared to when is connected between input and ground.
- Because Cgd is fairly small, bootstrapping is only a mild annoyance in digital circuits.
- However is the inverter is biased in its linear region near VDD/2 the Cgd is multiplied by the large gain of the inverter (this is of major importance in analog circuits)

Other factors affecting delay …

- Arrival time at multiple-input gates
- Velocity saturation
- Supply voltage dependence
- Gate-to-source (rather than gate to gnd) capacitance

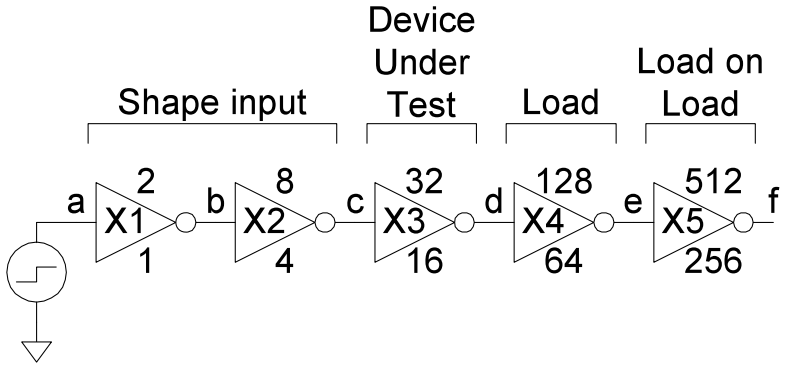
- We'll see the details later …

Subcircuits

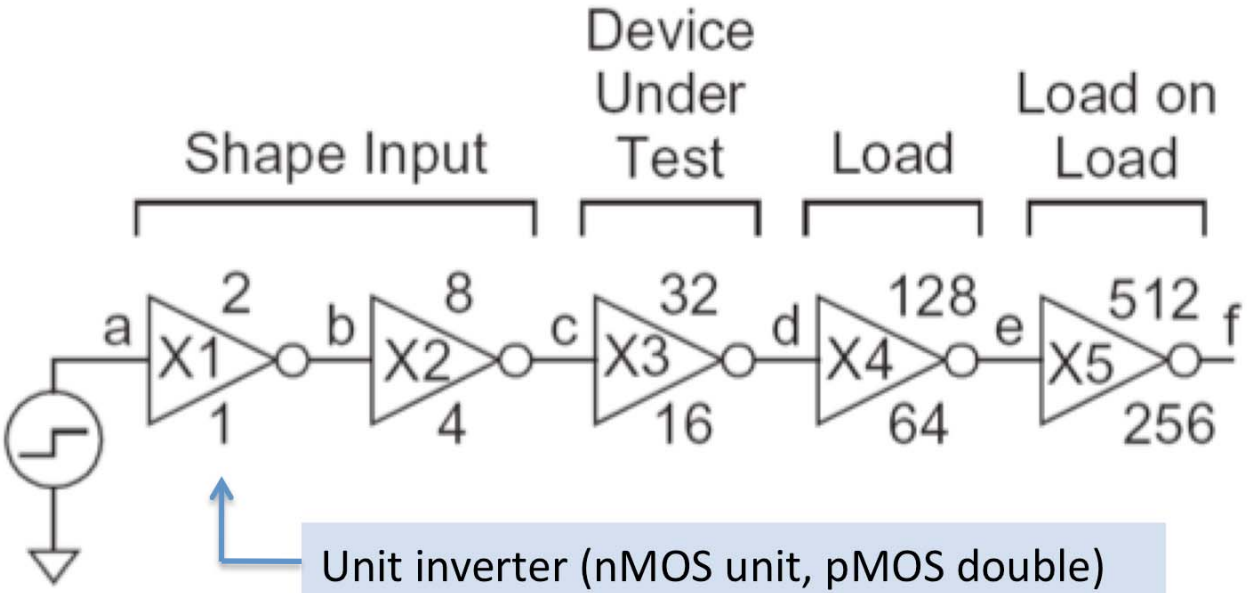
- Declare common elements as subcircuits

```
.subckt inv a y N=4 P=8
M1 y a gnd gnd NMOS W='N' L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2 y a vdd vdd PMOS W='P' L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
```

- Example: Fanout-of-4 Inverter Delay
  - Reuse inv
  - Shaping
  - Loading



FO4 inverter delay



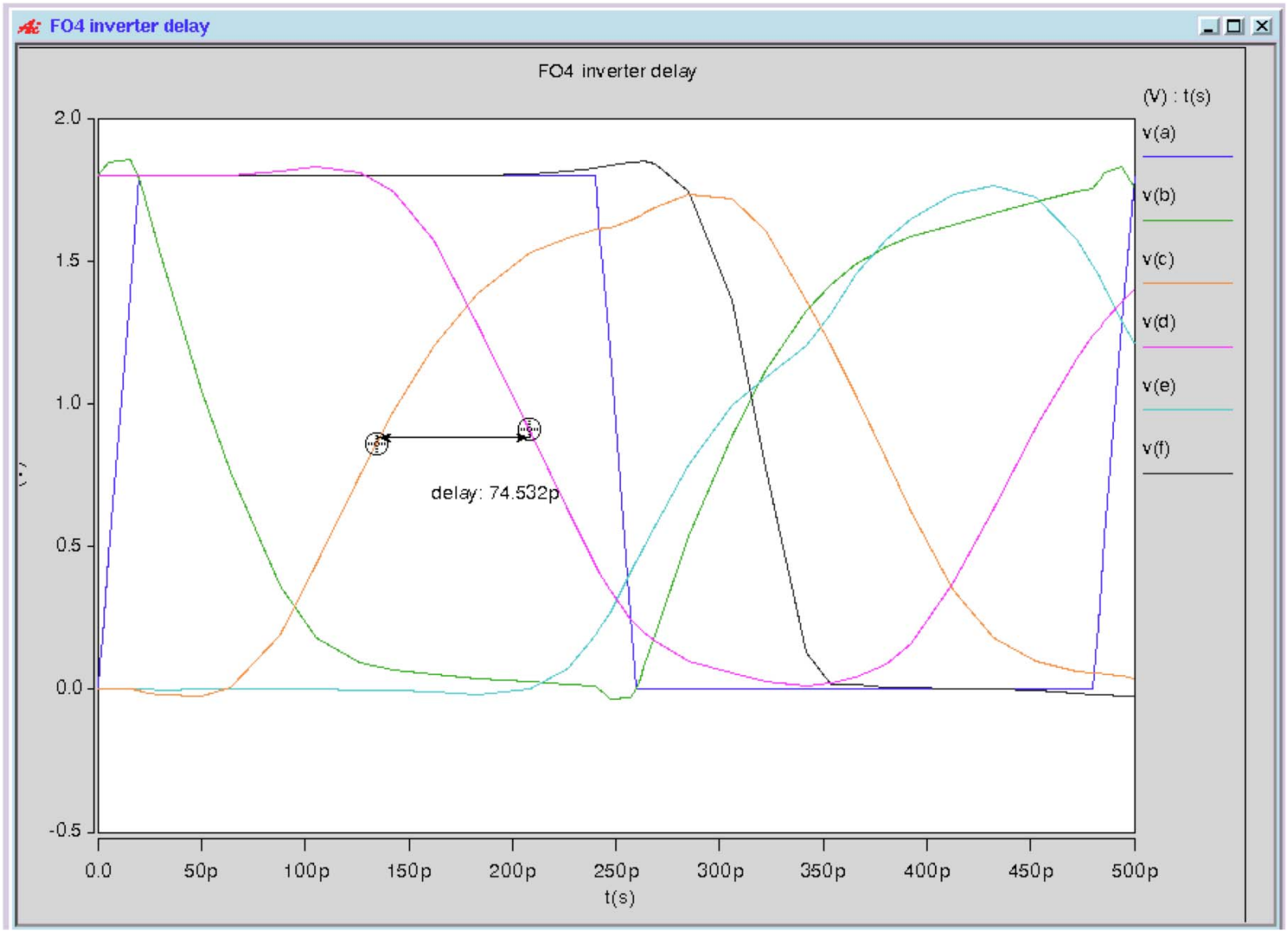

```
X1 a b inv N=4    P=8     *shape input waveform
X2 b c inv N=16   P=32    *reshape input waveform
X3 c d inv N=64   P=128   *DUT
X4 d e inv N=256  P=512   *load
X5 e f inv N=1024 P=2048  *slow down switching rate of e
```

FO4 inverter delay

```
* fo4.sp
* David_Harris@hmc.edu 2/16/05
* Modified C. Talarico 9/30/11
• Delay (typ) of FO4 inverter in TSMC 180nm process

*************** Parameters and models
.param SUPPLY=1.8
.param H=4
.option scale=90n
.include '../mosistsmc180/mosistsmc180.sp'
.option post nomod brief

*************** Subcircuits
.global vdd gnd

.subckt inv a y N=4 P=8
M1      y       a       gnd     gnd     nmos    W='N'   L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2      y       a       vdd     vdd     pmos    W='P'   L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends

************** Simulation netlist
Vdd     vdd     gnd     'SUPPLY'
Vin     a       gnd     PULSE   0 'SUPPLY' 0ps 20ps 20ps 220ps 480ps
X1      a       b       inv             * shape input waveform
X2      b       c       inv     M='H'   * reshape input waveform
X3      c       d       inv     M='H**2' * device under test
X4      d       e       inv     M='H**3' * load
x5      e       f       inv     M='H**4' * load on load

************ Analysis and Measurements
•.tran 1ps 500ps
.measure tpdr                           * rising propagation delay
+     TRIG v(c) VAL='SUPPLY/2' FALL=1
+     TARG v(d)         VAL='SUPPLY/2' RISE=1
.measure tpdf                           * falling propagation delay
+     TRIG v(c)         VAL='SUPPLY/2' RISE=1
+     TARG v(d)         VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2'      * average propagation delay
.measure trise                                  * rise time
+       TRIG v(d)       VAL='0.2*SUPPLY' RISE=1
+       TARG v(d)       VAL='0.8*SUPPLY' RISE=1
.measure tfall                                  * fall time
+       TRIG v(d)       VAL='0.8*SUPPLY' FALL=1
+       TARG v(d)       VAL='0.2*SUPPLY' FALL=1
.end
```

FIGURE 8.10 FO4 SPICE deck

FO4 inverter delay



Optimization

- HSPICE can automatically adjust parameters
  - Seek value that optimizes some measurement
- Example: Best P/N ratio
  - We've assumed 2:1 gives equal rise/fall delays
  - But we see rise is actually slower than fall
  - What P/N ratio gives equal delays?
- Strategies
  - (1) run a bunch of simulations with different P size
  - (2) let HSPICE optimizer do it for us

Optimization P/N ratio

```
* fo4opt.sp
* David_Harris@hmc.edu 2/2/03
* Modified C. Talarico 9/30/11
* P/N ratio for equal rise/fall delay (typ)

•*************** Parameters and models
•.option accurate
.param SUPPLY=1.8
.param H=4
.option scale=90n nomod brief
.include '../mosistsmc180/mosistsmc180.sp'
*************** Subcircuits
.global vdd gnd
.subckt inv a y N=4 P=8
M1      y       a       gnd     gnd     NMOS    W='N'   L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2      y       a       vdd     vdd     PMOS    W='P'   L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
***************  Simulation netlist
Vdd     vdd     gnd     'SUPPLY'
Vin     a       gnd     PULSE   0 'SUPPLY' 0ps 20ps 20ps 220ps 480ps
X1      a       b       inv     P='P1'          * shape input waveform
X2      b       c       inv     P='P1'  M=4     * reshape input waveform
X3      c       d       inv     P='P1'  M=16    * device under test
X4      d       e       inv     P='P1'  M=64    * load
X5      e       f       inv     P='P1'  M=256   * load on load
****************  Optimization setup
.param P1=optrange(8,4,16)              * search from 4 to 16, guess 8
.model optmod opt itropt=30             * maximum of 30 iterations
.measure bestratio param='P1/4'         * compute best P/N ratio
*****************  Stimulus
*.tran 0.1ps 480ps SWEEP OPTIMIZE=optrange RESULTS=diff MODEL=optmod
.tran 0.1ps 280ps SWEEP OPTIMIZE=optrange RESULTS=tpd MODEL=optmod
.measure tpdr                           * rising propagation delay
+       TRIG v(c)       VAL='SUPPLY/2' FALL=1
+       TARG v(d)       VAL='SUPPLY/2' RISE=1
.measure tpdf                           * falling propagation delay
+       TRIG v(c)       VAL='SUPPLY/2' RISE=1
+       TARG v(d)       VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2' goal=0       * average prop delay
.measure diff param='tpdr-tpdf' goal = 0        * diff between delays
.end
```

Optimization Results

Best P/N ratio for lowest average delay is 1:1

.TITLE '* fo4opt.sp'

Index	p1	bestratio	tpdr	tpdf	tpd	diff	temper	alter#
1.0000	4.0000	1.0000	9.163e-11	5.860e-11	7.511e-11	3.303e-11	25.0000	1

Best P/N ratio for equal rise and fall delay is ≈ 2.84:1

.TITLE '* fo4opt.sp'

index	p1	bestratio	tpdr	tpdf	tpd	diff	temper	alter#
6.0000	11.3522	2.8381	8.271e-11	8.270e-11	8.270e-11	2.192e-15	25.0000	1

Design Corners

- It is important to simulate circuits in multiple design corners to verify the correct operation of the circuit across variations in device characteristics (process variations) and environmental conditions (supply an temperature variations)

Design Corners

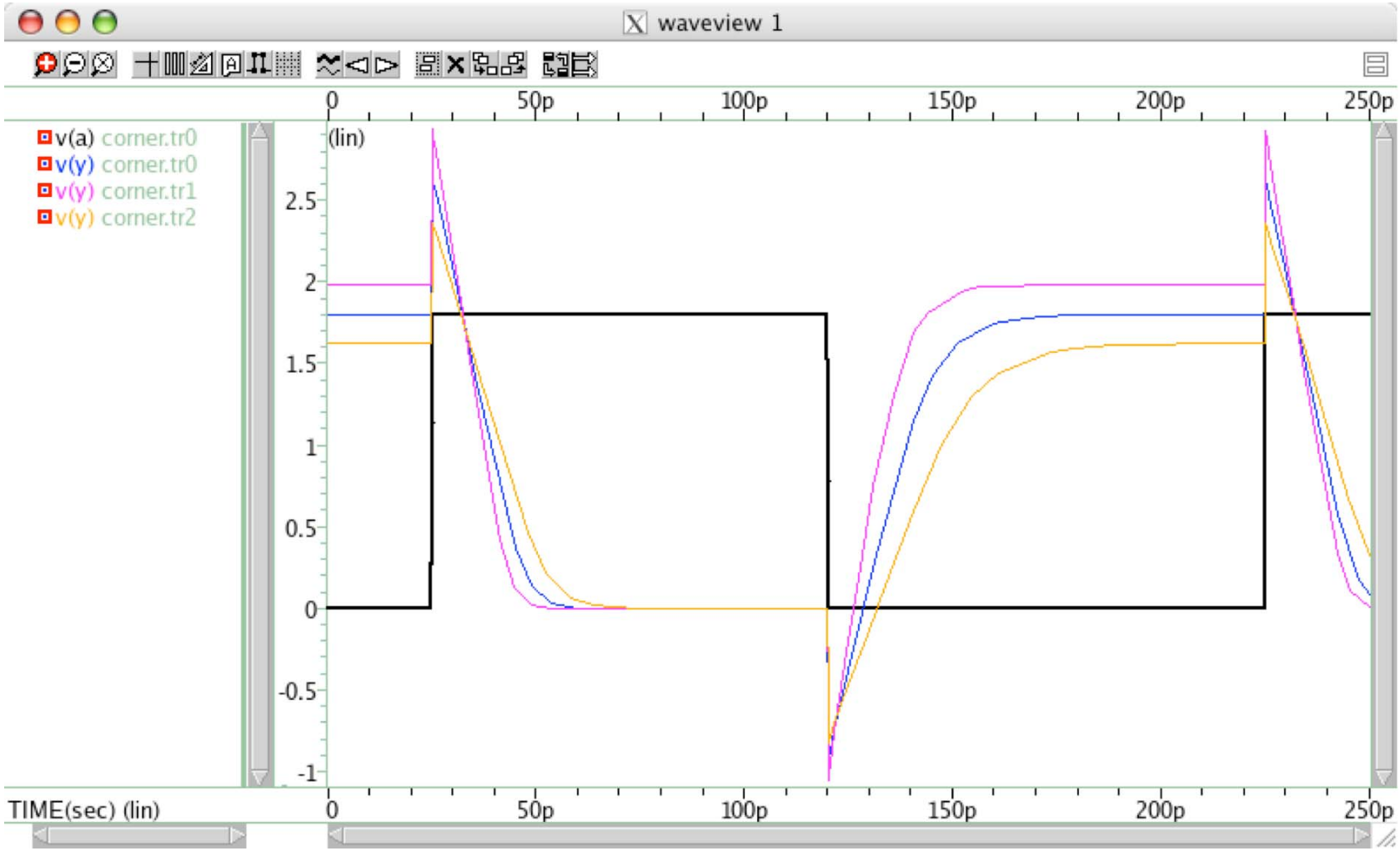
```
* Corner.sp
* Step response of uloaded unit inverter across
* design corners

******** Parameters and models
.options scale=90nm
.param SUP=1.8 *must be set before calling lib
.lib '../mosistsmc180/opConditions.lib' TT
.option post nomod brief

******** Simulation Netlist
Vdd vdd gnd 'SUPPLY'
Vin a gnd PULSE 0 'SUPPLY' 25ps 0ps 0ps 95ps 200ps
Mn y a gnd gnd NMOS W=4 L=2
+ AS=20 PS=18 AD=20 PD=18
Mp y a vdd vdd PMOS W=8 L=2
+ AS=40 PS=26 AD=40 PD=26

******** Analysis
.tran 0.1ps 250ps
.alter
.lib '../mosistsmc180/opConditions.lib' FF
.alter
.lib '../mosistsmc180/opConditions.lib' SS
.end
```

Design Corners

```
* opConditions.lib
* Example of OPCONDITIONS library

* TT: Typical nMOS, pMOS, voltage, temperature
.lib TT
.temp 70
.param SUPPLY='SUP'
.include 'modelsTT.sp'
.endl

* SS: Slow nMOS, pMOS, low voltage, high temperature
.lib SS
.temp 125
.param SUPPLY='0.9 * SUP'
.include 'modelsSS.sp'
.endl

* FF: Fast nMOS, pMOS, high voltage, low temperature
.lib FF
.temp 0
.param SUPPLY='1.1 * SUP'
.include 'modelsFF.sp'
.endl

* and so on ...
```

Design Corners

TT
FF
SS



Power Measurements

- HSPICE can measure power
  - Instantaneous P(t)
  - or average P over some interval

```
.print P(vdd)
.measure pwr AVG P(vdd) FROM=0ns TO=10ns
.measure charge INTEGRAL I(Vdd) FROM=0ns TO=10ns
.measure energy param='charge*SUPPLY'
```

Power Measurements

- Power in single gate
  - Connect to separate V_{DD} supply
  - When the input of a “logic gate” switches, it delivers power to the supply through the gate-to-source capacitances. Be careful to differentiate this input power from the power drawn by the “logic gate” discharging its internal and load capacitance