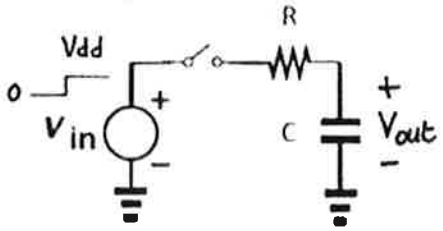
Problem Set #1

PB0



Given an RC circuit which input is a voltage step from 0 to V_{DD}, and which output is the voltage on the capacitor, derive the circuit delay time (time it takes the output voltage to reach the 50% of its final value), and the circuit rise time (time it takes the output voltage to go from the 10% to the 90% of its final value).

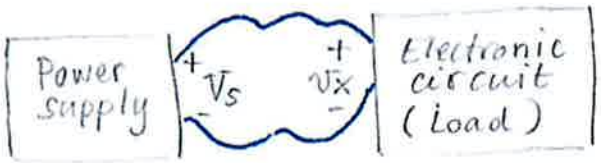
Verify the correctness of your results using MATLAB.

PB1

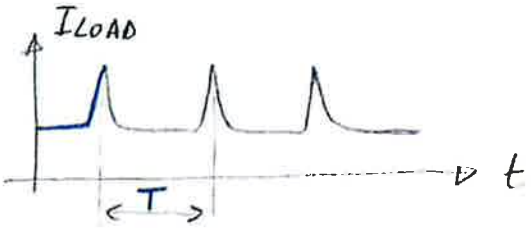
Use matlab to confirm the statements on slides 6 and 7 of the slide set on first and second order circuits.

PB2.

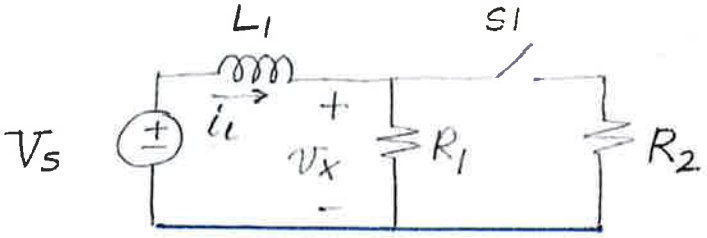
Consider the following system:



The current drawn by the load is time varying



Assuming the system can be resonably modeled as follows:



$V_s = 1.5V$

$L_1 = 500\,nH$

$R_1 = 1\,K\Omega$

$R_2 = 10\,\Omega$

$T = 5\,ns$

a. sketch $i_L(t)$ and $v_x(t)$

b. In order for the electronic circuit to work correctly the voltage v_x across it, should

not vary more than ±100 mV w.r.t. the nominal voltage supply $V_S = 1.5V$
If this is not the **case** how can you modify the system to fix the issue ?

c. Draw a model of your "modified" system (make sure to properly size any component you add to the original model)

d. SPICE the model with and without modification and illustrate that your modification represent a significant improvement.
Make sure to illustrate that the SPICE results are reasonably close to your expectations.