## LTspice QuickStart

## CMOS inverter schematic and simulation using LTspice

1. start LTspice either through the GUI (double click on the SWCAD III icon) or using the following command: wine *whateverpath\_to/scad3.exe* 



2. Open: File > New Schematic



A new schematic file (Draft1.asc) will open for you to edit.

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3. Select, place, edit and connect together the necessary circuit elements.

Select the PMOS device:

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	op SPICE Directive	'S'																				
	SPICE Analysis																					
	Resistor	'R'																				
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	3 Inductor	'L'																				
	Ż Diode	'D'																				
	Component	F2																				
	Ém <u>R</u> otate	Ctrl+R																				
	É 3 Mirror	Ctrl+E																				
	💋 Draw <u>W</u> ire	F3																				
	며 Label <u>N</u> et	F4																				
	→ Place <u>G</u> ND	'G'																				
	Place BUS tap																					
	Telete	F5																				
	Duplicate	F6																				
	Move	F7																				
	Paste																					
	<pre>(') Drag</pre>	F8																				
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Select Comp	onent Symbol					
Top Directory:	C:\Program Files\LTC\	C\SwCADIII\lib\sym				
	µ	P-Channel MOSFET transisto substrate connection(used for MOSFETS)	r with explicit r monolithic			
c.		Open this macromodel's t	est fixture			
	Ċ d	pmos4				
💼 C:\Program F	iles\LTC\SwCADIII\lib\	sym\				
bv cap CNSW csw current diode e e2 f FerriteBead FerriteBead	FerriteBead_Z(I) g g2 h ind ind2 LED load load2 lpnp Itline	mesfet njf nmos nmos4 npn npn2 npn3 npn4 pjf pmos pmos4	pnp pnp2 polcap res res2 schottky SLM SLx sw tline			
			>			
C	ancel	ОК	]			

Click OK to confirm the selection. Drag the mouse to the position where you want to place the device and then left click.

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Type Ctrl+R to rotate or Ctrl+E to mirror.	



Type ESC and then right click on the symbol to edit the device parameters.

Monolithic MOSFET - M1		X
Model Name: Length(L): Width(W): Drain Area(AD): Source Area(AS): Drain Perimeter(PD): Source Perimeter(PS): No. Parallel Devices(M):	PMOS_tr 0.5u 1u	OK Cancel
PMOS_tr I=0.5u w=1u		



If you want to change the name (M1) of the transistor or the location of the name, right click on the name of the transistor.

Enter new referen	ce designator for M1 🛛 🛛 🔀
Justification Left 🗸	OK Cancel
M_p	



The appearance of the circuit can be modified at any time by using the Edit Menu (or the corresponding toolbar icons)

🖊 Line	ar Technology LTs	spice/Switc	herCAD III - [Draft1.asc]	
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	op SPICE Directive	'S'	, <b>P</b>	
	SPICE Analysis		M_p	
	Resistor	'R'		
	芉 Capacitor	'C'	alt wos_u	
	3 Inductor	'L'		
	Ż Diode	'D'		
	D ⊆omponent	F2		
	Em Rotate	Ctrl+R		
	É <u>a</u> Mirror	Ctrl+E		
	🖉 Draw <u>W</u> ire	F3		
	P Label <u>N</u> et	F4		
		'G'		
	► Place BUS tap			
	X Delete	F5		
	Duplicate	F6		
	Move Move	F7		
_	🖪 Paste			



Add the NMOS device and the voltage sources (Edit > Component)

Right click on the NMOS device and the voltage sources to enter their parameters. To set the parameters of the input voltage use the advanced button.

Independent Voltage Source - V1	$\mathbf{X}$
Functions O (none)	DC Value
⊙ PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)	Make this information visible on schematic:
SINE(Voffset Vamp Freq Td Theta Phi Ncycles)	
◯ EXP(V1 V2 Td1 Tau1 Td2 Tau2)	Small signal AC analysis(.AC)
SFFM(Voff Vamp Fcar MDI Fsig)	AC Amplitude:
○ PWL(t1 v1 t2 v2)	AC Phase:
O PWL FILE: Browse	Make this information visible on schematic: 🗹
Vinitial[V]: 0 Von[V]: 5	Parasitic Properties         Series Resistance[Ω]:         Parallel Capacitance[F]:
T delay[s]: 0	Make this information visible on schematic: 💌
Trise[s]: 1n	
Tfall[s]: 1n	
Ton[s]: 10n	
Tperiod[s]: 20n	
Ncycles: 3	
Additional PWL Points	
Make this information visible on schematic: 🗹	Cancel OK



All components necessary to build the inverter are now on the schematic. Next step requires to connect the component together using Edit > Draw Wire.





Let's now complete the circuit adding grounds (Edit > Place GND) where needed.

Right click on each ground symbol and make sure that all grounds are common.

Net Na	me		×					
GND(global node 0)								
ABC	0							
	Port Type:	None	~					
(Port type is only visible if drawn at the end of a wire.)								
Cancel OK								

Let's label a couple of nodes of the circuit with convenient names (for example the node where the input signal is applied and the node where the output of the inverter is taken) by using Edit > Net Name

Net Name 🛛 🔀	Net Name 🛛 🔀
GND(global node 0)	GND(global node 0)
Port Type: None 🗸	Port Type: Output 💙
(Port type is only visible if drawn at the end of a wire.)	(Port type is only visible if drawn at the end of a wire.)
Cancel OK	Cancel OK



At this point all we have to do is to specify the SPICE analysis we would like to run and where the models for the transistors are located.

Let's put the spice models in a file called <code>my.cmos</code> located in the directory: /opt-u/CAD/MySpiceLib

```
* Spice Models Library. Filename: my.cmos
.model NMOS_tr NMOS(kp=0.25m Vto=1 lambda=0.02)
.model PMOS_tr PMOS(kp=0.25m Vto=-1 lambda=0.02)
```

To add to the schematic the necessary spice directives and analysis we use: Edit > SPICE Directives and Edit > SPICE Analysis.

ic:	
Justification Left  Vertical Text	OK Cancel
	<
	.:1
c:	
Justification Left 💌 Vertical Text	OK Cancel
	c: Justification Left  Vertical Text C: Justification Left  Vertical Text

or even better use .include

Type Ctrl-M to start a new line.

Edit Simulation Command	×									
Transient ACAnalysis DC sweep Noise DC Transfer DC op pnt										
Perform a non-linear, time-domain simulation.										
Stop Time: 40n										
Time to Start Saving Data: 0										
Maximum Timestep: 10p										
Start external DC supply voltages at 0V: 📃										
Stop simulating if steady state is detected: 📃										
Don't reset T=0 when steady state is detected:										
Step the load current source: 📃										
Skip Initial operating point solution: 📃										
Syntax: .tran <tprint> <tstop> [<tstart> [<tmaxstep>]] [<option> [<option>]]</option></option></tmaxstep></tstart></tstop></tprint>										
or better , crain top wort										
Cancel OK										



4. Save the schematic As: inverter.asc



5. Set up the SPICE netlist generation preferences using: Tools > Control Panel > Netlist Option

🗸 Control Panel 🛛 🔀		
Operation     Provide the set of the se		
Style/Convention		
Semiconductor Models Default Devices[*] Default Libraries[*]		
[*] Setting remembered between program invocations.		
Reset to Default Values       OK     Cancel		

6. Run the Spice Simulation (Simulate > Run)

Linear Technology LTspice/Switcher	CAD III - inverter.asc	
<u>F</u> ile <u>E</u> dit Hierarchy <u>V</u> iew <u>S</u> imulate <u>T</u> ools <u>V</u>	<u>M</u> indow <u>H</u> elp	
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	CVCIDE invester State 0.254: 05: 100 Title /opst-uiCAX/WylSprodul.libing.ones	
🔛 inverter.raw		
Ons 2ns 4ns 6n	ns 8ns 10ns 12ns 14ns 16ns 14	8ns 20ns
P		

 Make sure there are no errors by checking View >SPICE Error Log Hops!! Here we notice the bulks are not properly connected, so we 1) fix the schematic, 2) run again the simulation and 3) check again for errors



8. In order to observe the traces we are interested in 1) right click on the inverter.raw window, 2) click on Add Trace or Visible Traces and 3) make your selections. Alternatively you can also click on the nodes of interest on the schematic window.



9. The spice netlist is automatically saved as inverter.net and can be opened using: View > Spice Netlist

```
* /home/ctalarico/MySpiceCir/inverter.asc
M_p N001 in out N001 PMOS_tr l=0.5u w=1u
M_n out in 0 0 NMOS_tr l=0.5u w=0.5u
Vdd N001 0 5V
Vin in 0 PULSE(0 5 0 1n 1n 5n 10n 5)
* CMOS Inverter
.tran 0 40n 0n 10p .tran lop 40n
.lib/opt-u/CAD/MySpiceLib/my.cmos
.backanno .include
.end
```