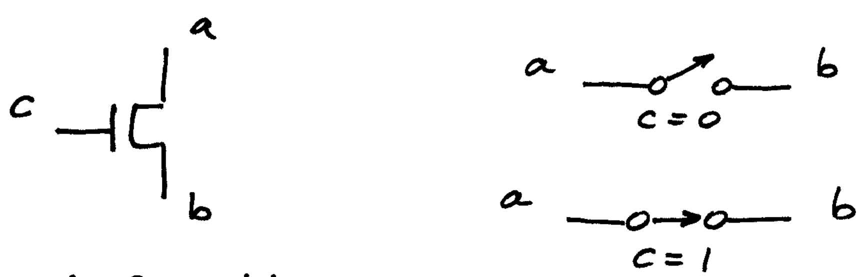
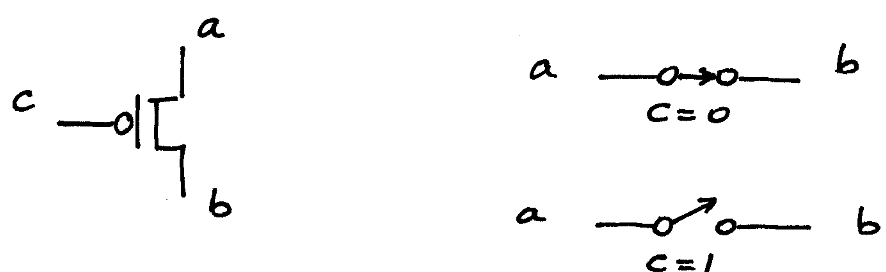
MOS Transistor Switches

In the case of digital circuits it is possible to model the MOS transistor in an extremely simplified way.
The easiest model is to see the MOSFET as a controlled switch (the gate controls the passage of current between source and drain).



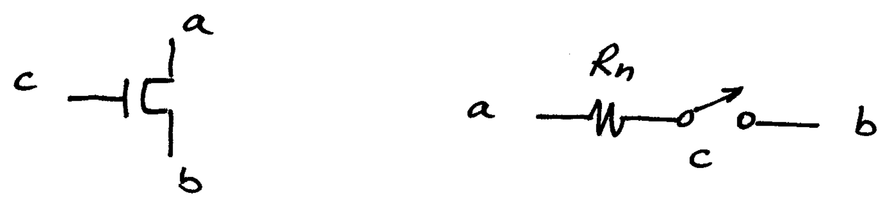
nMOS switch

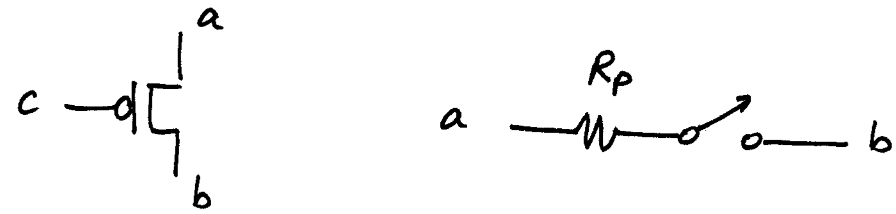


pMOS switch

In case we are interested in the switching time characteristic (not just the function) of the digital circuit we can model the MOSFET as a controlled switch with a certain resistance (drain-source equivalent resistance).

Since the MOSFET is a "non-linear" resistor the drain-source resistance can only be approximated.





A simple approximation for the source to drain resistance is to take the MOS resistance in linear region (the best-case value of the resistance is when the MOS is in saturation)

in linear region:

$$I_{ds} \simeq \beta \cdot (V_{gs} - V_T)\, V_{ds}$$

$$R = \frac{V_{ds}}{I_{ds}} \simeq \frac{1}{\beta\,(V_{DD} - V_T)}$$

in cut-off region

$$I_{ds} = 0$$

$$R = \infty$$

In saturation region:

$$I_{ds} \simeq \frac{\beta}{2} (V_{gs} - V_T)^2$$

$$R = \frac{V_{ds}}{I_{ds}} \cong \frac{V_{DD}}{\frac{\beta}{2} (V_{DD} - V_T)^2}$$

Summarizing:

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{T_n})} \propto \left(\frac{L}{W}\right)_n$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{T_p}|)} \propto \left(\frac{L}{W}\right)_p$$