Level One SPICE Model

Slides adapted from:

N. Weste, D. Harris, *CMOS VLSI Design*,
© Addison-Wesley, 3/e, 2004

R.T. Howe and C.G. Sodini,
Microelectronics: an Integrated Approach, Prentice-Hall

LEVEL 1 Model (Schichman-Hodges)

- Hand calculation and Simulation are both important
  - One doesn't replace the other !!!

- SPICE Level 1 is adequate for channel lengths longer than about 1.5µm. So why do we bother ?

- Using a more accurate SPICE model will change the "numbers" but not the trade-offs

LEVEL 1 equations

- *Cutoff Region,* $V_{gs} \leq V_T$

$$I_{ds} = 0$$

- *Linear Region,* $V_{ds} < V_{gs} - V_T$ (and $V_{gs} > V_T$)

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot V_{ds}) \cdot \left(V_{gs} - V_T - \frac{V_{ds}}{2} \right) \cdot V_{ds}$$

- *Saturation Region,* $V_{ds} \geq V_{gs} - V_T$ (and $V_{gs} > V_T$)

$$I_{ds} = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot V_{ds}) \cdot \left(V_{gs} - V_T \right)^2$$

LEVEL 1 equations

$$L_{eff} = L + XL - 2LD$$

LD Lateral diffusion into channel from source/drain diffusion
XL accounts for masking and etching effects

We will neglect these terms

$$W_{eff} = W + XW - 2WD$$

WD Lateral diffusion into channel from bulk along width
XW accounts for masking and etching effects

- If KP is not specified and UO and COX are entered the parameter is computed from:

$$KP = UO \cdot COX$$

- If COX is not specified is calculated from TOX:

$$COX = \frac{\varepsilon_{ox}}{TOX}$$

LEVEL 1 equations

$$V_T = VTO + GAMMA \cdot \left(\sqrt{PHI - V_{bs}} - \sqrt{PHI} \right)$$

if GAMMA is not specified :

$$GAMMA = \frac{(2 \cdot q \cdot \varepsilon_{si} \cdot NSUB)^{1/2}}{COX}$$

if PHI is not specified :

$$PHI = 2 \cdot \upsilon_T \cdot \ln\left(\frac{NSUB}{n_i} \right) \qquad with: \ \upsilon_T = \frac{KT}{q}$$

An Example of Parameters (1/2)

Parameter	Purpose	EE 114 Technology	
		NMOS	PMOS
KP	μC_{ox}	50 $\mu A/V^2$	25 $\mu A/V^2$
COX	ε_{ox}/t_{ox}	2.3 $fF/\mu m^2$	2.3 $fF/\mu m^2$
VTO	Threshold Voltage	0.5 V	0.5 V
LAMBDA	Channel length modulation	0.1 $V^{-1}\mu m/L$	0.1 $V^{-1}\mu m/L$
CGDO, CGSO	Gate-drain/source overlap capacitance	0.5 $fF/\mu m$	0.5 $fF/\mu m$
CJ	Zero bias area capacitance	0.1 $fF/\mu m^2$	0.3 $fF/\mu m^2$
CJSW	Zero bias sidewall capacitance	0.5 $fF/\mu m$	0.35 $fF/\mu m$

Source: R. Dutton and B. Murmann, Stanford University

An Example of Parameters (2/2)

Parameter	Purpose	EE 114 Technology	
		NMOS	PMOS
PB	Junction Potential	0.95 V	0.95 V
MJ	Area Junction Grading Coefficient	0.5	0.5
MJSW	Area Junction Grading Coefficient	0.33	0.33
HDIF	Half-length of S/D diffusion ($=L_{diff}/2$)	1.5 μm	1.5 μm
GAMMA	Bulk Threshold Parameter	0.6 $V^{1/2}$	0.6 $V^{1/2}$
PHI	Surface Potential (2ϕ)	0.8 V	0.8 V

Source: R. Dutton and B. Murmann, Stanford University

Example of SPICE Model

```
.model my_nmos nmos Kp=50u vto=0.5 lambda='lambda_n/L_n'
+ cox=2.3m capop=1 cjsw=0.5n cgdo=0.5n cgso=0.5n cj=0.1m
+ pb=0.95 mj=0.5 pbsw=0.95 mjsw=0.33 gamma=0.6 phi=0.8
+ acm=3 cjgate=0 hdif=1.5u
```