

Problem Set

Problem

Assume you got a new technology file for SPICE, so you need to do some hand calculations and related SPICE simulations to confirm what to expect from the technology at hand.

1. Assume a $W=40\mu\text{m}$ and $L=1.6\mu\text{m}$ NMOS device, with $KP=50\mu\text{A}/\text{V}^2$, $V_{TO}=0.5\text{V}$ and $COX=2.3\text{mF}/\text{m}^2$ and use the following lambda scaling rule:

$$\lambda(L) = \frac{0.1 \mu\text{m} \cdot \text{V}^{-1}}{L}$$

For a bias current of 0.25mA and assumed $V_{ds}=2.5\text{V}$, compute (by hand) the required V_{gs} and resulting C_{gs} as well as small-signal g_m and g_{ds} (ignoring all extrinsic capacitances).

2. Now compute by hand all extrinsic capacitances. Assume that $CGSO=0.5\text{nF}/\text{m}$ and $CGDO=0.5\text{nF}/\text{m}$. The junction capacitances are specified by the formulae given in Table 1. Table 1 also provides all needed HSPICE parameters. Compute the resulting C_{gd} , C_{gs} , C_{jdb} , C_{jsb} values (use $L_{diff}=3\mu\text{m}$).
3. Construct an HSPICE deck, to be used for finding out the dc operating point and “.op” output for the circuit of figure 1. Use $R=10\text{K}\Omega$, $R_i=20\text{K}\Omega$, $V_{DD}=5\text{V}$, $V_B=2.5\text{V}$, $I_B=250\mu\text{A}$ and the model formulation shown in table 2. Run the simulations and confirm your hand calculations in part 1. and 2. (These should be virtually identical to your hand calculations). State exactly how you arrive at the total nodal values provided by SPICE, starting from your results in 1. and 2. Your homework solution must include both your input and output files (Make sure to correctly specify V_I to get $V_{ds}=2.5\text{V}$).

Capacitance	Value	
c_{dtot}	$c_{gd}+c_{db}$	$c_{db} = c_{jdb}$
c_{gtot}	$c_{gs}+c_{gd}+c_{gb}$	
c_{stot}	$c_{gs}+c_{sb}$	$c_{sb} = c_{jsb}$
c_{gs}	$c_{gs}^* + c_{gso} \cdot W$	$c_{gs_ov} = c_{gso} \cdot W$
c_{gd}	$c_{gd}^* + c_{gdo} \cdot W$	$c_{gd_ov} = c_{gdo} \cdot W$

Triode region: $c_{gd}^*=c_{gs}^*=(1/2) \cdot c_{ox} \cdot W \cdot L$

Saturation region: $c_{gd}^*=0$; $c_{gs}^*=(2/3) \cdot c_{ox} \cdot W \cdot L$

$$V_{th} = V_{TO} + \text{GAMMA} (\text{PHI}+V_{SB})^{0.5} - \text{GAMMA} (\text{PHI})^{0.5}$$

Table 1.

Parameter	Purpose	nMOS
KP	μCox	$50\mu\text{A}/\text{V}^2$
COX	$\epsilon_{\text{ox}}/\text{tox}$	$2.3\text{fF}/\mu\text{m}^2$
VTO	Threshold Voltage	0.5V
LAMBDA	Channel Length Modulation	$0.1\text{V}^{-1}\mu\text{m}/\text{L}$
CGDO,CGSO	Gate-drain, gate-source overlap capacitance	$0.5\text{fF}/\mu\text{m}$
CJ	Zero Bias area capacitance	$0.1\text{fF}/\mu\text{m}^2$
CJSW	Zero bias sidewall capacitance	$0.5\text{fF}/\mu\text{m}$
PB	Junction potential	0.95V
MJ	Area junction grading coefficient	0.5
MJSW	Sidewall junction grading coefficient	0.33
HDIF	Half length of S/D diffusion ($L_{\text{diff}}/2$)	$1.5\mu\text{m}$
GAMMA	Bulk threshold voltage	$0.6\text{ V}^{1/2}$
PHI	Surface Potential	0.8V

$$C_{jdb} = \frac{AD \cdot CJ}{\left(1 + \frac{VDB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VDB}{PBSW}\right)^{MJSW}}$$

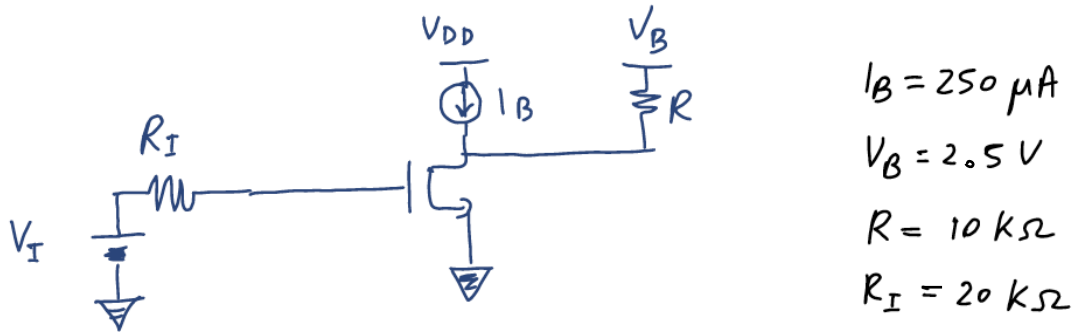
$$C_{jsb} = \frac{AS \cdot CJ}{\left(1 + \frac{VSB}{PB}\right)^{MJ}} + \frac{PS \cdot CJSW}{\left(1 + \frac{VSB}{PBSW}\right)^{MJSW}}$$

Table 2.

```
.param lambda=0.1u
.param Ln=1.6u

.model my_nmos nmos kp=50u vto=0.5 lambda='lambda/Ln' cox=2.3e-3 capop=1
+ cgdo=0.5n cgso=0.5n cj=0.1m cjsw=0.5n pb=0.95 mj=0.5 pbsw=0.95
+ mjsw=0.33 gamma=0.6 phi=0.8
+ acm=3 cjgate=0 hdif=1.5u
```

Figure 1.



Write a short report including:

1. Hand calculation (state clearly any assumption you make)
2. Hspice input and output files
3. Table showing hand calculation and SPICE results. Explain the discrepancy.
4. State exactly how you arrive at the total nodal values provided by SPICE, starting from your hand calculation results.