Layout Design Rules

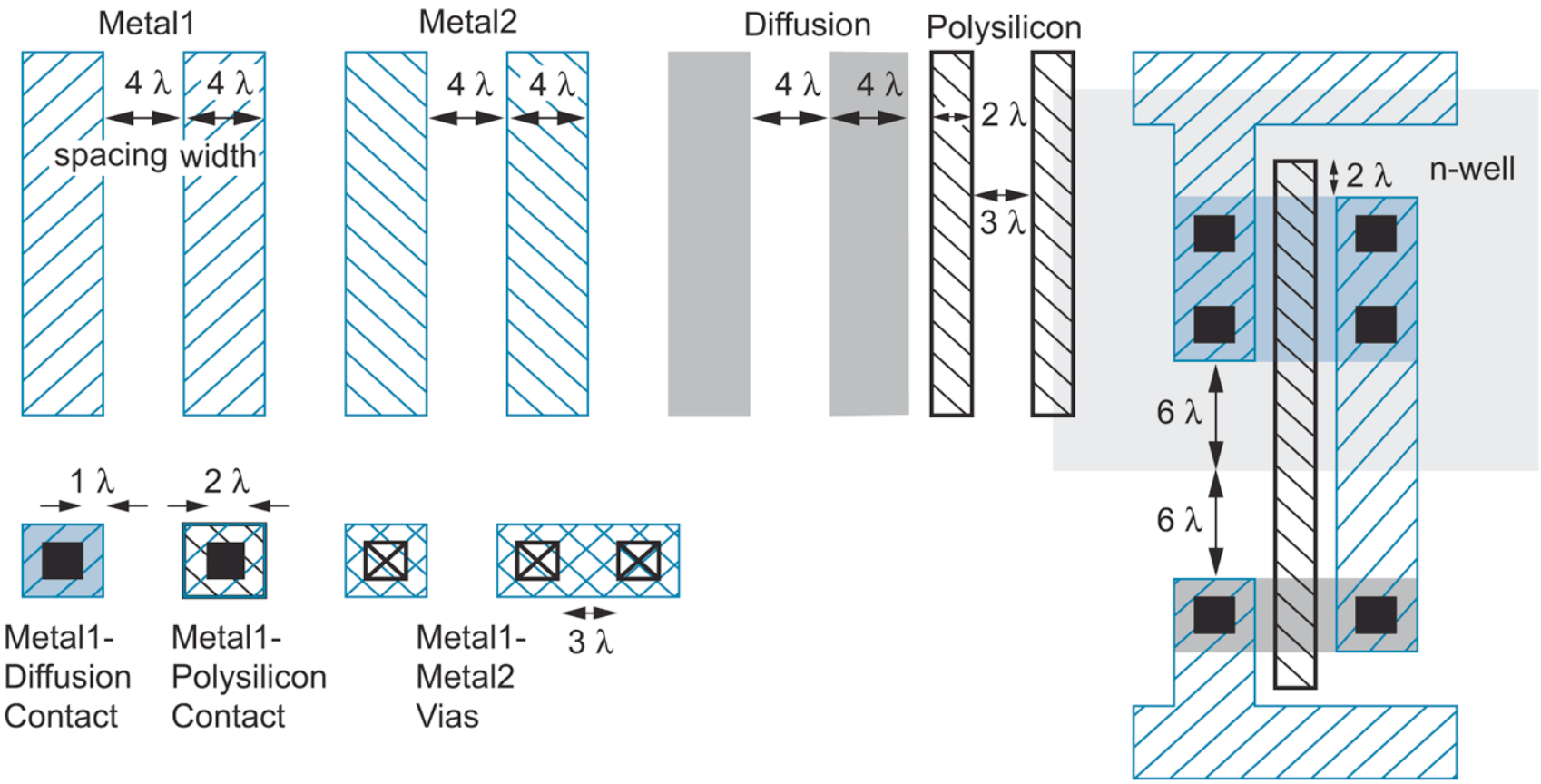

FIG 1.39 Simplified λ-based design rules for layouts with 2-metal layers (MOSIS)

Wiring Tracks

- A **wiring track** is the space required for a wire
  - 4λ width, 4λ spacing from neighbor = 8λ pitch
  - Transistors also consume one wiring track

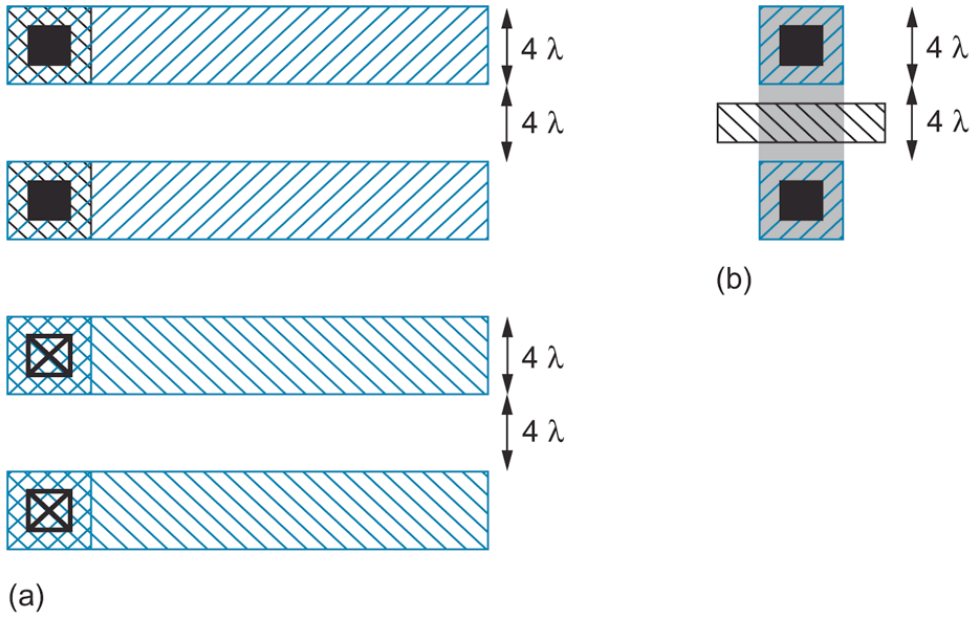

FIG 1.44 Pitch of routing tracks

Well Spacing

- Wells must surround transistors by 6λ
  - Implies 12λ between opposite transistor flavors
  - Leaves room for one wire track

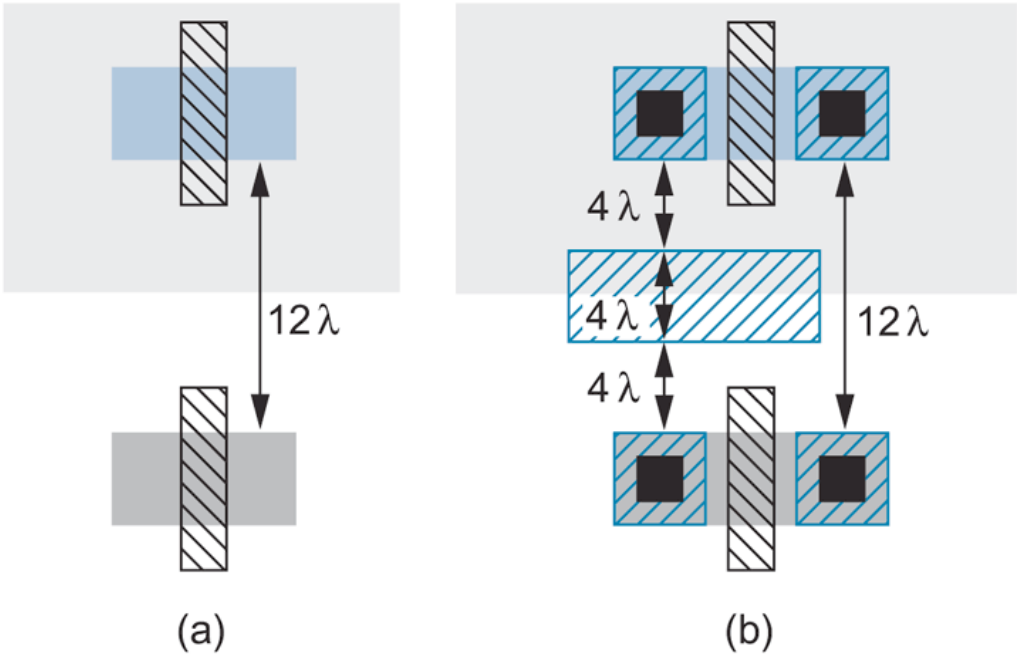

FIG 1.45 Spacing between nMOS and pMOS transistors

Inverter Standard Cell Area